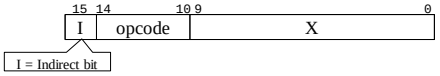
Easy I
A Simple Accumulator Processor
Instruction Set Architecture (ISA)

Instruction Format (16 bits)



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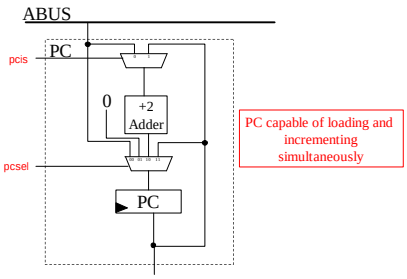
Instruction Set Architecture (ISA)

Instruction Set

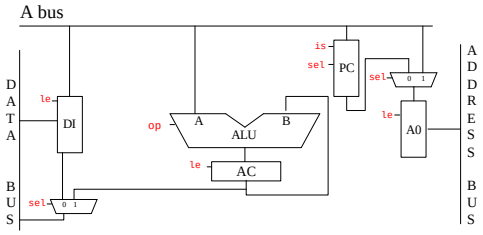
Name	Opcode	Action I=0	Action I=1
Comp	00 000	AC ? not AC	AC <- not AC
ShR	00 001	AC ? AC / 2	AC ? AC / 2
BrN(i)	00 010	AC < 0 ? PC ? X	AC < 0 ? PC ? MEM[X]
Jump(i)	00 011	PC ? X	PC ? MEM[X]
Store(i)	00 100	MEM[X] ? AC	MEM[MEM[X]] ? AC
Load(i)	00 101	AC ? MEM[X]	AC ? MEM[MEM[X]]
And(i)	00 110	AC ? AC and X	AC ? AC and MEM[X]
Add(i)	00 111	AC ? AC + X	AC ? AC + MEM[X]

Easy all right … but universal it is!

Inside the Easy-I PC



Easy I
Data Paths (with control points)



Easy I
Control Unit State Transition Table (Part I)

Curr State	opcode	I	AC:15	Next State	ALU op	Mem OP	PC sel	PC is	DI le	AC le	AO sel	AO le	EDB sel
reset1	xx xxx	x	x	reset2	XXX	NOP	01	X	0	0	X	0	X
reset2	xx xxx	x	x	fetch	XXX	NOP	10	1	0	0	0	1	X
fetch	00 00x	0	x	sopr	XXX	NOP	11	X	1	0	X	0	X
fetch	00 010	0	x	brn1	XXX	RD	11	X	1	0	X	0	X
fetch	00 011	0	x	jump	XXX	RD	11	X	1	0	X	0	X
fetch	00 100	0	x	store1	XXX	RD	11	X	1	0	X	0	X
fetch	00 101	0	x	load1	XXX	RD	11	X	1	0	X	0	X
fetch	00 11x	0	x	aopr	XXX	RD	11	X	1	0	X	0	X
aopr	00 110	x	x	fetch	AND	NOP	10	1	0	1	0	1	X
aopr	00 111	x	x	fetch	ADD	NOP	10	1	0	1	0	1	X
sopr	00 000	x	x	fetch	NOTB	NOP	10	1	0	1	0	1	X
sopr	00 001	x	x	fetch	SHRB	NOP	10	1	0	1	0	1	X

Easy I
Control Unit State Transition Table (Part II)

Current State	opcode	I	AC:15	Next State	ALU op	Mem OP	PC sel	PC is	DI le	AC le	AO sel	AO le	EDB sel
store1	xx xxx	x	x	store2	XXX	NOP	11	X	0	0	1	1	X
store2	xx xxx	x	x	store3	XXX	WR	10	1	0	0	0	1	1
load1	xx xxx	x	x	load2	XXX	NOP	11	X	0	0	1	1	X
load2	xx xxx	x	x	load3	XXX	RD	11	X	1	0	X	0	X
load3	xx xxx	x	x	fetch	XXX	NOP	10	1	0	1	0	1	X
brn1	xx xxx	x	0	fetch	XXX	NOP	10	1	0	0	0	1	X
brn1	xx xxx	x	1	brn2	XXX	NOP	10	1	0	0	0	1	X
brn2	xx xxx	x	x	fetch	XXX	NOP	10	0	0	0	1	1	X
jump	xx xxx	x	x	fetch	XXX	NOP	10	0	0	0	1	1	X

CU with 14 states => 4 bits of state