University of Puerto Rico
Mayagüez Campus
College of Engineering
Department of Electrical and Computer Engineering
Bachellor of Science in Electrical Engineering

Course Syllabus

1. General Information:

Alpha-numeric codification: ICOM 4215
Course Title: Computer Architecture and Organization
Number of credits: 3
Contact Period: 3 hours of lecture per week
Required in ICOM and Elective in INEL

2. Course Description:

English: Architectural aspects of general purpose computers: addressing modes, data types, registers, support for programming languages and operating systems. Comparative study of commercial architectures. Organizational aspects of general purpose computers, central processing unit, control unit, microprogramming, architecture and logic units, memory systems, input/output systems.

Spanish: Aspectos arquitecturales de computadoras de propósito general: sets de instrucciones, modos de direccionamiento, tipos de datos, registros, apoyo para lenguajes de programación y sistemas operativos. Estudio comparativo de arquitecturas comerciales. Aspectos organizacionales de computadoras de propósito general: unidad central de procesamiento, unidad de control, microprogramación, unidades aritméticas y lógicas, sistemas de memoria, sistemas de entrada/salida.

3. Pre/Co-requisites and other requirements:

Prerequisite: INEL4206

4. Course Objectives:

The objective is to provide the student with various architectural philosophies in defining hardware and software interface within a computer system. In addition, the students will learn how to design a simple CPU.
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5. Instructional Strategies:

☒conference ☒discussion ☐computation ☐laboratory

☒seminar with formal presentation ☐seminar without formal presentation ☐workshop

☐art workshop ☐practice ☐trip ☐thesis ☐special problems ☐tutoring

☐research ☒other, please specify: Team work, workshops

6. Minimum or Required Resources Available:

Computer labs, high level language compilers, simulator for digital systems.

7. Course time frame and thematic outline[1]

Outline	Contact Hours
Introduction to computer architecture	5
RISC and CISC architectures	3
Contemporary microprocessors	3
Data paths	1
Control Unit	6
Microprogramming	3
Arithmetic Units	3
Caches	2
Virtual Memory	2
Projects	15
Exams	2
Total hours: (equivalent to contact period)	45

8. Grading System

☒Quantifiable (letters) ☐ Not Quantifiable

9. Evaluation Strategies

The faculty member teaching the course will provide the student with the evaluation strategy he/she will be using throughout the semester. This will be done within the first week of classes.

	Quantity	Percent
Exam 1	**1**	**15%**
Exam 2	**1**	**15%**
Final Exam	**1**	**15%**
Homeworks and quizzes	**1**	**5%**
Project 1	**1**	**15%**
Project 2	**1**	**10%**
Project 3	**1**	**15%**
Attendance & Punctuality		**5%**
Other (Specify): Discussion and participation, teamwork		**5%**
TOTAL:		**100%**

Note: see instructor sheet for evaluation strategy details.

10. Bibliography:

- Heuring, V. P. and Jordan, H. F. Computer Systems Design and Architecture, 2nd Edition, Prentice Hall, 2007.
- Reference: William Stallings, Computer Organization and Architecture: Designing for Performance, Eighth edition, Prentice Hall, 2009.

11. According to Law 51

Students will identify themselves with the Institution and the instructor of the course for purposes of assessment (exams) accommodations. For more information please call the Student with Disabilities Office which is part of the Dean of Students office (Chemistry Building, room 019) at (787)265-3862 or (787)832-4040 extensions 3250 or 3258.

12. Contribution of the Course to meeting the requirements of Criterion 5:

Math	Basic Science	General	Engineering Topic
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12. Course Outcomes	**Map to Program Outcomes**
1. Describe different computer architectures	(a)
2. Compare different computer architectures	(a)
3. Design a computer program to simulate the operation of a simple CPU	(c)
4. Design hardware for a simple CPU	(c)
5. Represent CPU specifications using RTN or metalanguages	(k)
6. Use digital circuit simulator or HDL to test a CPU design	(k)

Person(s) who prepared this description and date of preparations: José Navarro.
Submitted by: Isidoro Couvertier, Comité Timón, October 2007.