ICOM 4215: Project 2 Spring 2011

Processor ALU

Phase 1: Implement an Adder, a Multiplier and a Division Unit

Phase 2: Complete the ALU

Today: April 12, 2011

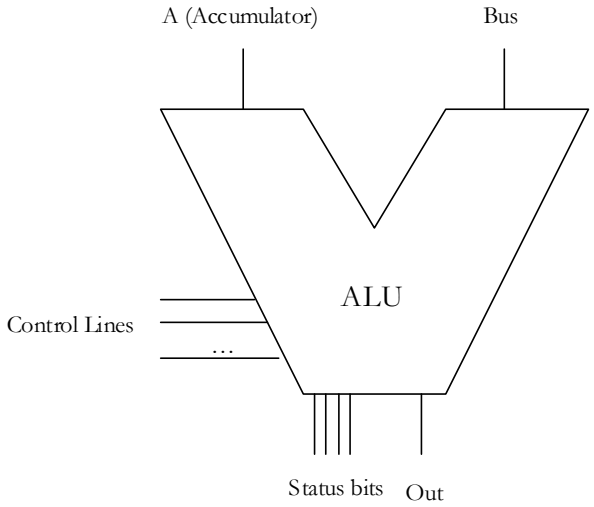
Due Date: Phase 1: 4/29/2011

Due Date: Phase 2: 5/6/2011

Submission:

- Via oral exam, aka "Happy Hour" with simulator.
- Report, via email

Project:
ALU design of the RISC AR. The ALU implements arithmetic and logic operations Most of the arithmetic or logic operations will require two operands. In the first phase you will implement three functional units. In the second phase of the project, you will implement the rest of the ALU. The ALU will include the logic necessary to implement the and, or, xor, not, add, mul, div, neg, rotate left and right, and dec.



The language to implement the Project will either be Verilog or VHDL (your Choice). The design should be clear enough to understand its components. We suggest you implement a testbench for input of the test signals.