ICOM 4215 Project 3 Fall 2010 Processor Simulator

Today: May 5, 2011

Due date: May 18, 2011

Points: 100 points (Penalties: Next day: -10 points, Two days late: -25 points, Three days late: -40 points, Four days late or more: not accepted)

Group project – Three students per group

Submission:

- Via oral exam, aka “Happy Hour”
- Report, via email

Project

Design the controller for the RISC A2 previously designed in Projects 1 and 2. The following sections describe the processor.

Project requirements

Your team will design all the components of the processor and determine the control lines. Then the only part to turn in is the simulation either in Verilog or VHDL of the controller. As deliverable your group needs to specify all the components of the processor and the controller design and behavior. Notice that each group must decide whether to work with a 2 bus architecture or a 3 bus architecture. In addition, each group will have a different processor design, therefore, the controller’s characteristics are different.

The report will contain: detailed schematics of the processor design. Detailed explanation of the controller, timing diagrams showing the behavior of the controller, appendix containing the code developed in VHDL or VERILOG.

The oral exam will be individually graded. Each student must demonstrate the proficiency and capability of designing a processor and a controller.

General Processor Description: RISC AR2 (Same as before)

The RISC AR2 is a processor designed by your professor, taking the ideas from the Simple Risc Processor, from the Jordan and Heuring textbook, a processor designed by Manuel Jimenez, Sunil Vaidya, Bradley Vansant, and Dave Dorner for the EE 813 graduate course at Michigan State University, and the processor designed by Adem Kader and Mustafa Paksoy for the E25 : COMPUTER ARCHITECTURE course at Swathmore University.

Processor Features:

- 8-bit internal data bus
- Internal 256-word 8 bit wide program memory

- 8 byte register file
- On chip 4 bits hardware multiplier providing 8 bit results.
- 2 external I/O pins
- RISC instruction set: 20 instructions
    - 5 arithmetic
    - 3 logical
    - 5 data transfer
    - 6 control flow instructions
    - 1 machine control

Processor Block Diagram

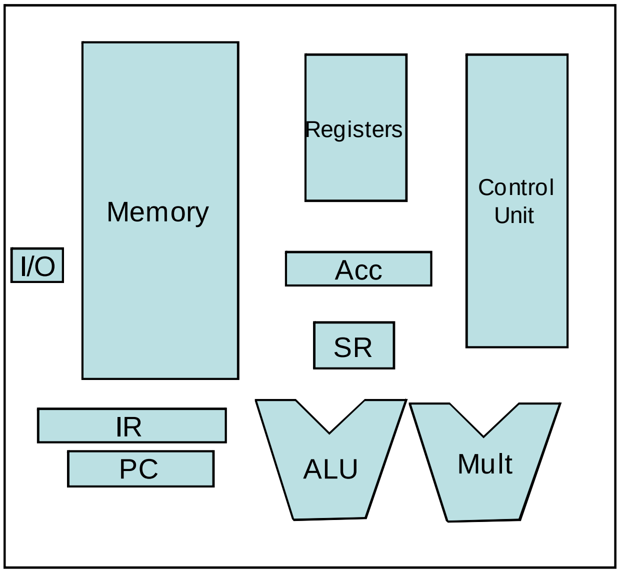

Figure 1: Block diagram of the RISC AR2

Memory and Registers

The size of the memory is 256 organized as 256 addresses of 1 byte each.

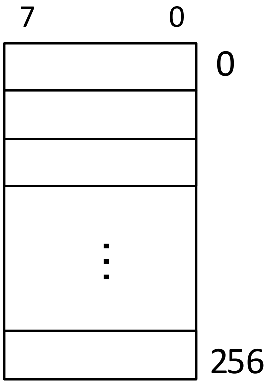

Figure 2: Visual illustration of the memory of the RISC AR2

Internally, the processor has 8 general purpose registers, 8 bits each. The names of the registers are from **R0** to **R**7.

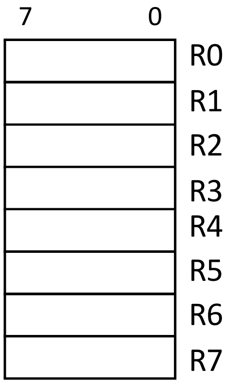

Figure 3: Visual illustration of the general purpose register structure of the RISC AR2

The processor has a 8 bit program counter called **PC**, an 8 bit accumulator called **A**, and a 16 bit instruction register called **IR**. There is a 4-bit status register called **SR**. The format of the Status Register is | Z | C | N | O | where Z is zero, C is Carry, N is negative, and O is overflow. When instructions are saved into memory, big endian ordering is used.

Four addressing modes are supported by the processor:

a) Implicit
b) Immediate
c) Direct
d) Register indirect

The list below shows the different addressing modes supported and the corresponding instruction formats for each (see figures 4 to 7).

(a) *Implicit addressing*: The only operand needed is contained in the accumulator (A)

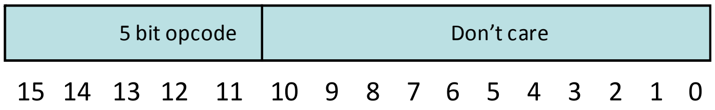

Figure 4: Instruction format for the *Implicit* addressing mode

(b) *Immediate addressing*: The data to be operated is part of the instruction itself.

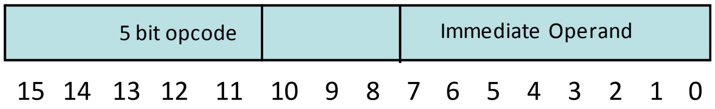

Figure 5: Instruction format for the *Immediate* addressing mode

(c) *Direct*: The memory location is indicated within the instruction

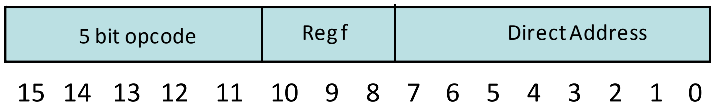

Figure 6: Instruction format for the *Direct* addressing mode

(c) *Register indirect*: Register f points to the memory location to be accessed.

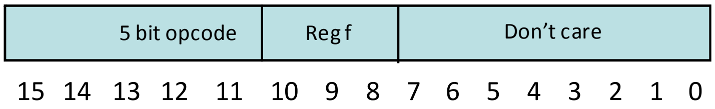

Figure 7: Instruction format for the *Register Indirect* addressing mode

Instruction Set

The following table is a summary of the instruction set of the RISC AR2. Note that register f refers to one of the eight general purpose registers.

Table 1: Instruction set of the RISC AR2

Item	Opcode	Name (Mnemonic)	Operands	Addressing Modes	Operation	Details
1	00 000	AND rf	Accumulator, register f	Direct	A ← A and rf	Logical AND
2	00 001	OR rf	Accumulator, register f	Direct	A ← A or rf	Logical OR
2	00 010	XOR rf	Accumulator, register f	Direct	A ← A xor rf	Logical XOR
3	00 011	ADDC rf	Accumulator, register f	Direct	A ← A + (rf) +carry	Addition with carry
4	00 100	MUL rf	Four least significant bits of accumulator , four least significant bits of register f	Direct	A ← A *(rf)	Multiply
5	00 101	DIV rf	Four least significant bits of accumulator , four least significant bits of register f	Direct	A ← A / (rf)	Division
6	00 110	NEG	Accumulator	Implicit	A ← not(A)	Two's complement
7	00 111	RLC	Accumulator	Implicit	A ← A6..A0 &Cf, Cf ←A7	Rotate left through carry
8	01 000	RRC	Accumulator	Implicit	A ← Cf & A7..A1, Cf ←A0	Rotate right through carry
9	01 001	DEC	Accumulator	Implicit	A ← A-1	Decrement accumulator
10	01 010	LDA rf	Accumulator, register f	Direct	A ← (rf)	Load accumulator from register f

11	01 011	STA rf	Accumulator, register f	Direct	(rf)← A	Store accumulator to register f
12	01 100	LDA addr	Accumulator	Direct	A ← [addr]	Load accumulator from memory location addr
13	01 101	STA addr	Accumulator	Direct	[addr]← A	Store accumulator to memory location addr
14	01 110	LDI Immediate	Accumulator	Immediate	A ← Immediate	Load accumulator with immediate
15	10 000	BRZ	Status register	Implicit	If Z=1, PC ←r7	Branch if Zero
16	10 001	BRC	Status register	Implicit	If C=1, PC ←r7	Branch if Carry
17	10 010	BRN	Status register	Implicit	If N=1, PC ←r7	Branch if Negative
18	10 011	BRO	Status register	Implicit	If O=1, PC ←r7	Branch if Overflow
19	11 111	STOP	PC	Implicit		Stop execution
20	11 000	NOP		Implicit		No operation