A BiCMOS Low Power, Low Voltage Current Mirror

Andrés Rosado-Sepúlveda
Advisor: Manuel Jiménez

Electrical and Computer Engineering Department
University of Puerto Rico, Mayagüez Campus
Mayagüez, Puerto Rico 00681-5000
andresr@ieee.org

Abstract

This paper presents the development of a BiCMOS current mirror (CM) with requirements to operate with voltages lower than 1.5 volts and currents in the range of microamperes. A discussion of traditional CM configurations is presented as well as improvements achieved through BiCMOS technology. Details of the proposed configuration are provided highlighting its novel characteristics. Also included are future plans to continue evaluating and refining the proposed structure.

1. Introduction

The ever-rising proliferation of portable electronics has increased the need for low power, low voltage devices. One possible approach to achieve this goal is by designing power efficient, low voltage base components and building blocks. This would enable to achieve both higher integration levels in VLSI technology and more power-efficient systems.

Current mirrors are one of the building blocks more widely used in many applications. However, they usually require either a relatively high voltage or input current to operate properly. Thus, new current mirrors that consume less power will serve well the increasing need for low power consuming building blocks.

BiCMOS technology has been increasingly accepted for developing low power current mirrors, especially in the communications area. In this field, low power is needed mostly because of the limited resources of portable communications devices.

In this paper we describe the work in progress to develop a BiCMOS CM configuration intended to meet the requirements of low supply voltage and low power consumption. The designed structure combines the high output impedance of a bipolar Wilson configuration with the low current requirements of MOS transistor in a configuration suitable for low voltage operation.

This paper has been organized as follows. In the next section, traditional CM configurations in bipolar and MOS technologies are reviewed. Section 3 presents a discussion of salient BiCMOS implementations reported in the recent literature. Next, a discussion of the proposed BiCMOS current mirror is presented, to conclude with an overview the work in progress to complete such a design.

2. Traditional Current Mirrors

In bipolar or MOS technology, several current mirror configurations have been developed. Among them, the cascode, Wilson, and Widlar configurations are the most widely used when only one technology is available.

The cascode current mirror, shown in Figure 1, is widely used in CMOS technology. This configuration has high output impedance, which reduces the circuit gain error, improving its input current. Although this is a desirable property in a current mirror, it requires high input and output voltages, making it unfeasible for low voltage, low power applications. Moreover, the configuration also exhibits a high dependence on the transistor's beta.

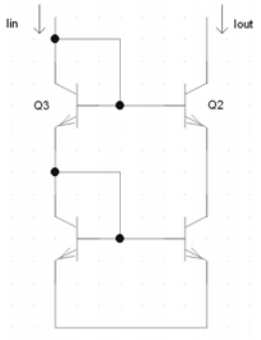

Figure 1: Cascode Current Mirror

The Wilson current mirror, shown in Figure 2, has similar input current and output voltage requirements as the cascode configuration. However, its output resistance is reduced to decrease the dependency of the circuit on the beta of the transistors.

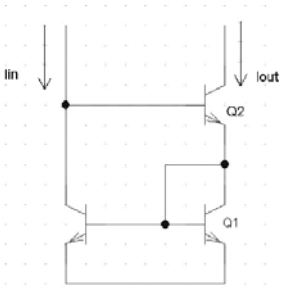

Figure 2: Wilson Current Mirror

The Widlar current source, shown in Figure 3, can handle currents in the order of microamperes. Resistor **R** is used as a feedback element to control the output current. Although this configuration can work with relatively low voltages, it may be infeasible to implement if the available area is small.

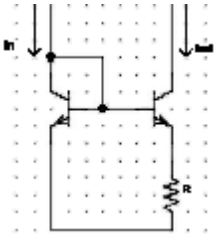

Figure 3: Widlar Current Mirror

3. BiCMOS CM Configurations

With the increasing acceptance of BiCMOS technology, several approaches have been reported to overcome the deficiencies identified in traditional approaches.

A low power BiCMOS current mirror configuration proposed by Sasaki et al is shown in Figure 4 [Sasaki92]. It has been reported to be stable for voltages around 1V and currents in the range of microamperes. Unfortunately, some chipmakers do not offer support for depletion mode MOS transistors, making difficult its implementation.

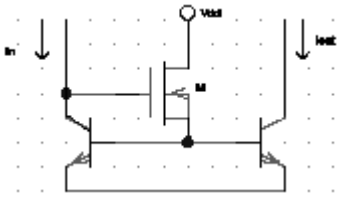

Figure 4: Sasaki's Current Mirror

Another way to implement low voltage current mirrors is by using a DC level shifter, as shown in Figure 5 [Ramirez94]. The resulting structure is suitable for high-speed applications, since its reaction time is in the order of nanoseconds. In addition, it can be implemented in different technologies working at voltages around 1V. Implementing the level shifter however, requires two current sources, which increase the amount of current necessary for proper operation.

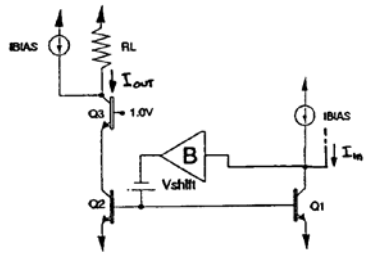

Figure 5: BiCMOS Current Mirror with DC Level Shifter

A configuration proposed by Serrano et al, uses a voltage clamp to reduce the input voltage, as shown in Figure 6 [Serrano99]. It can operate with input currents of the order of nanoamperes and the output current can be in a range from around 100 nanoamperes down to a few picoamperes. This configuration can handle high capacitances and the MOS transistors can operate in any mode. However, it requires more current than normal to operate properly because it uses an operational transconductance amplifier to create the voltage clamp.

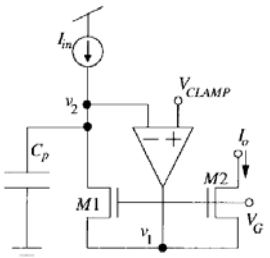

Figure 6: BiCMOS Current Mirror with Voltage Clamp

A merged BiCMOS current mirror, shown in Figure 7, can be used to achieve low power consumption [Ueno91]. It can manage currents in the range of 10 microamperes and can react in the range of nanoseconds. However, the mirror effect depends on the input and output voltage and it is limited by the number of collectors the transistor can have. Moreover, this configuration is very sensitive to the Early effect.

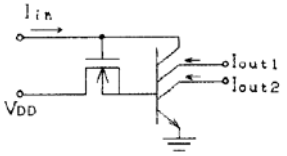

Figure 7: BiCMOS Merged Current Mirror

4. Proposed Configurations

From the discussion in the previous sections, it is noted that still, there is room for improvement in CM configurations.

4.1 Pseudo-Wilson BiCMOS Current Mirror

One of the BiCMOS current mirrors proposed in this research is based on the Wilson configuration presented earlier. Figure 8 illustrates the current mirror structure.

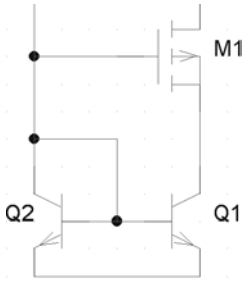

Figure 8: Pseudo-Wilson BiCMOS Current Mirror

The bipolar Wilson configuration was selected because it can handle currents in the range of microamperes and has high output impedance. It is not followed completely because it causes some stability problems.

The top bipolar transistor in the original Wilson configuration is replaced with a PMOS transistor (M1). Since M1 does not require a gate current, the input current of the overall configuration is improved. The output resistance is also increased.

The configuration will need low input voltage because the gate-drain junction can be

inversely polarized, which reduces the needed voltage. Thus the design is expected to achieve both stability at low supply voltages and small current requirements.

The output current versus the output voltage at 1 μA is shown in Figure 9. It shows that it handles properly small currents and with a minimum input voltage of 0.7 V.

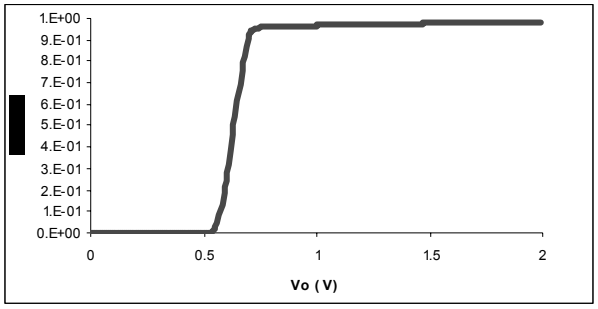

Figure 9: Output current vs. voltage for the Pseudo-Wilson BiCMOS CM

4.2 BiCMOS Wilson Current Mirror

The second configuration is based on the MOS Wilson current mirror. It replaces the top MOS transistor with a bipolar (Q1), as shown in Figure 10.

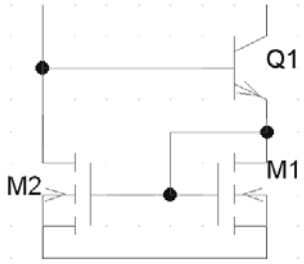

Figure 10: BiCMOS Wilson Current

The configuration will need low input voltage because the base-emitter junction voltage of a bipolar transistor is smaller than the gate-source junction voltage for a MOS. Thus this design is also expected to achieve stability at low supply voltages and small currents requirements.

5. Future Work

This research is still in progress. Currently, the models of the transistors to be used to simulate the current mirrors are under development. In the next stages of this work, the proposed current mirror will be simulated for establishing its sensitivity, voltage and current requirements, temperature dependence, dependence on the transistor beta and Early Effect and other measures that would allow to compare its performance with other established configurations.

References

[Ramirez94] Ramirez-Angulo, J., "Low voltage current mirrors for built-in current sensors", 1994 IEEE International Symposium on Circuits and Systems, 1994. ISCAS '94, Volume: 5, 1994 Page(s): 529 -532 vol. 5.

[Sasaki92] Sasaki, M.; Ogata, Y.; Taniguchi, K.; Ueno, F.; Inoue, T., "Bi-CMOS current mode circuits with 1 V supply voltage and their application to ADC", 1992 IEEE International Symposium on Proceedings, 1992, vol. 3, pp: 1273 –1276.

[Serrano99] Serrano-Gotarredona, T.; Linares-Barranco, B.; Andreou, A.G., "Very wide range tunable CMOS/bipolar current mirrors with voltage clamped input", Circuits and Systems I: IEEE Transactions on Fundamental Theory and Applications, Volume: 46 Issue: 11, Nov. 1999 Page(s): 1398 –1407

[Ueno91] Ueno, F.; Inoue, T.; Taniguchi, K.; Yamashita, T., "Current-mode multiple valued logic circuit by merged Bi-CMOS transistors", Circuits and Systems, Proceedings of the 33rd Midwest Symposium on 1990, 1991 Page(s): 877 -880 vol.2