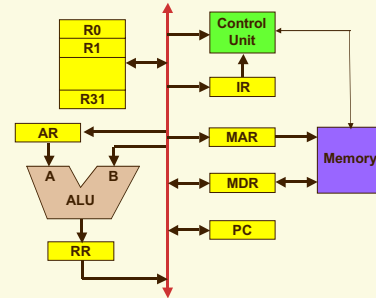
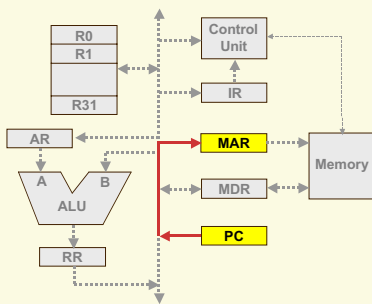


Data Path y Unidad de Control

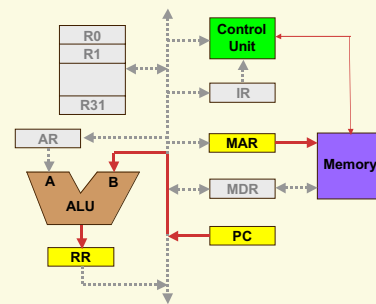
Single Bus Data Path



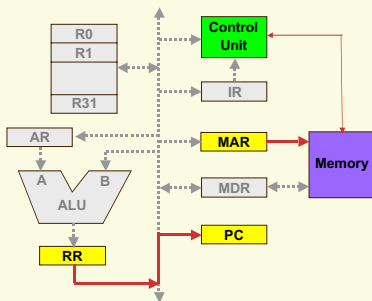
Fetch - Paso 1



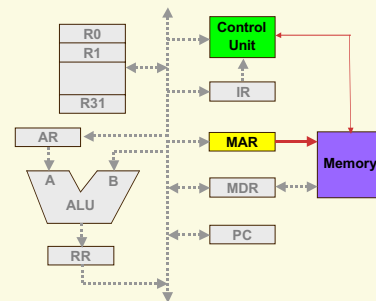
Fetch - Paso 2

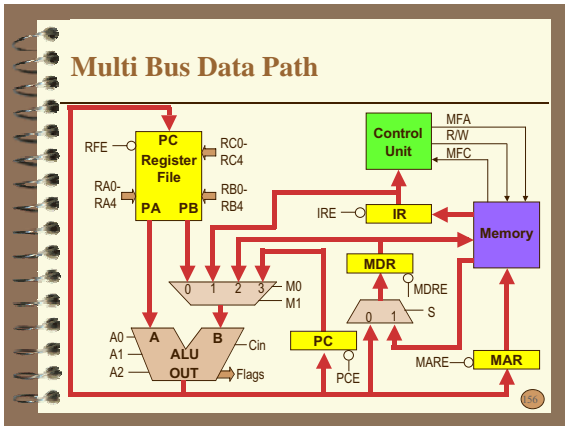
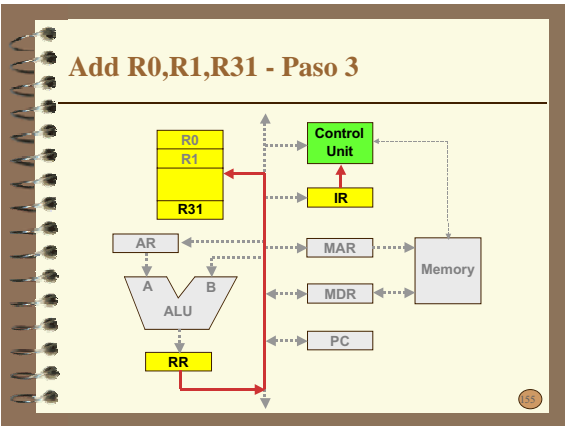
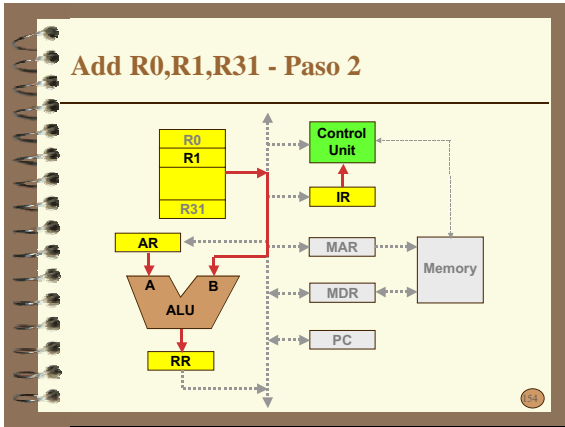
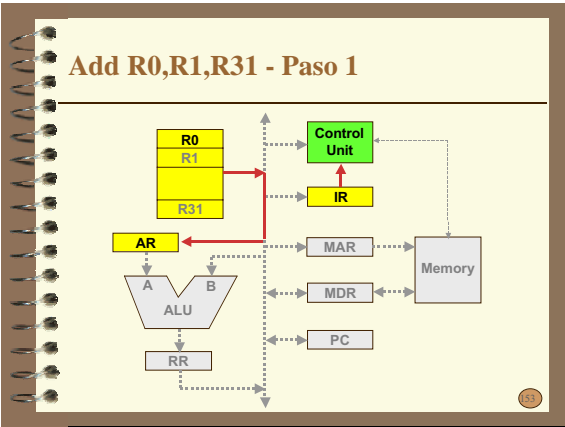
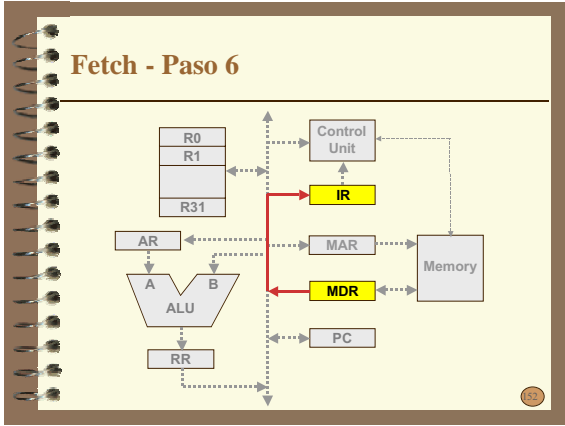
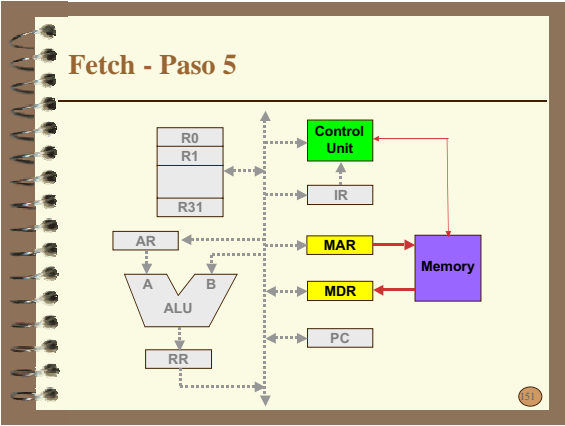


Fetch - Paso 3



Fetch - Paso 4 (se repite)

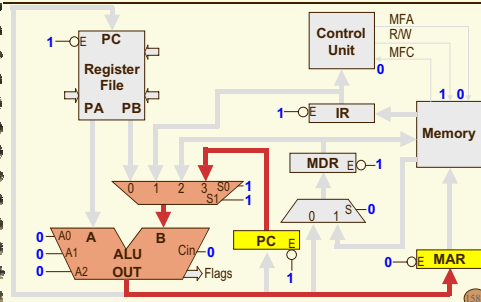




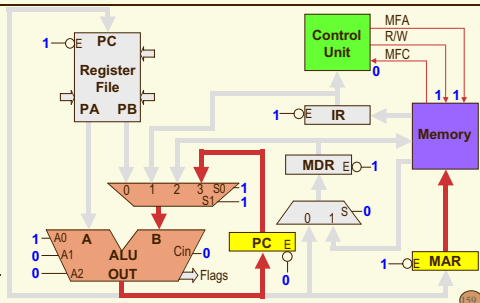
Funciones del ALU

A2-A0	OUT
000	B
001	B+4
010	A+B
011	A-B
100	A or B
101	A and B
110	SAR B
111	SLL B

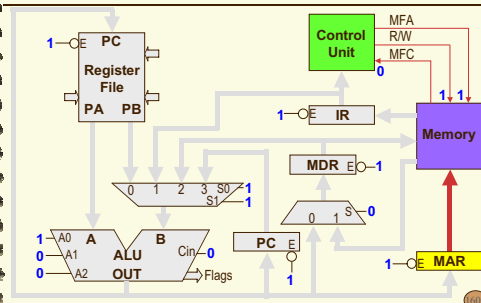
Fetch- Paso 1



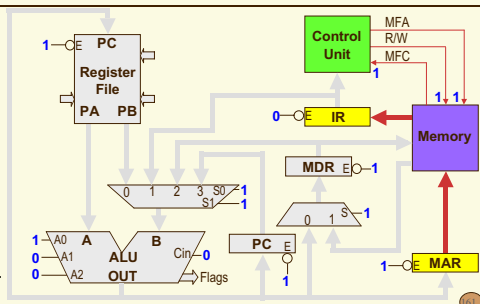
Fetch- Paso 2



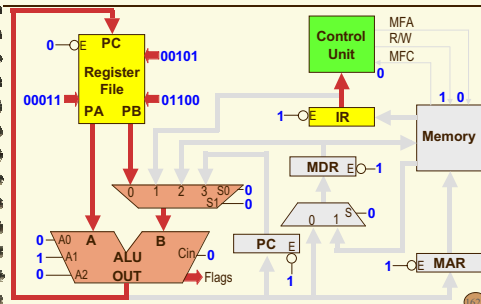
Fetch- Paso 3 (se repite)

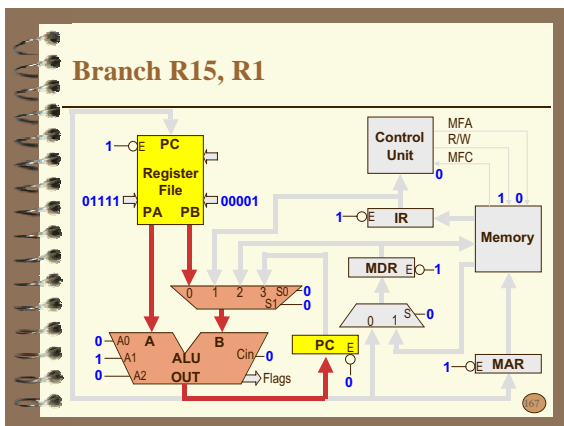
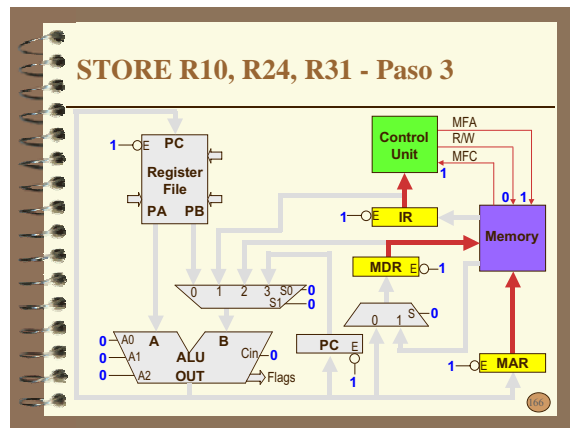
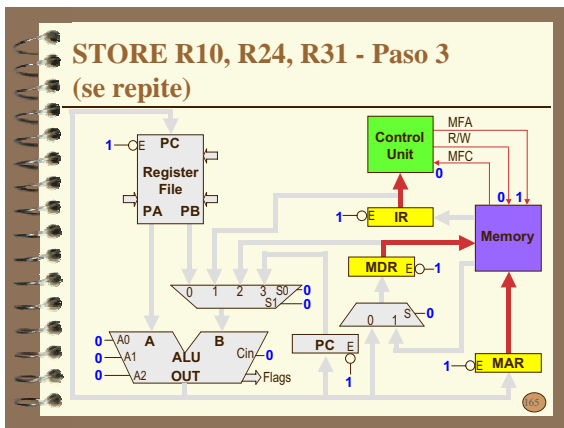
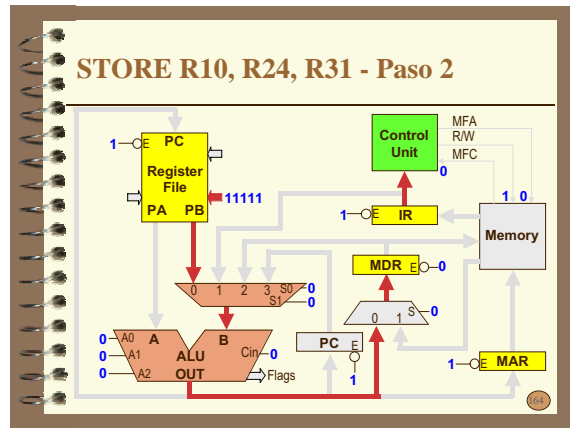
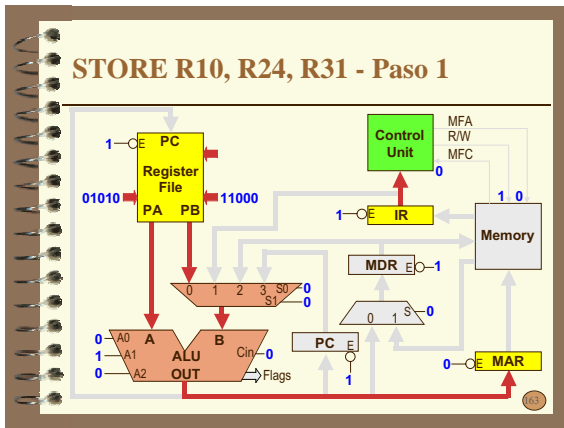


Fetch- Paso 4



ADD R3, R12, R5 - Paso 1





Señales de Control

Fetch

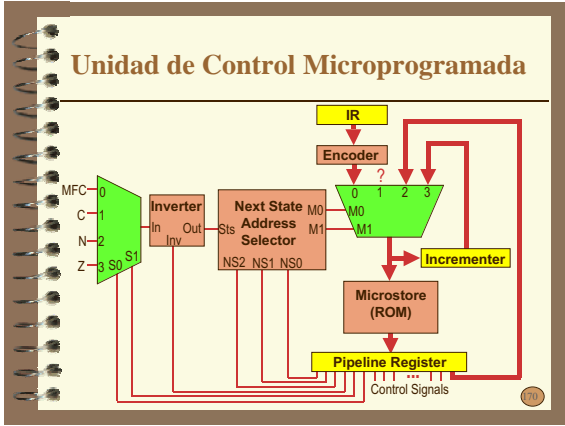
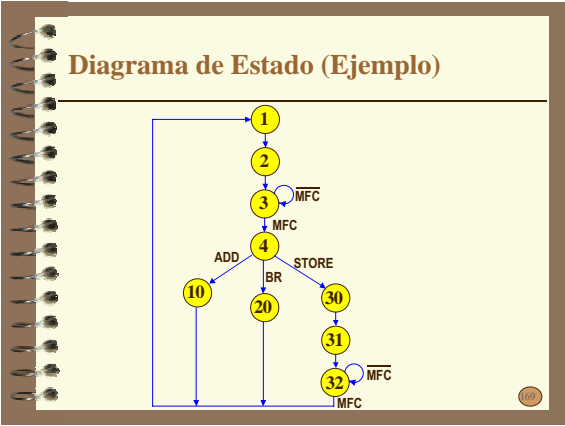
Paso	A2-A0	M1-M0	S	RA2-RA0	RB2-RB0	RC2-RC0	RFE	IRE	PCE	MARE	MDRE	RW	MFA	Cin
1	000	11	X	XXXXX	XXXXX	XXXXX	1	1	0	1	X	0	X	
2	001	11	X	XXXXX	XXXXX	XXXXX	1	1	0	1	1	1	1	X
3	XXX	XX	X	XXXXX	XXXXX	XXXXX	1	1	1	1	1	1	1	X
4	XXX	XX	X	XXXXX	XXXXX	XXXXX	1	0	1	1	1	1	1	X

ADD R3,R12,R5

Paso	A2-A0	M1-M0	S	RA2-RA0	RB2-RB0	RC2-RC0	RFE	IRE	PCE	MARE	MDRE	RW	MFA	Cin
10	010	00	X	00011	01100	00101	0	1	1	1	1	X	0	X

STORE R10,R24,R32

Paso	A2-A0	M1-M0	S	RA2-RA0	RB2-RB0	RC2-RC0	RFE	IRE	PCE	MARE	MDRE	RW	MFA	Cin
30	010	00	X	01010	11000	XXXXX	1	1	1	0	1	X	0	X
31	000	00	X	XXXXX	11111	XXXXX	1	1	1	1	0	X	0	X
32	XXX	XX	X	XXXXX	XXXXX	XXXXX	1	1	1	1	1	0	1	X



Next State Address Selector

NS2	NS1	NS0	Sts	M1	M0	Selección
0	0	0	X	0	0	Encoder
0	0	1	X	0	1	?
0	1	0	X	1	0	Pipeline
0	1	1	X	1	1	Incrementer
1	0	0	0	0	0	Encoder
1	0	0	1	1	0	Pipeline
1	0	1	0	1	1	Incrementer
1	0	1	1	1	0	Pipeline
1	1	0	0	1	1	Incrementer
1	1	0	1	0	0	Encoder
1	1	1	X	0	0	-----

Inverter

Inv	In	Out
0	0	0
0	1	1
1	0	1
1	1	0

Señales de Control

Fetch Estado	S1S0	Inv	NS2-NS0	PL5-PL0
1	XX	X	011	XXXXXX
2	XX	X	011	XXXXXX
3	00	1	101	000011
4	XX	X	000	XXXXXX
ADD R3,R12,R5				
10	XX	X	010	000001
STORE R10,R24,R32				
30	XX	X	011	XXXXXX
31	XX	X	011	XXXXXX
32	XX	X	111	100000 ????