

University of Puerto Rico  
 Mayagüez Campus  
 College of Engineering  
 Department of Electrical and Computer Engineering  
 Bachelor of Science in Electrical Engineering

**Course Syllabus**

<b>1. General Information:</b>	
Alpha-numeric codification: INEL 4207 Course Title: Digital Electronics Number of credits: 3 Contact Period: 3credit hours, 3 hours of lecture per week Required in ICOM	
<b>2. Course Description:</b>	
English: Theory of Operation and Structure of Bipolar (BJT), metal Oxide semiconductor MOS logic gates; operation of semiconductor memories; Programmable Logic Arrays;(PLA);operational amplifiers; analog to digital A/Dand D/A digital to analog converters	
Spanish: Teoría de operación y estructura de compuertas lógicas diseñadas con transistores BJT y MOSFETs; operación de memorias en semiconductores, Matrices de lógica programable (PLA); Amplificadores operacionales; Convertidores de señales análoga digital A/D y digital análoga D/A.	
<b>3. Pre/Co-requisites and other requirements:</b>	
INEL4201 and INEL 4205	
<b>4. Course Objectives:</b>	
The objective of the course is to provide each student an understanding of the internal structure, operation and interfacing requirements of digital logic families, semiconductor memories and A/D and D/A converters	
<b>5. Instructional Strategies:</b>	
<input checked="" type="checkbox"/> conference <input checked="" type="checkbox"/> discussion <input type="checkbox"/> computation <input checked="" type="checkbox"/> laboratory  <input type="checkbox"/> seminar with formal presentation <input type="checkbox"/> seminar without formal presentation <input type="checkbox"/> workshop  <input type="checkbox"/> art workshop <input type="checkbox"/> practice <input type="checkbox"/> trip <input type="checkbox"/> thesis <input type="checkbox"/> special problems <input type="checkbox"/> tutoring  <input type="checkbox"/> research <input type="checkbox"/> other, please specify:	
<b>6. Minimum or Required Resources Available:</b>	
<b>7. Course time frame and thematic outline</b>	
<b>Outline</b>	<b>Contact Hours</b>
Introduction	1
BJT fundamentals	3
Basic Bipolar gates	6
MOS fundamentals	3
Fabrication and layout of MOS circuits	3
NMOS, CMOS and BiCMOS gates	6
Interface logic	3
Regenerative Circuits	4
Operational Amplifiers	3
Sampling and quantization of analog signals	3
A/D and D/A convertes	4
Semiconductor memories	4
Exams	2
<b>Total hours: (equivalent to contact period)</b>	<b>45</b>
<b>8. Grading System</b>	
<input checked="" type="checkbox"/> Quantifiable (letters) <input type="checkbox"/> Not Quantifiable	

**9. Evaluation Strategies** (Suggested): The faculty member teaching the course will provide the student with the evaluation strategy he/she will be using throughout the semester. This will be done within the first week of classes.

	Quantity	Percent
<input checked="" type="checkbox"/> Exams	2	50%
<input type="checkbox"/> Final Exam		
<input type="checkbox"/> Short Quizzes		
<input checked="" type="checkbox"/> Oral Reports	1	25%
<input type="checkbox"/> Monographies		
<input type="checkbox"/> Portfolio		
<input checked="" type="checkbox"/> Projects	1	25%
<input type="checkbox"/> Journals		
<input type="checkbox"/> Other, specify:		
<b>TOTAL:</b>		<b>100%</b>

**10. Bibliography:**

Neamen, Donald A. Microelectronics Circuit Analysis and Design, 2007, McGraw Hill.

**11. According to Law 51**

Students will identify themselves with the Institution and the instructor of the course for purposes of assessment (exams) accommodations. For more information please call the Student with Disabilities Office which is part of the Dean of Students office (Chemistry Building, room 019) at (787)265-3862 or (787)832-4040 extensions 3250 or 3258.

**12. Contribution of Course to meeting the requirements of Criterion 5:**

Math	Basic Science	General	Engineering Topic
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**13. Course Outcomes**

**Map to Program Outcomes**

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|--|-----|
| 1. Be able to determine the standard or criteria against which the outcome of the design process will be measured or compared.               | (a) |
| 2.   |     |
| 3. Be able to follow logical and orderly design procedures, choosing the best solution for a given set of criteriarization of logic families | (b) |
| 4. Analysis and characterization of logic families   | (c) |
| 5. Analysis and characterization of logic families   | (e) |

Person(s) who prepared this description and date of preparation: Gladys O. Ducoudray. Submitted by Gladys O. Ducoudray Nov 2006