University of Puerto Rico
Mayagüez Campus
College of Engineering
Department of Electrical and Computer Engineering
Bachellor of Science in Electrical Engineering

Course Syllabus

1. General Information:

Alpha-numeric codification: INEL 4218
Course Title: Introduction to VLSI Design
Number of credits: 3
Contact Period: 3credit hours, 3 hours of lecture per week
Elective in INEL and ICOM

2. Course Description:

English: Study of transistor properties and design methodologies for digital and analog circuits

Spanish: Estudio de las propiedades y diseño de los transistores para circuitos digitales y análogos.

3. Pre/Co-requisites and other requirements:

INEL4201

4. Course Objectives:

This course seeks to develop basic tools and understanding of VLSI design at transistor level. It includes process for designing layout and simulations of components for a system using Cadence Tools.

5. Instructional Strategies:

☒conference ☒discussion ☐computation ☐laboratory

☐seminar with formal presentation ☐seminar without formal presentation ☐workshop

☐art workshop ☐practice ☐trip ☐thesis ☐special problems ☐tutoring

☐research ☒other, please specify: Problem with design comoponents. Open ended solution

6. Minimum or Required Resources Available:

7. Course time frame and thematic outline

Outline	Contact Hours
I Introduction to CMOS Circuits.	5
MOS Transistor Theory. Introduction. MOS Device Design Equation. The Complemenatry CMOS Inverter-DC Characteristics. Alternate CMOS Inverters. The Differential Stage. The Transmission Gate. Bipolar Devices.	10
CMOS Processing Technology.	3

Silicon Semiconductor Technology: An Overview. CMOS Technologies. Layout Design Rules. CAD Issues.	
Circuit Characterization and Performance Estimation. Introduction. Resistance Estimation. Capacitance Estimation. Inductance. Switching Characteristics. CMOS Gate Transistor Sizing. Power Consumption. Determination of Conductor Size. Charge Sharing. Design Margining. Yield. Scaling of MOS Transistor Dimensions.	10
CMOS Circuit and Logic Design. Introduction. CMOS Logic Structures. Basic Physical Design of Simple Logic Gates. Clocking Strategies. Physical and Electrical Design of Logic Gates. 10 Structures.	6
Structured Design Strategies. Introduction. Design Economics. Design Strategies. Design Methods. CMOS Chip Design Options. Design Capture Tools. Design Verification Tools.	6
CMOS TestMethodolgies. Introduction. Fault Models. Design for Testability. Automatic Test Pattern Generation. Design for Manufacturability.	10
Total hours: (equivalent to contact period)	48

8. Grading System

☒Quantifiable (letters) ☐ Not Quantifiable

9. Evaluation Strategies (Suggested): The faculty member teaching the course will provide the student with the evaluation strategy he/she will be using throughout the semester. This will be done within the first week of

classes.

	Quantity	Percent
☒ **Exams**	**3**	**50%**
☒ **Final Exam**	**1**	**25%**
☐ **Short Quizzes**		
☐ **Oral Reports**		
☐ **Monographies**		
☐ **Portfolio**		
☐ **Projects**		
☐ **Journals**		
☒ **Other, specify: Final project**		**25%**
TOTAL:		**100%**

10. Bibliography:

1. Principles of CMOS VLSI Design a Systems perspective with verilog /vhdl manual, West Nell H. E./ Eshraghian, Kamran Smith, Michael John Sebastian 2002, Pearson/Higher Education.
2. Design of Analogs CMOS Integrated Circuits, Mc Graw Hill (2000), Razabi, B.
3. Principles of CMOS VLSI Design: A system perspective, Second Edition N. Weste and Kamram Eshraghian
4. Design of Analog CMOS Integrated Circuits, Author: Behzad Razavi, House: McGraw-Hill (Electrical Engineering Series).

11. According to Law 51

Students will identify themselves with the Institution and the instructor of the course for purposes of assessment (exams) accommodations. For more information please call the Student with Disabilities Office which is part of the Dean of Students office (Chemistry Building, room 019) at (787)265-3862 or (787)832-4040 extensions 3250 or 3258.

12. Contribution of Course to meeting the requirements of Criterion 5:

Math	Basic Science	General	Engineering Topic
			√

13. Course Outcomes

	Map to Program Outcomes
-Be able to determine the standard or criteria against which the outcome of the design process will be measured or compared.	(a)
-Be able to follow logical and orderly design procedures, choosing the best solution for a given set of criteria	(b)
-Analysis and characterization of simple logic families	(c)
-Analysis and characterization of single stage amplifiers using cadence tools	(e, k)
-Communicate effectively their project	(g)

Person(s) who prepared this description and date of preparation: (Electronics Committee). Submitted by: Gladys O. Ducoudray, May 2007