## University of Puerto Rico – Mayagüez School of Engineering

## **INEL 4206 – Microprocessors**

Problem Set 1 Due: Thursday September 5, 2002

1. Design a combinational logic circuit that complies with the following specifications:

Input					Output			
I <sub>0</sub>	I <sub>1</sub>	$I_2$	I <sub>3</sub>		$O_0$	$O_1$	$O_2$	O <sub>3</sub>
0	0	0	0		0	0	0	1
0	0	0	1		0	0	1	0
0	0	1	0		0	0	1	1
0	0	1	1		0	1	0	0
0	1	0	0		0	1	0	1
0	1	0	1		1	1	0	0
1	1	0	0		1	0	1	1
1	0	1	1		1	0	1	0
1	0	1	0		0	0	0	1

(This is a  $0 \ll 1$  then  $1 \ll 5$ ,  $5 \ll 1$  loop)

a) Provide a Karnaugh Map (K-Map) and Boolean equation for each of the outputs  $(O_n)$ .

b) Make the design in Logic Works, use a "Hex Keyboard wo/STB" as input, with the pins arranged as follows: display the output of the circuit.  $\boxed{123}_{4567} = 10^{-10}_{-11}$ 

	1	2	3	-10
4	5	6	7	—l1
8	9	А	В	—l2
С	D	Е	F	—I3

- 2. Design a combinational circuit that works as a decoder, it will receive the binary equivalents for 1 through 5, and set high the output corresponding to that number. (*The circuit must have exactly 5 outputs; you may NOT use the available decoders in Logic Works*)
  - a) Provide the schematics for the decoder.
  - b) Make a new device symbol and package the circuit you designed above, so that it can be used as an "IC". It should look something like this:



3. Design a five LED scanner (sequence of LED's that light up from side to side in a loop). Use the two circuits you have designed in problems 1 and 2 as part of the sequential circuit that will make up the scanner.

Problem Set Submission:

Your solution will consist of four (4) Logic Works files.

- 1) Solution for problem 1
- 2) Solution for problem 2
- 3) Library file with the packaged IC from problem 2
- 4) Solution for problem 3

Send these 4 files in an e-mail attachment to: inel4205-submit@ece.uprm.edu The subject of the e-mail should be PS1:<<*student #>>* 

K-maps and Boolean Equations from problem 1a will be handed in to the professor on Sept 5.

Correction criterias:

Criteria	Weight(%)
Correctness	60%
Design	20%
Efficiency	10%
Style	10%

Remember the policy on late submission stated on the "Course Information Sheet".