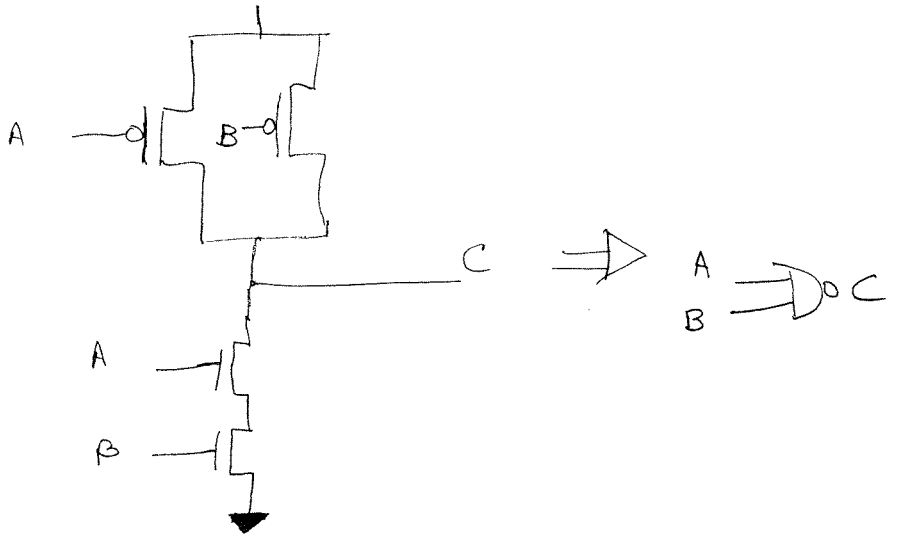
NAND

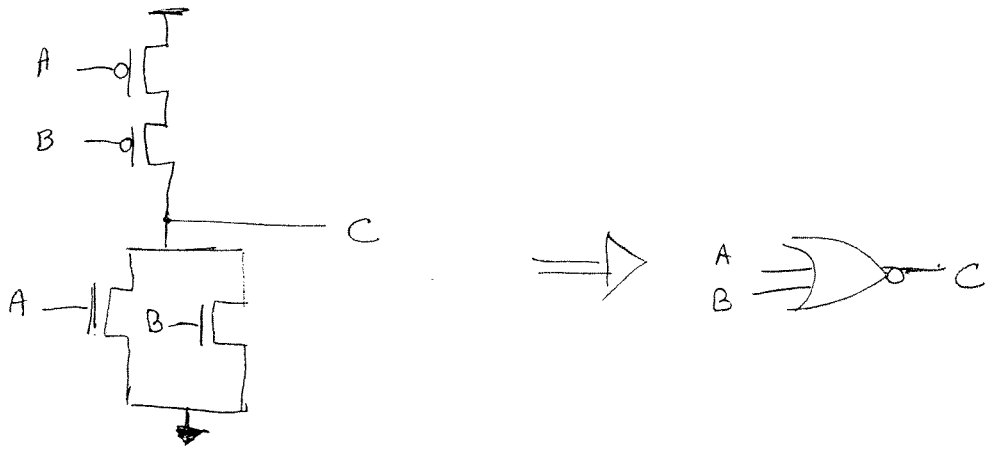
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0



UNIVERSAL

NOR

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0



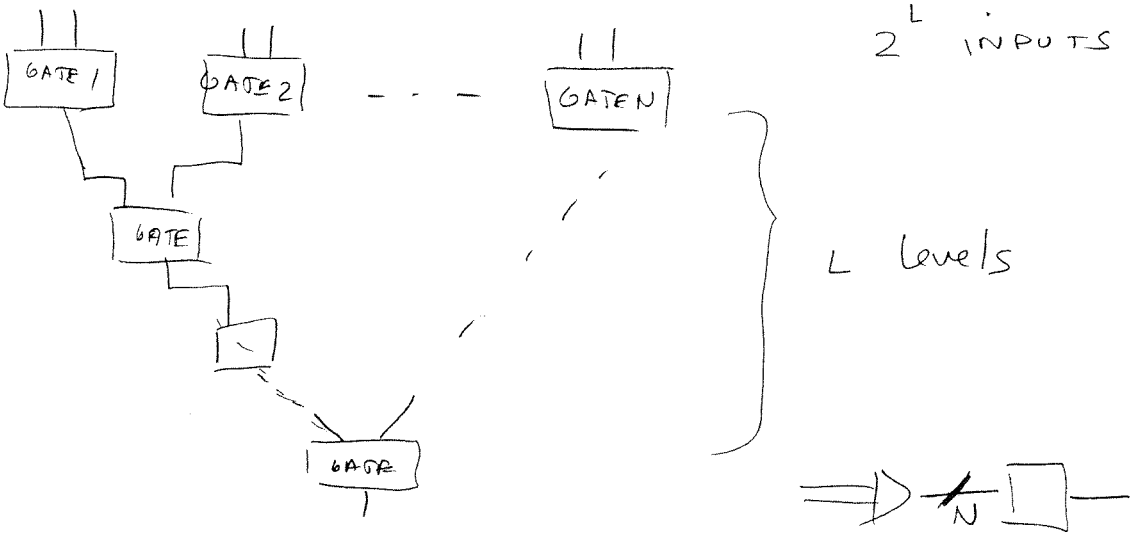
UNIVERSAL

INVERTER WITH NAND'S

A	B
0	1
1	0

AND

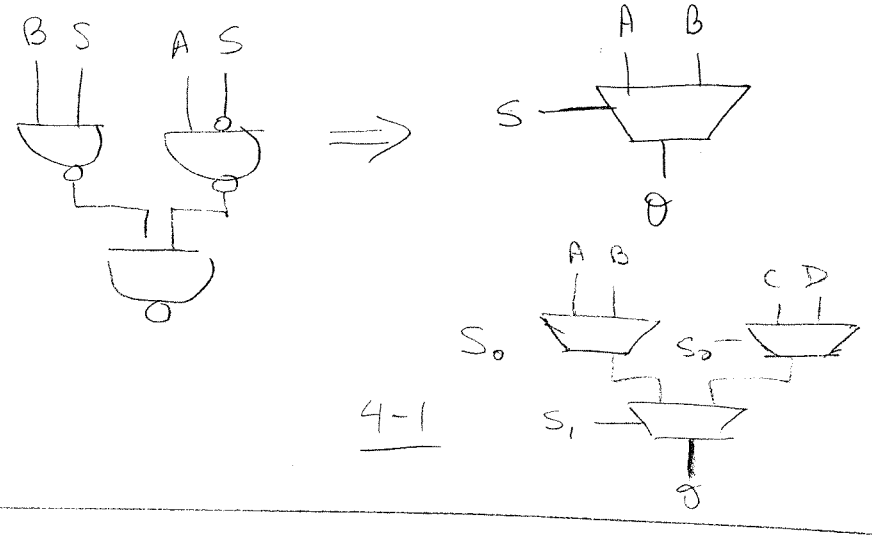
N - INPUT NAND - NOR



---

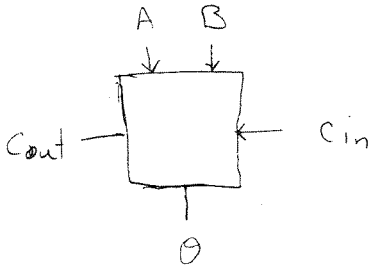
2 — 1 MUX.

A	B	Sel	ϑ
0	x	0	0
1	x	0	1
x	0	1	0
x	1	1	1

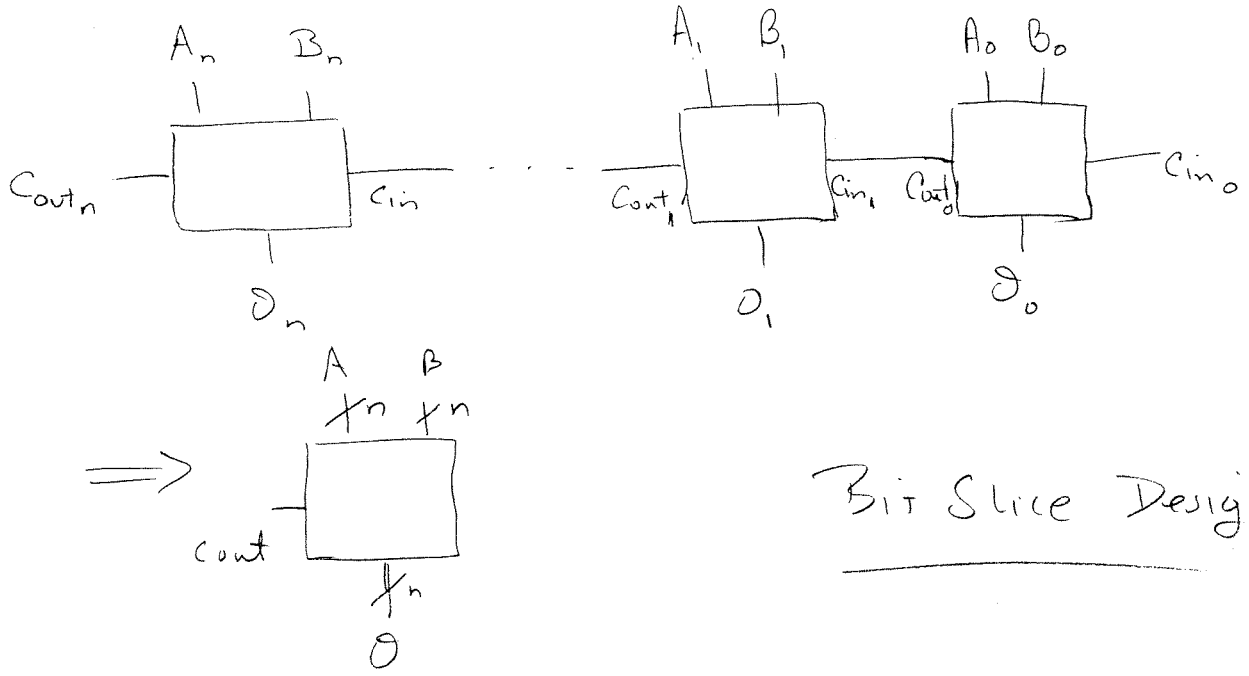


ADDER (1 bit)

A	B	Cin	ϑ	Cout
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1



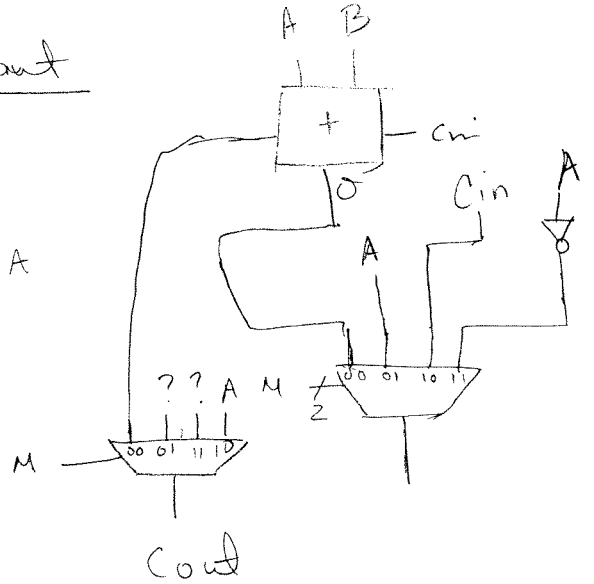
ADDER (N BIT)

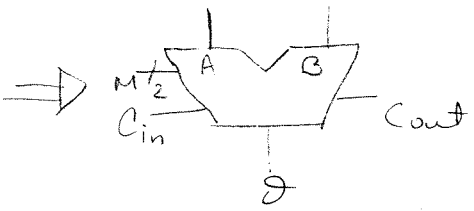


Bit Slice Design

ALU (1 bit)

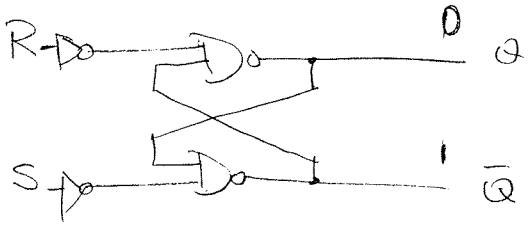
M_1M_0	A	B	C	Cout
0 0			A+B+Cin	
0 1			A	
1 1			$\overline{A}$	
1 0			Cin	A



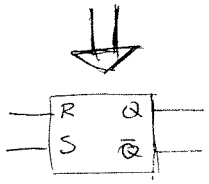


Memory and Sequential Circuits

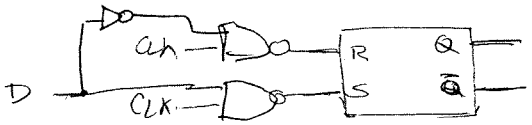
R-S latch

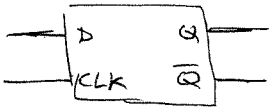


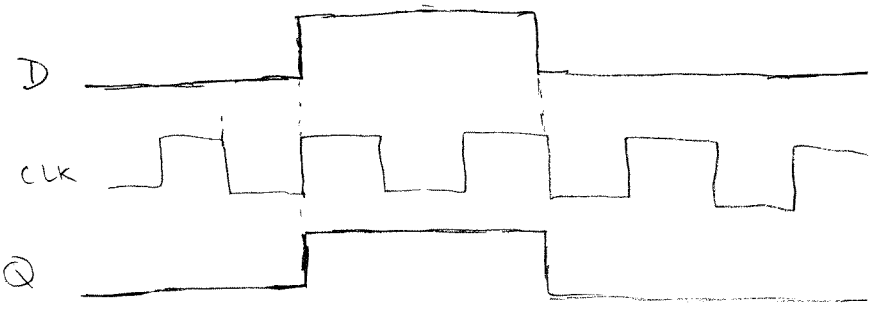
R	S	Q_t	Q_{t+1}
0	0	X	INVALID
1	1	0	0
1	1	1	1
0	1	X	1
1	0	X	0



D Flip-Flop

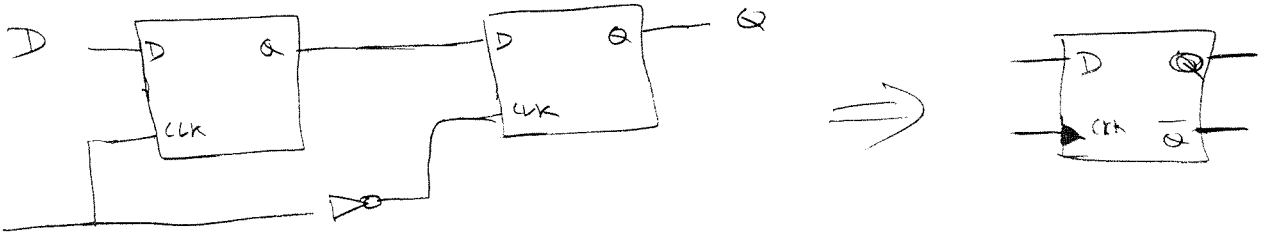




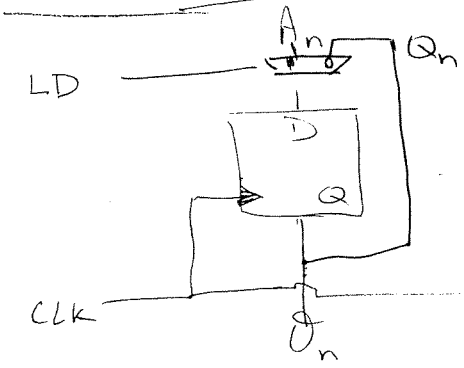


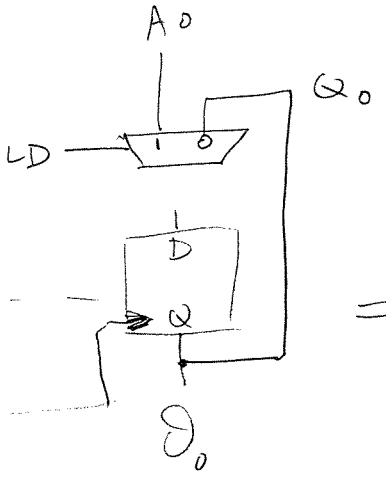
Master-Slave D-Flip Flop. (Edge-triggered)

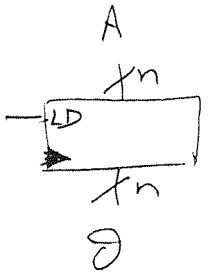
Race Condition



Register N-BIT



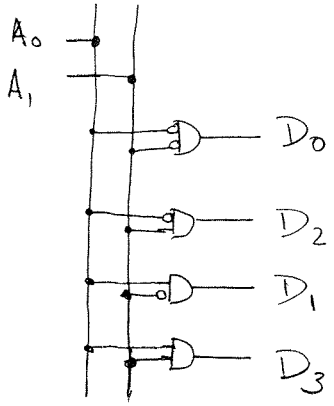




---

2 - 4 Decoder

A_1	A_0	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	1	0	0	0	1
1	0	0	0	1	0



---

4 x 8 Memory