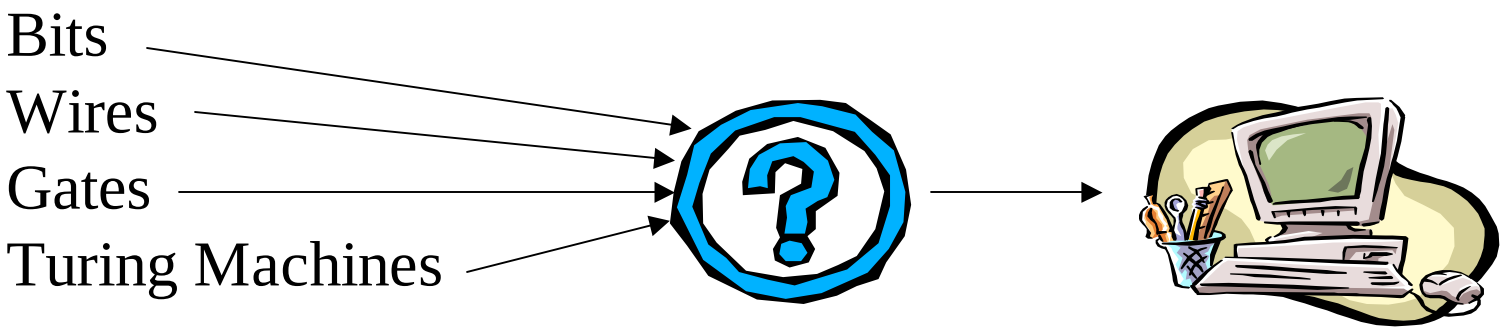
Practical Universal Computers



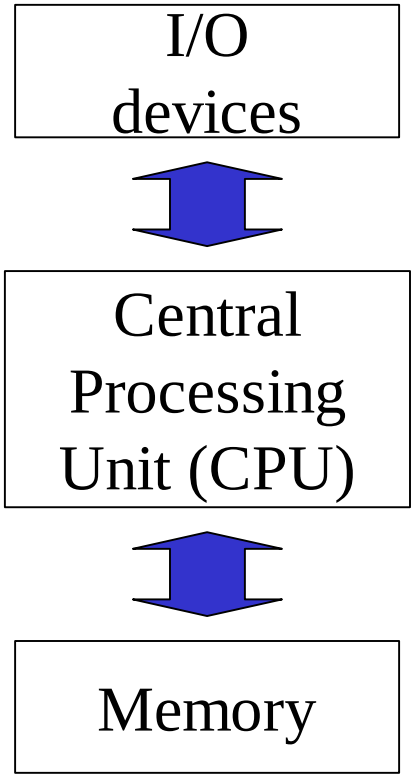
Lecture 4

Prof. Bienvenido Velez

Outline

- The von Neumann Architecture
  - Big Idea: Interpretation
  - Stored program concept
- Designing a simple processor
  - Instruction Set Architecture
  - Data Paths
  - Control Unit

The (John) Von Neumann Architecture
(late 40 s)



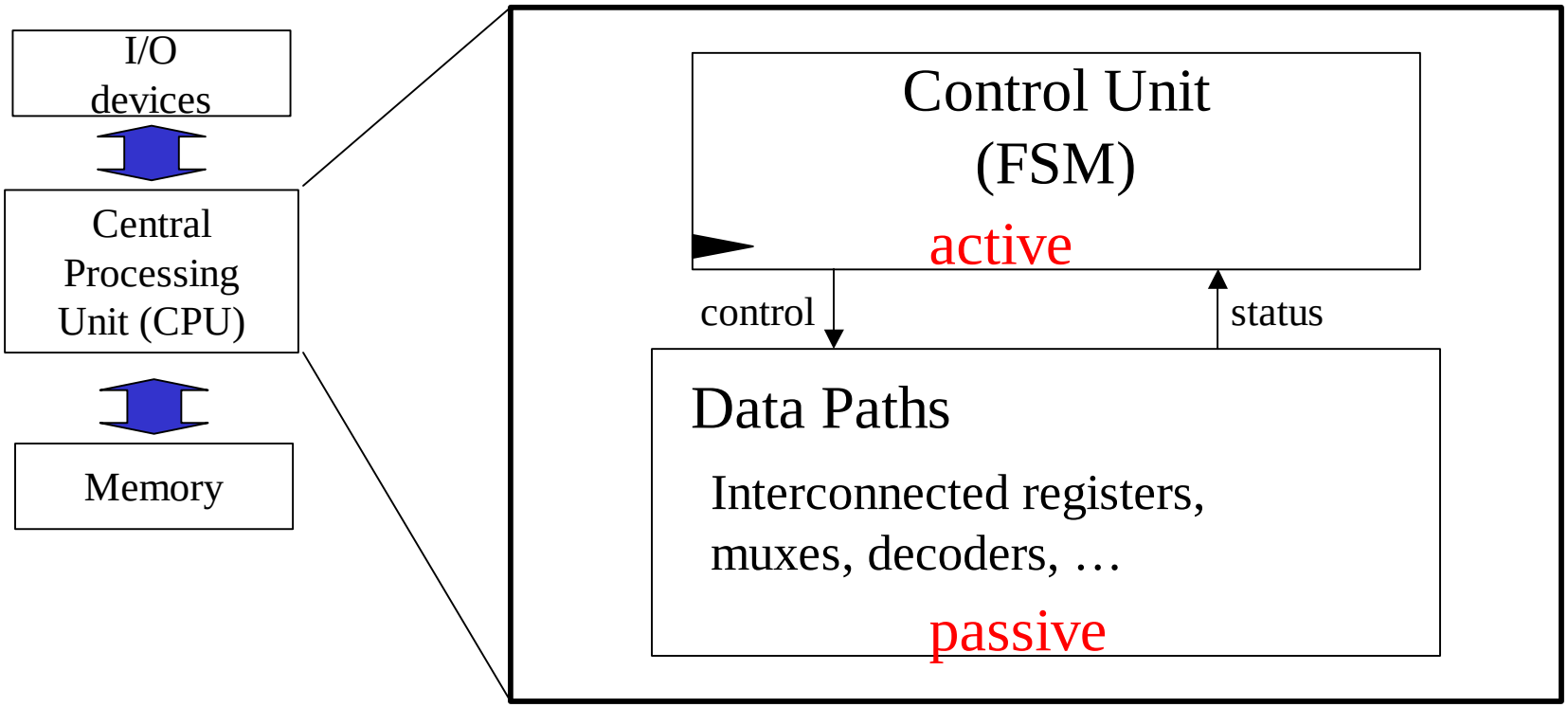
Allow communication with outside world

Interprets instructions

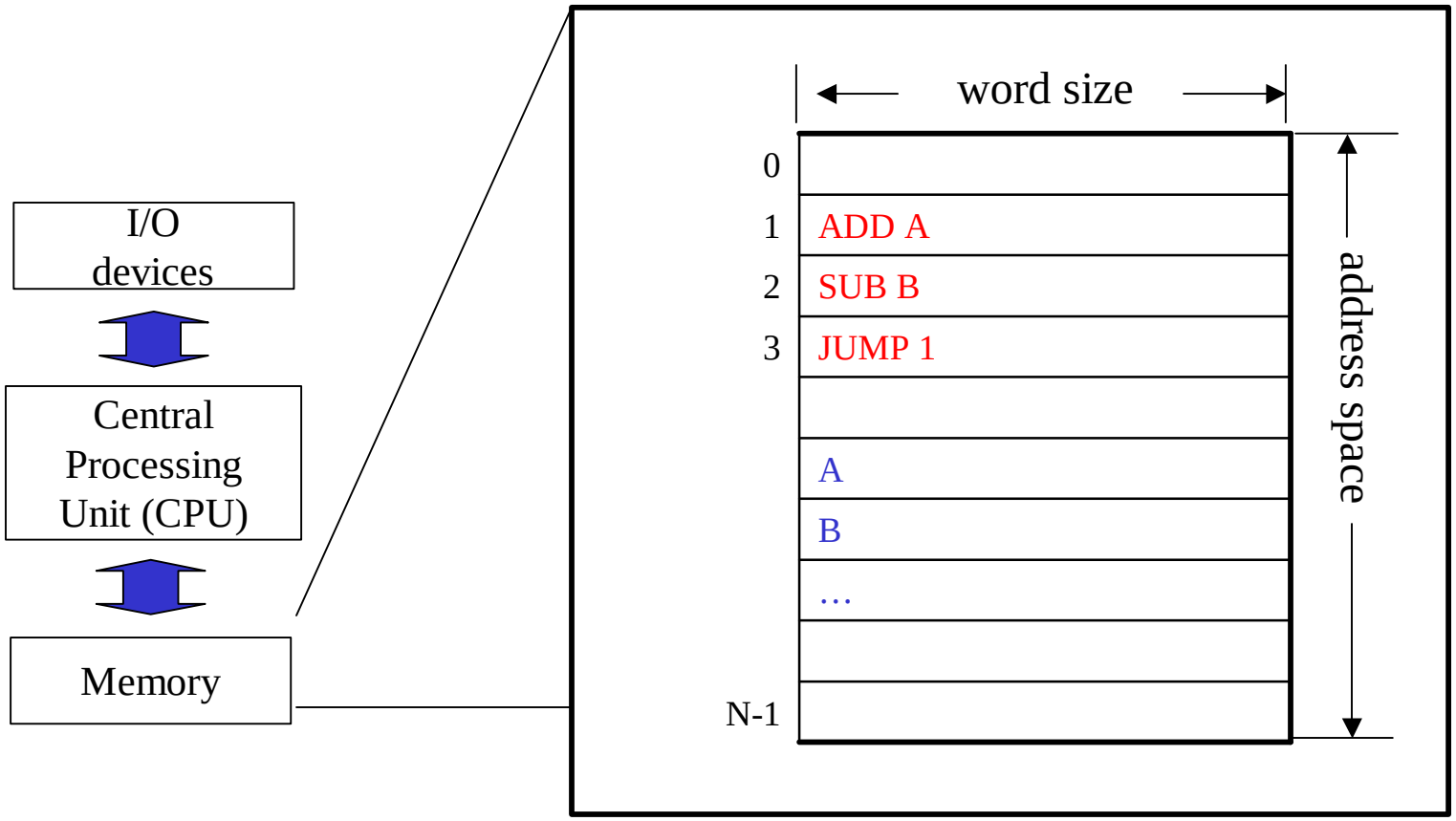
Stores both programs and data

After 60 years … most processors still look like this!

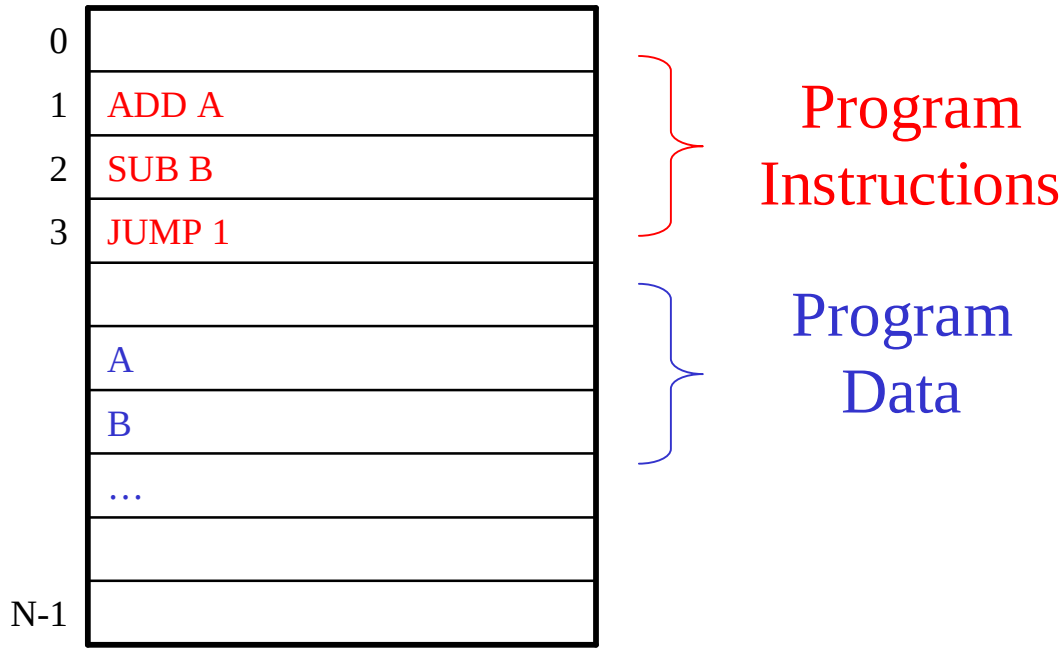
The von Neumann Architecture
Central Processing (CPU)



The (John) Von Neuman Architecture
The Memory Unit



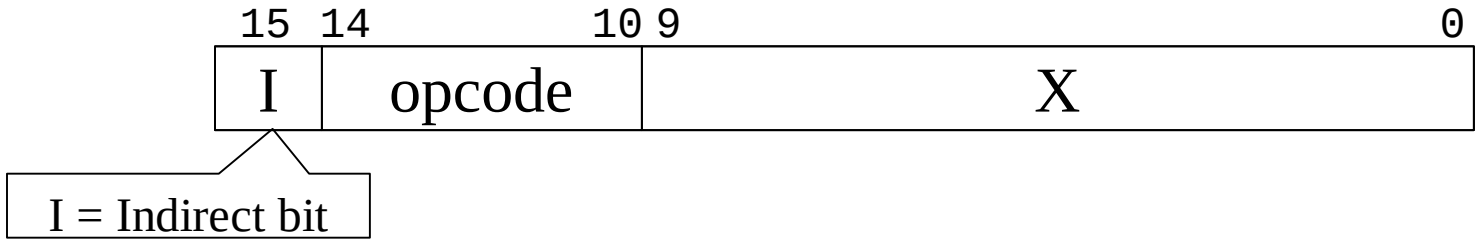
The (John) Von Neuman Architecture
Stored Program Concept



- Programs and their data coexist in memory
- Processor, under program control, keeps track of what needs to be interpreted as instructions and what as data.

Easy I
A Simple Accumulator Processor
Instruction Set Architecture (ISA)

Instruction Format (16 bits)



Easy I
A Simple Accumulator Processor
Instruction Set Architecture (ISA)

Instruction Set

Name	Opcode	Action I=0	Action I=1
Comp	00 000	AC ? not AC	AC <- not AC
ShR	00 001	AC ? AC / 2	AC ? AC / 2
BrN	00 010	AC < 0 ? PC ? X	AC < 0 ? PC ? MEM[X]
Jump	00 011	PC ? X	PC ? MEM[X]
Store	00 100	MEM[X] ? AC	MEM[MEM[X]] ? AC
Load	00 101	AC ? MEM[X]	AC ? MEM[MEM[X]]
And	00 110	AC ? AC and X	AC ? AC and MEM[X]
Add	00 111	AC ? AC + X	AC ? AC + MEM[X]

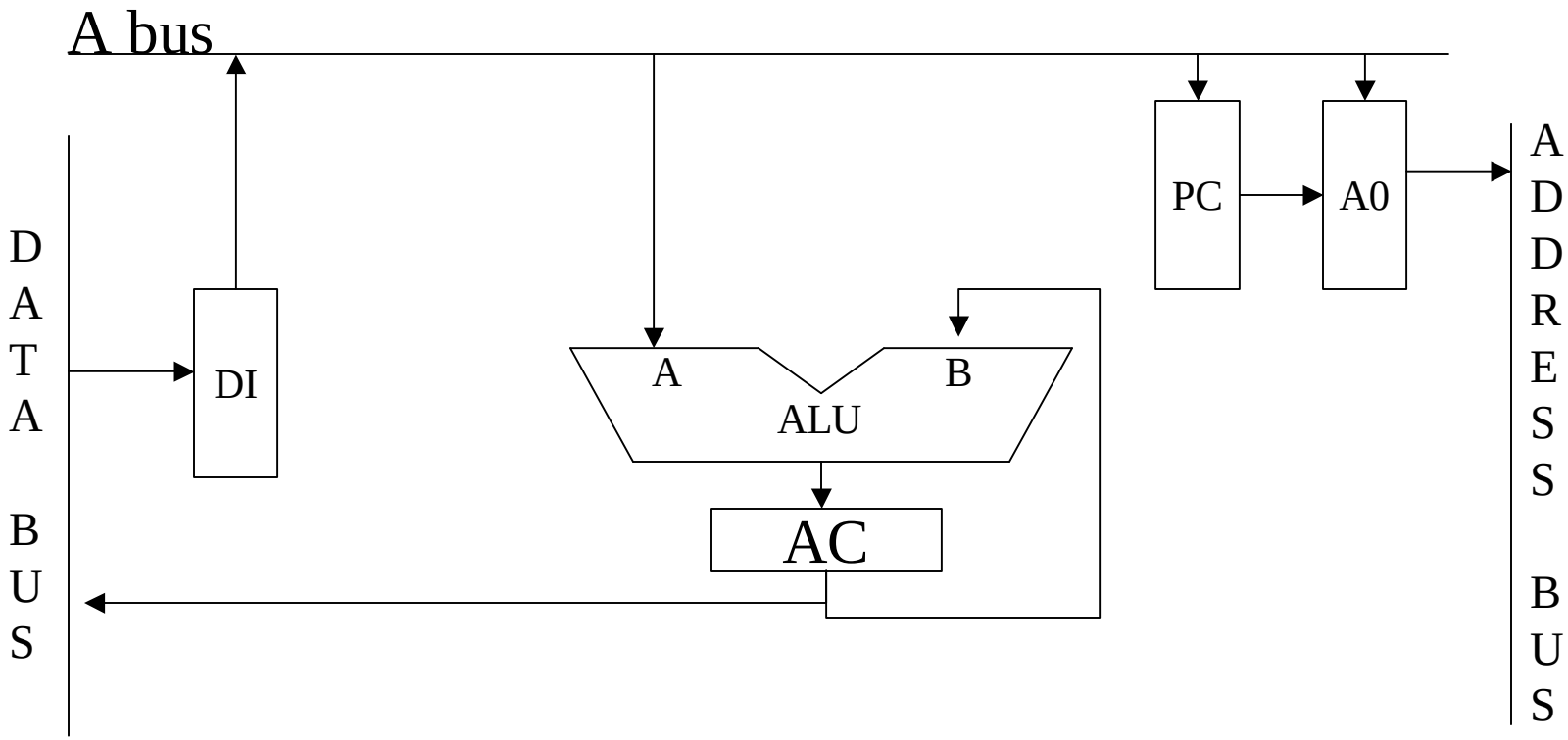
Easy all right … but universal it is!

Easy I
A Simple Accumulator Processor
Instruction Set Architecture (ISA)

Some Immediate Observations on the Easy I ISA

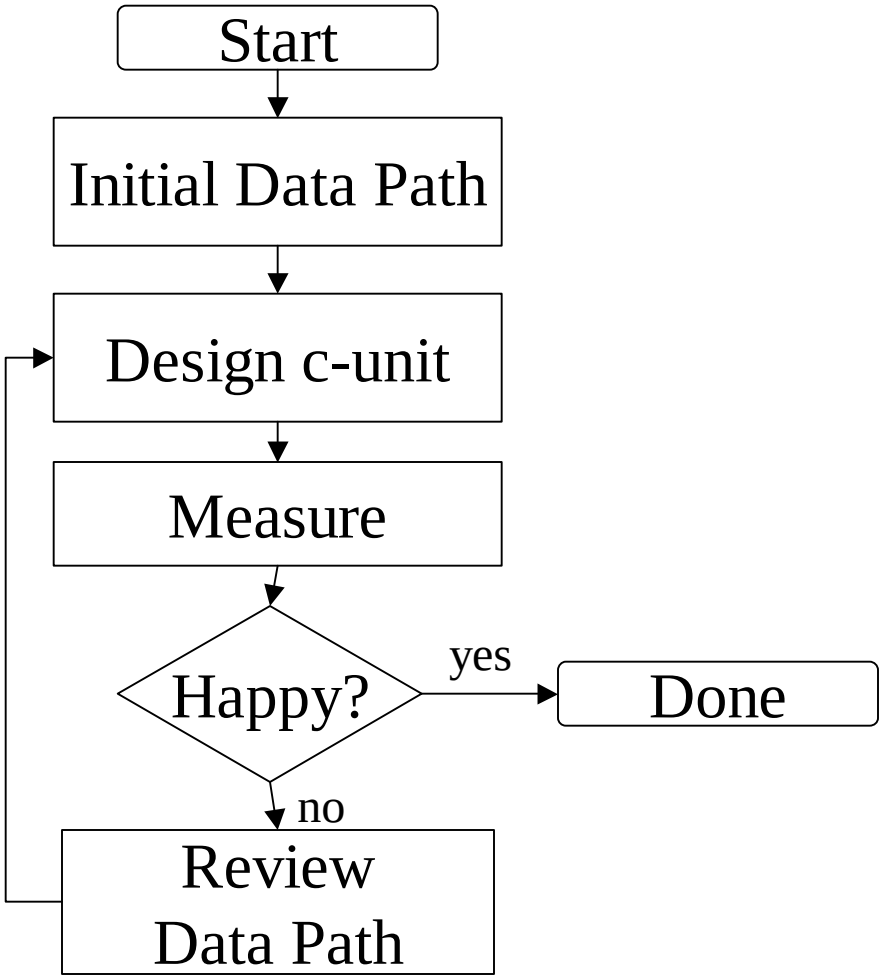
- Accumulator (AC) is implicit operand to many instructions. No need to use instruction bits to specify one of the operands. More bits left for address and opcodes.
- Although simple, Easy I is universal. (given enough memory). Can you see this?
- Immediate bit specifies level of indirection for the location of the operand. I = 1: operand in X field (immediate). I=1 operand in memory location X (indirect).

Easy I
Data Paths

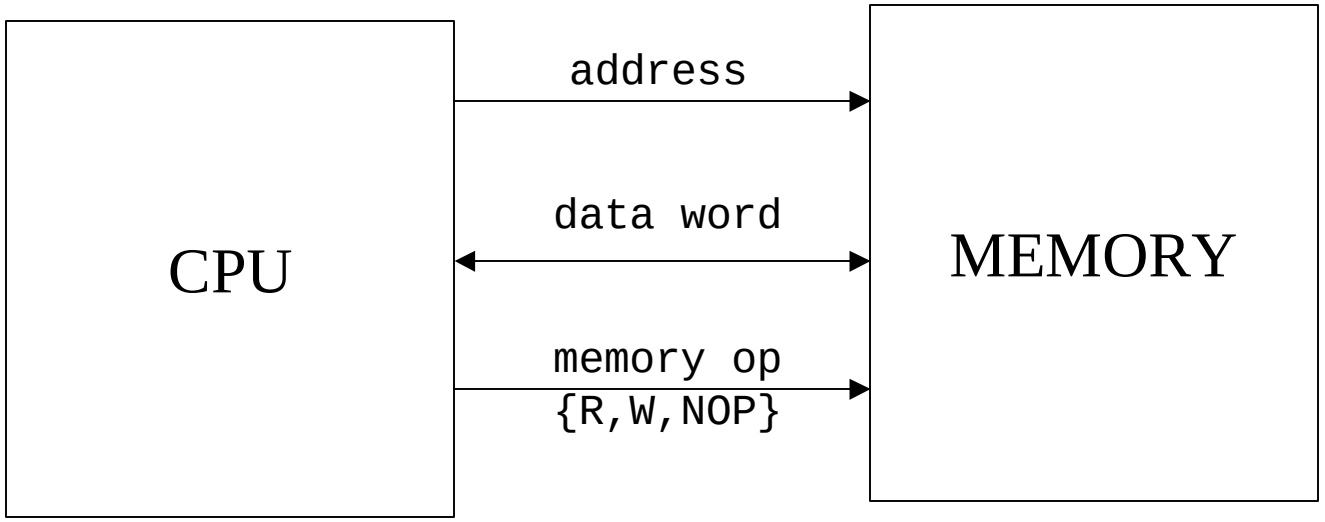


Typically, designing a processor is an iterative (aka trial end error) process

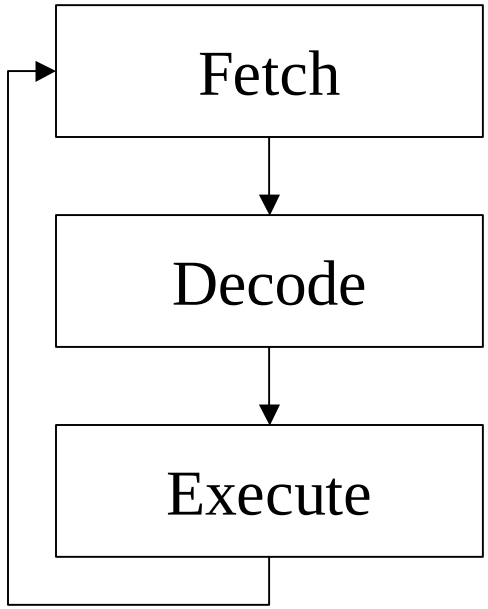
Processor Design Process



Easy I
Memory Interface



Easy I
Control Unit
(Level 0 Flowcharts)



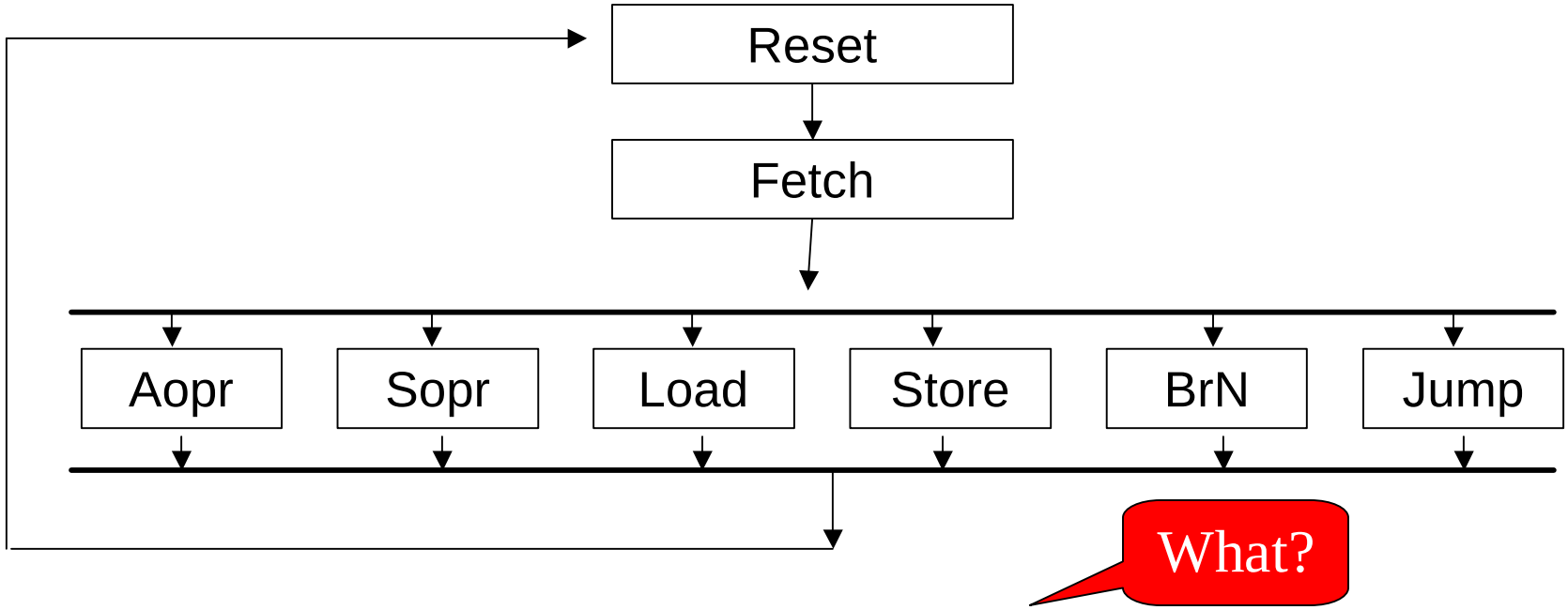
Read next instruction

Determine what it does and prepare to do it. Fetch operands.

Do it!

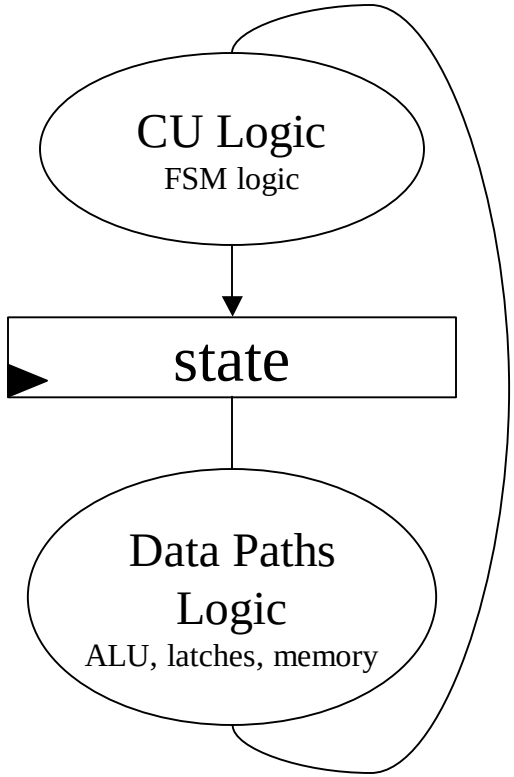
We will ignore indirect bit (assuming I = 0) for now

Easy I
Control Unit
(Level 1 Flowcharts)



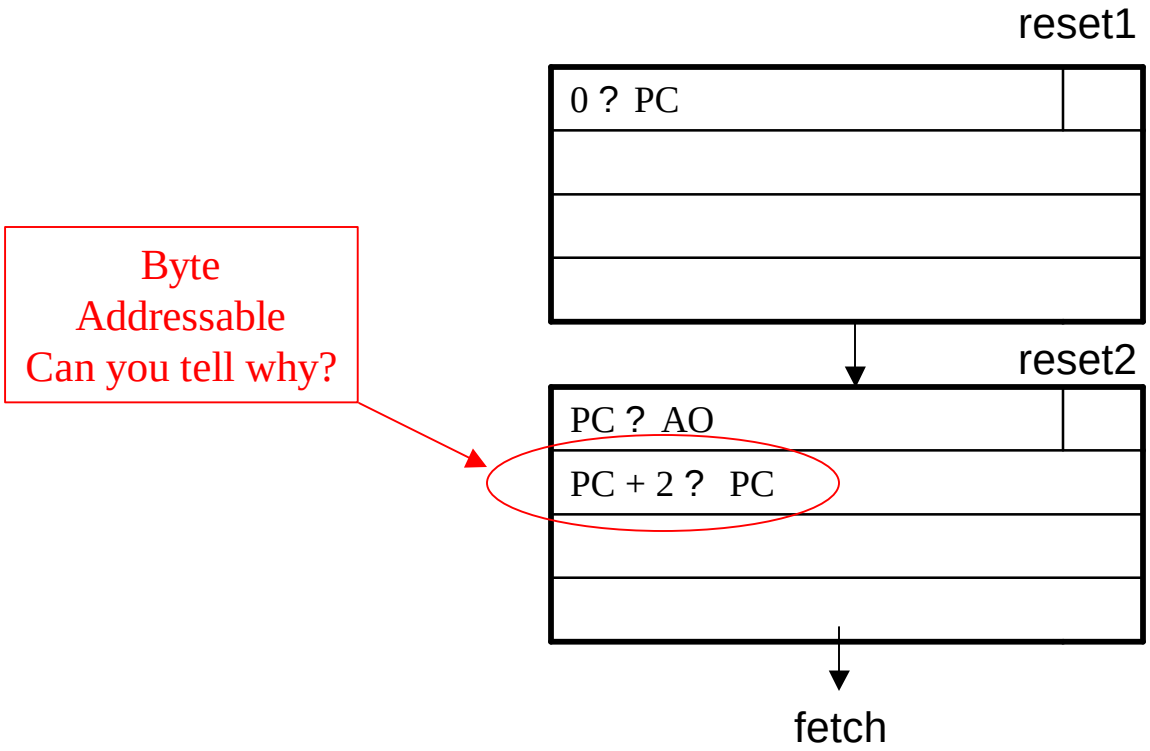
Level 1: Each box may take several CPU cycles to execute

What makes a CPU cycle?



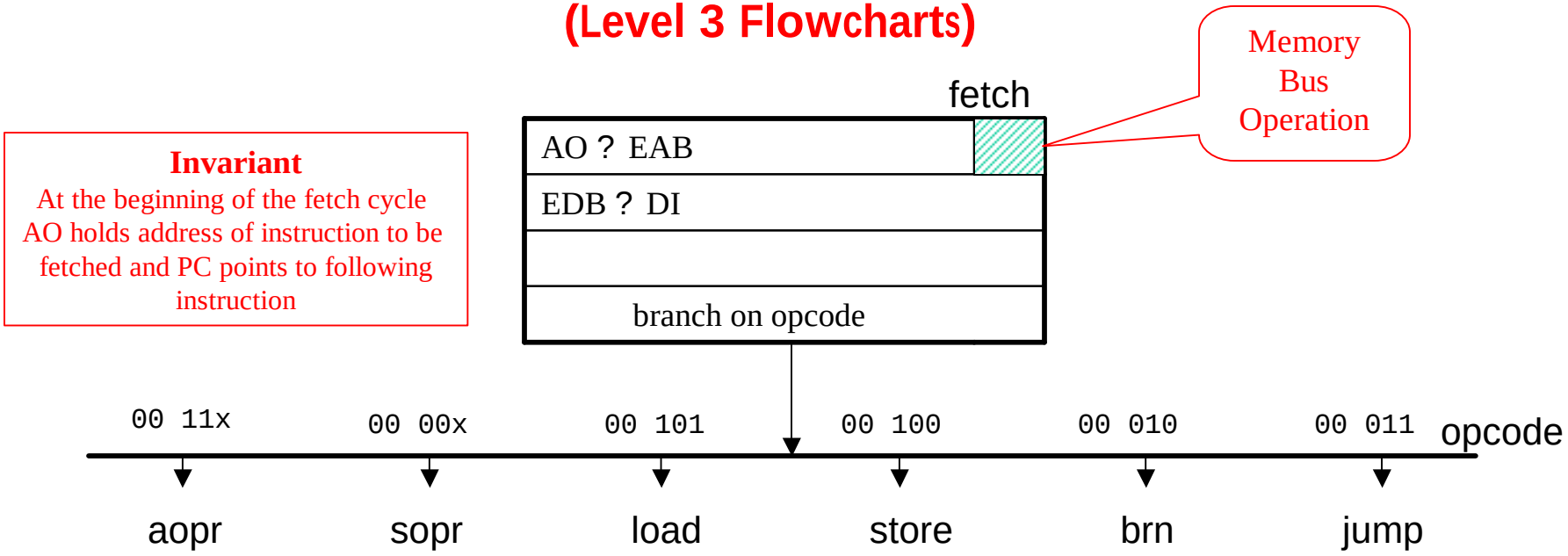
Cycle time must accommodate signal propagation

Easy I
Control Unit
(Level 2 Flowcharts)



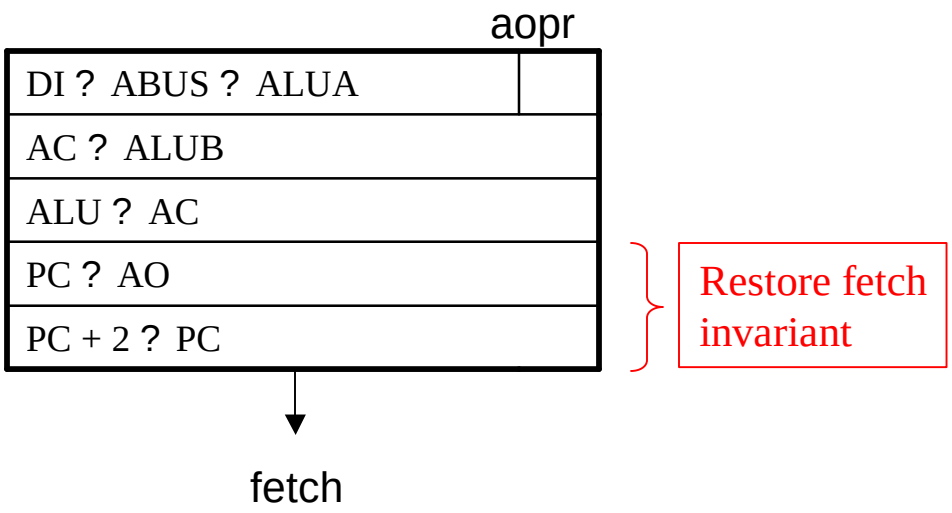
Each box may take only one CPU cycle to execute

Easy I
Control Unit
(Level 3 Flowcharts)

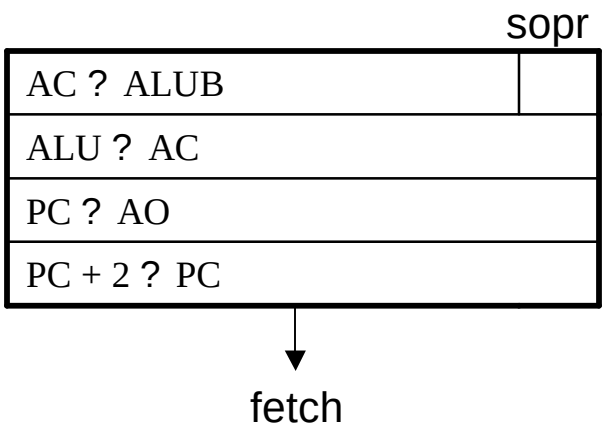


Opcode must be an input to CU's sequential circuit

Easy I
Control Unit
(Level 2 Flowcharts)

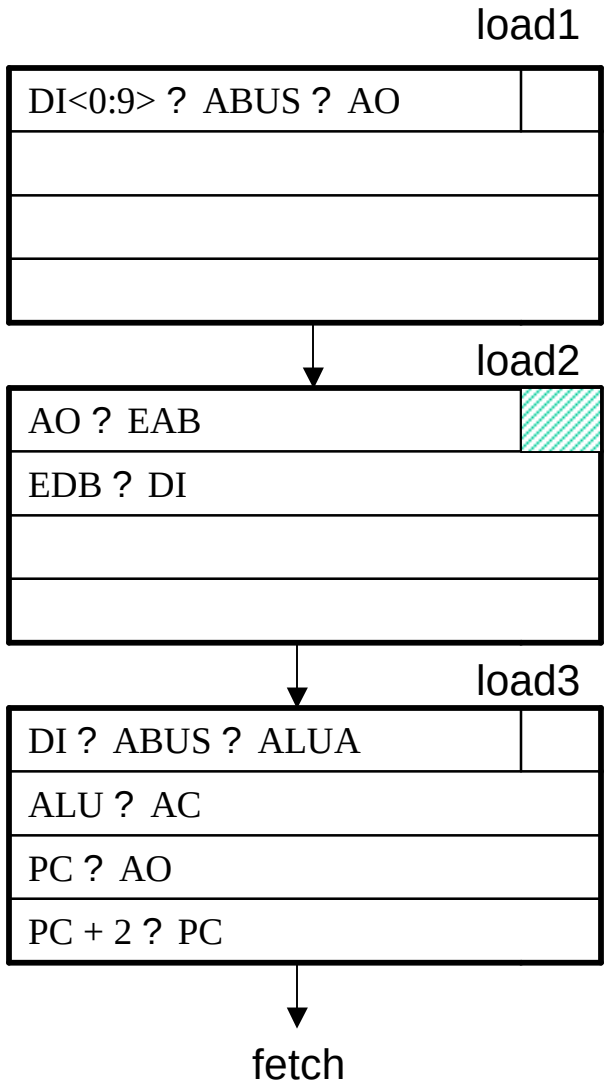


Easy I
Control Unit
(Level 2 Flowcharts)

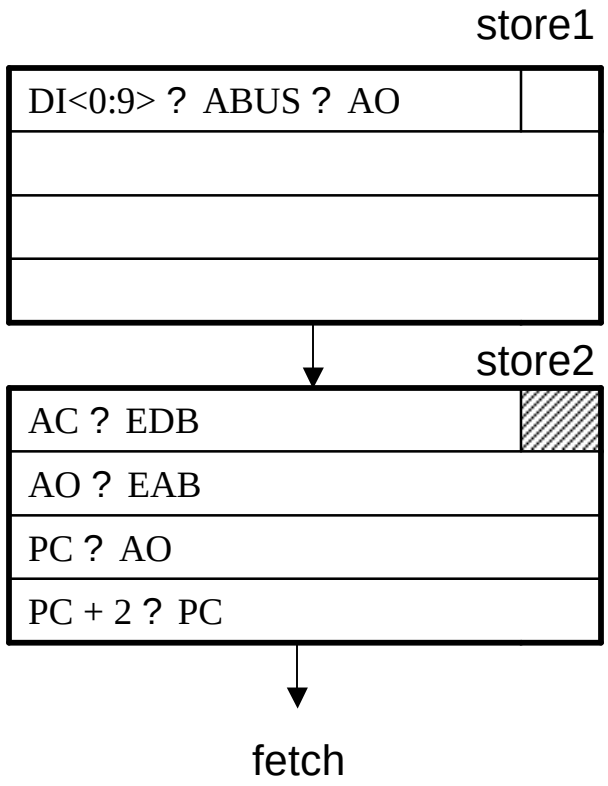


Easy I
Control Unit
(Level 2 Flowcharts)

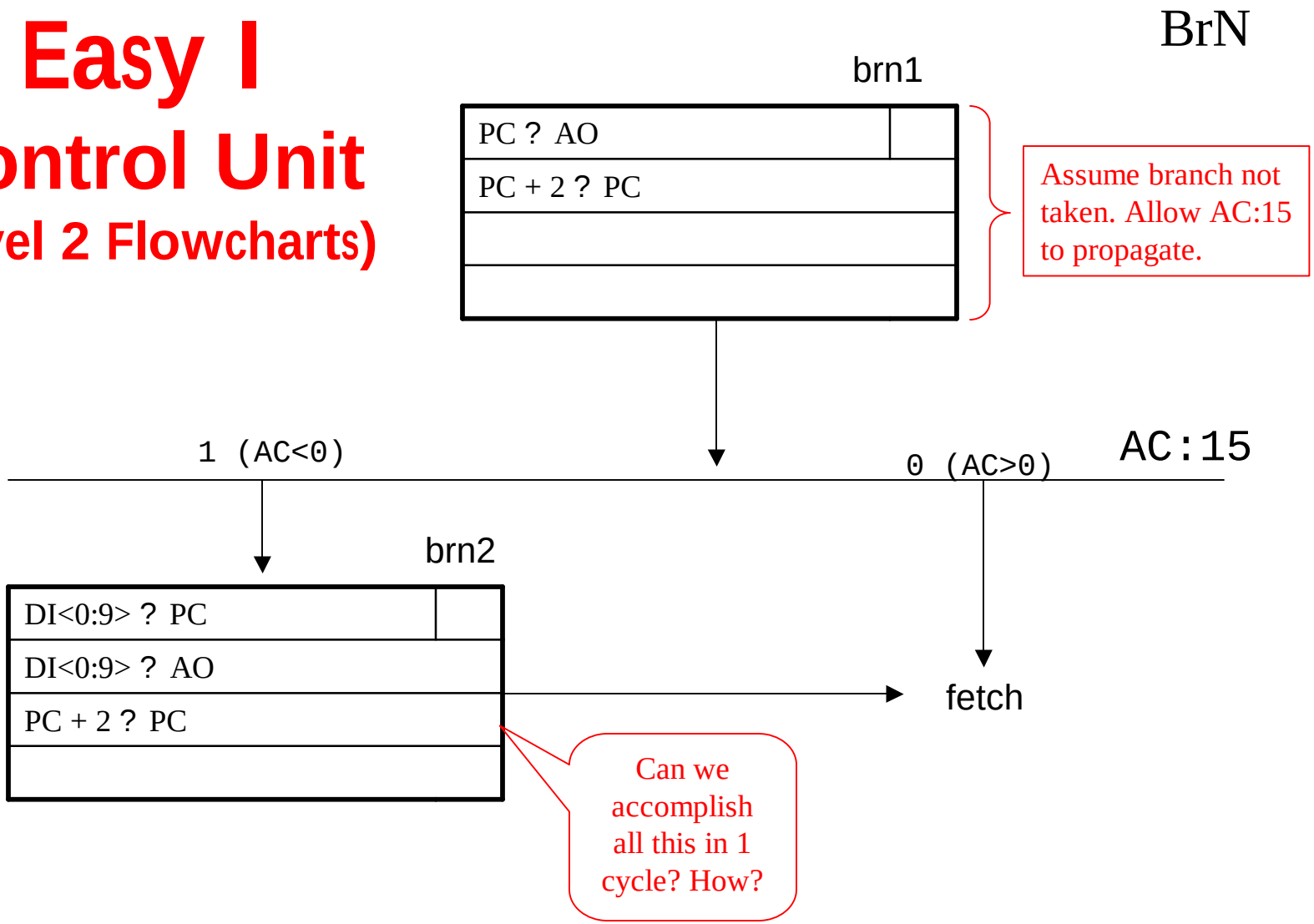
Load



Easy I
Control Unit
(Level 2 Flowcharts)

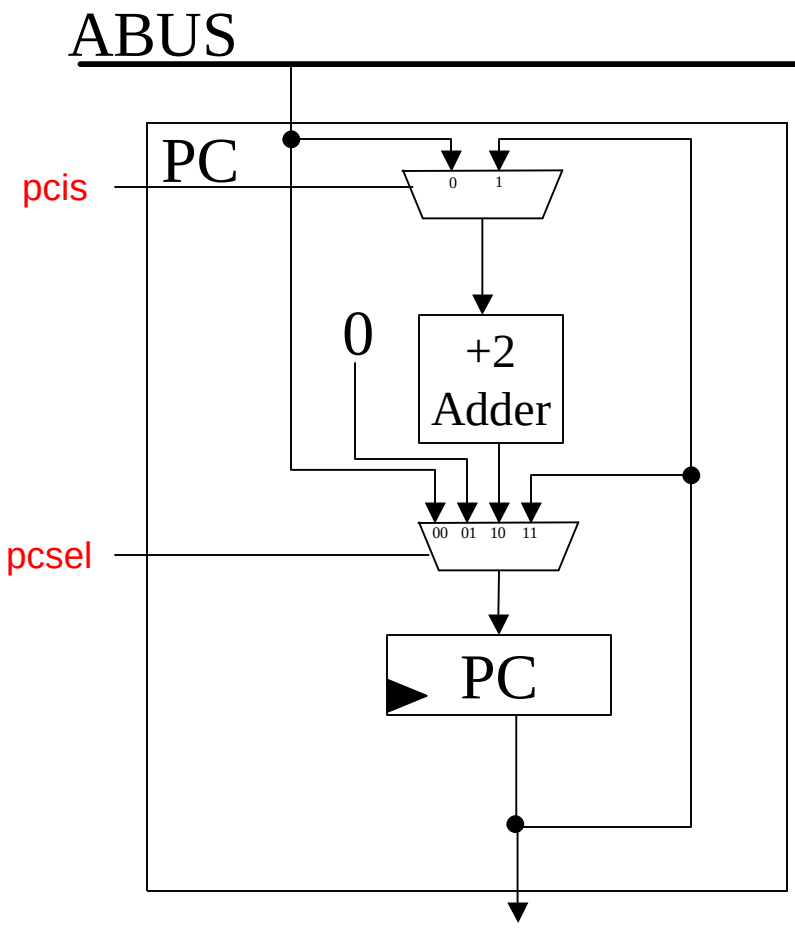


Easy I
Control Unit
(Level 2 Flowcharts)



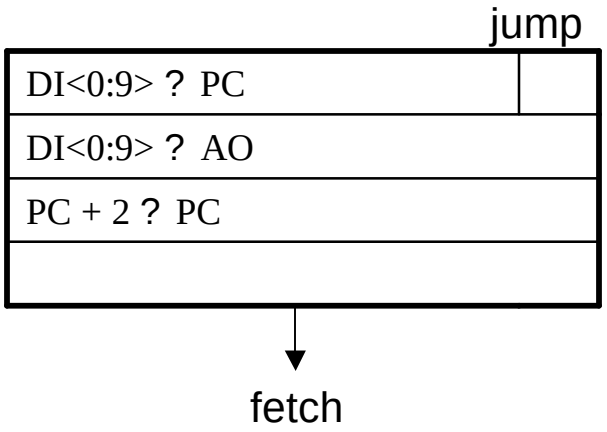
Bit 15 of AC input to the CU's sequential circuit

Inside the Easy-I PC

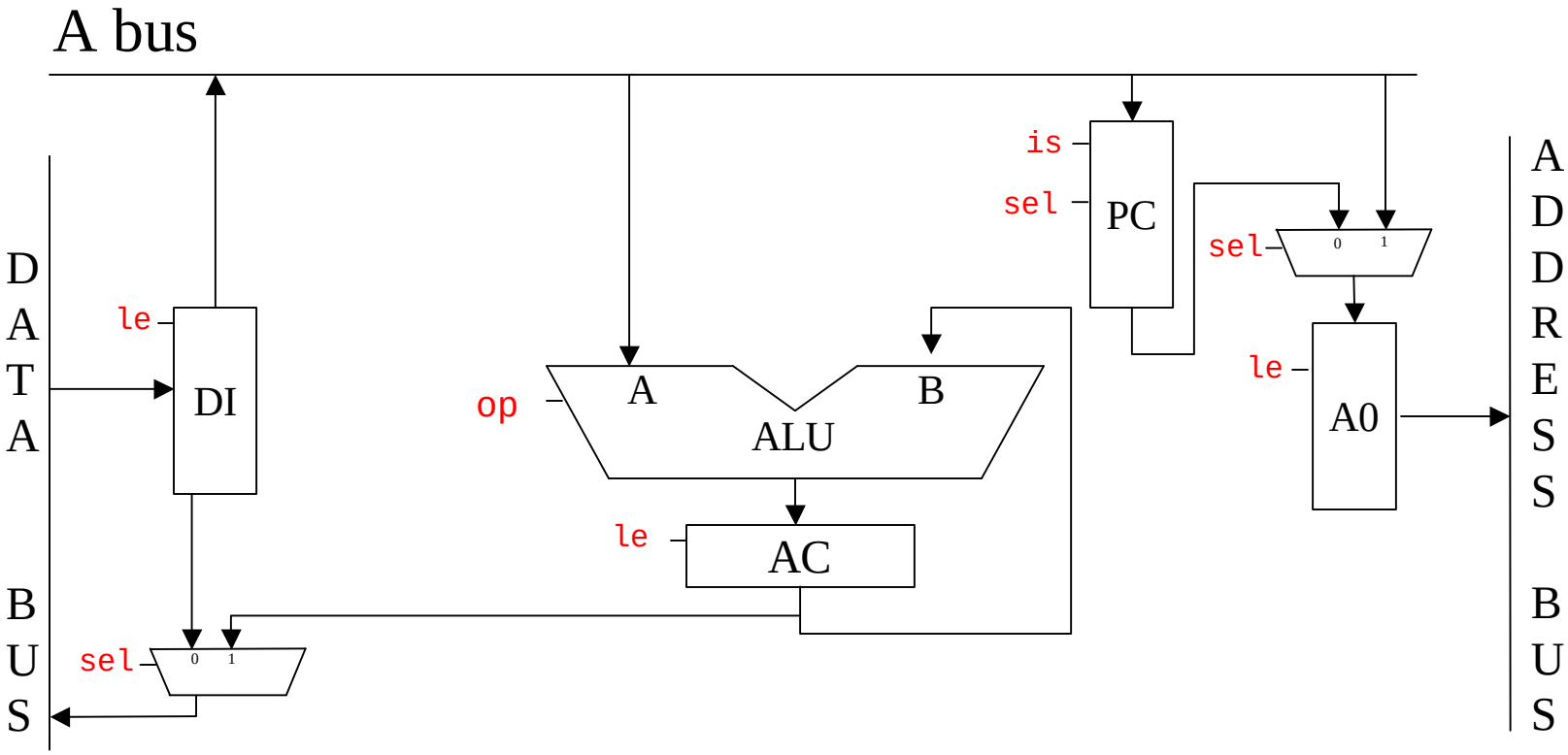


PC capable of loading and incrementing simultaneously

Easy I
Control Unit
(Level 2 Flowcharts)



Easy I
Data Paths (with control points)



Easy I

Control Unit State Transition Table (Part I)

Curr State	opcode	AC:15	Next State	ALU op	Mem OP	PC sel	PC is	DI le	AC le	AO sel	AO le	EDB sel
reset1	xx xxx	x	reset2	XXX	NOP	01	X	0	0	X	0	X
reset2	xx xxx	x	fetch	XXX	NOP	10	1	0	0	0	1	X
fetch	00 00x	x	sopr	XXX	NOP	11	X	1	0	X	0	X
fetch	00 010	x	brn1	XXX	RD	11	X	1	0	X	0	X
fetch	00 011	x	jump	XXX	RD	11	X	1	0	X	0	X
fetch	00 100	x	store1	XXX	RD	11	X	1	0	X	0	X
fetch	00 101	x	load1	XXX	RD	11	X	1	0	X	0	X
fetch	00 11x	x	aopr	XXX	RD	11	X	1	0	X	0	X
aopr	00 110	x	fetch	AND	NOP	10	1	0	1	0	1	X
aopr	00 111	x	fetch	ADD	NOP	10	1	0	1	0	1	X
sopr	00 000	x	fetch	NOTB	NOP	10	1	0	1	0	1	X
sopr	00 001	x	fetch	SHRB	NOP	10	1	0	1	0	1	X

Easy I

Control Unit State Transition Table (Part II)

Current State	opcode	AC:15		Next State	ALU op	Mem OP	PC sel	PC is	DI le	AC le	AO sel	AO le	EDB sel
store1	xx xxx	x		store2	XXX	NOP	11	X	0	0	1	1	X
store2	xx xxx	x		store3	XXX	WR	10	1	0	0	0	1	1
load1	xx xxx	x		load2	XXX	NOP	11	X	0	0	1	1	X
load2	xx xxx	x		load3	XXX	RD	11	X	1	0	X	0	X
load3	xx xxx	x		fetch	XXX	NOP	10	1	0	1	0	1	X
brn1	xx xxx	0		fetch	XXX	NOP	10	1	0	0	0	1	X
brn1	xx xxx	1		brn2	XXX	NOP	10	1	0	0	0	1	X
brn2	xx xxx	x		fetch	XXX	NOP	10	0	0	0	1	1	X
jump	xx xxx	x		fetch	XXX	NOP	10	0	0	0	1	1	X

CU with 14 states => 4 bits of state

Easy-I Control Unit – Some missing details

4-bit Encodings for States

State	Encoding
reset1	0000
reset2	0001
fetch	0010
aopr	0011
sopr	0100
store1	0101
store2	0110
store3	0111
load1	1000
load2	1001
load3	1010
brn1	1011
brn2	1100
jump	1101

ALU Operation Table

Operation	Code	Output
A	000	A
NOTB	001	not B
AND	010	A and B
ADD	011	A + B
SHRB	100	B / 2

We know how to implement this ALU !

Control Bus Operation Table

Operation	Code
NOP	00
ReaD	01
WRite	10

Easy I

Control Unit State Transition Table (Part I)

Curr State	opcode	AC:15	Next State	ALU op	Mem OP	PC sel	PC is	DI le	AC le	AO sel	AO le	EDB sel
0000	xx xxx	x	0001	XXX	00	01	X	0	0	X	0	X
0001	xx xxx	x	0010	XXX	00	10	1	0	0	0	1	X
0010	00 00x	x	0100	XXX	00	11	X	1	0	X	0	X
0010	00 010	x	1011	XXX	01	11	X	1	0	X	0	X
0010	00 011	x	1101	XXX	01	11	X	1	0	X	0	X
0010	00 100	x	0101	XXX	01	11	X	1	0	X	0	X
0010	00 101	x	1000	XXX	01	11	X	1	0	X	0	X
0010	00 11x	x	0011	XXX	01	11	X	1	0	X	0	X
0011	00 110	x	0010	010	00	10	1	0	1	0	1	X
0011	00 111	x	0010	011	00	10	1	0	1	0	1	X
0100	00 000	x	0010	001	00	10	1	0	1	0	1	X
0100	00 001	x	0010	100	00	10	1	0	1	0	1	X

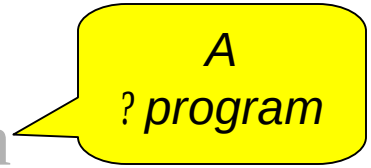
Easy I

Control Unit State Transition Table (Part II)

Current State	opcode	AC:15		Next State	ALU op	Mem OP	PC sel	PC is	DI le	AC le	AO sel	AO le	EDB sel
0101	xx xxx	x		0110	XXX	00	11	X	0	0	1	1	X
0110	xx xxx	x		0111	XXX	10	10	1	0	0	0	1	1
1000	xx xxx	x		1001	XXX	00	11	X	0	0	1	1	X
1001	xx xxx	x		1010	XXX	01	11	X	1	0	X	0	X
1010	xx xxx	x		0010	XXX	00	10	1	0	1	0	1	X
1011	xx xxx	0		0010	XXX	00	10	1	0	0	0	1	X
1011	xx xxx	1		1100	XXX	00	10	1	0	0	0	1	X
1100	xx xxx	x		0010	XXX	00	10	0	0	0	1	1	X
1101	xx xxx	x		0010	XXX	00	10	0	0	0	1	1	X

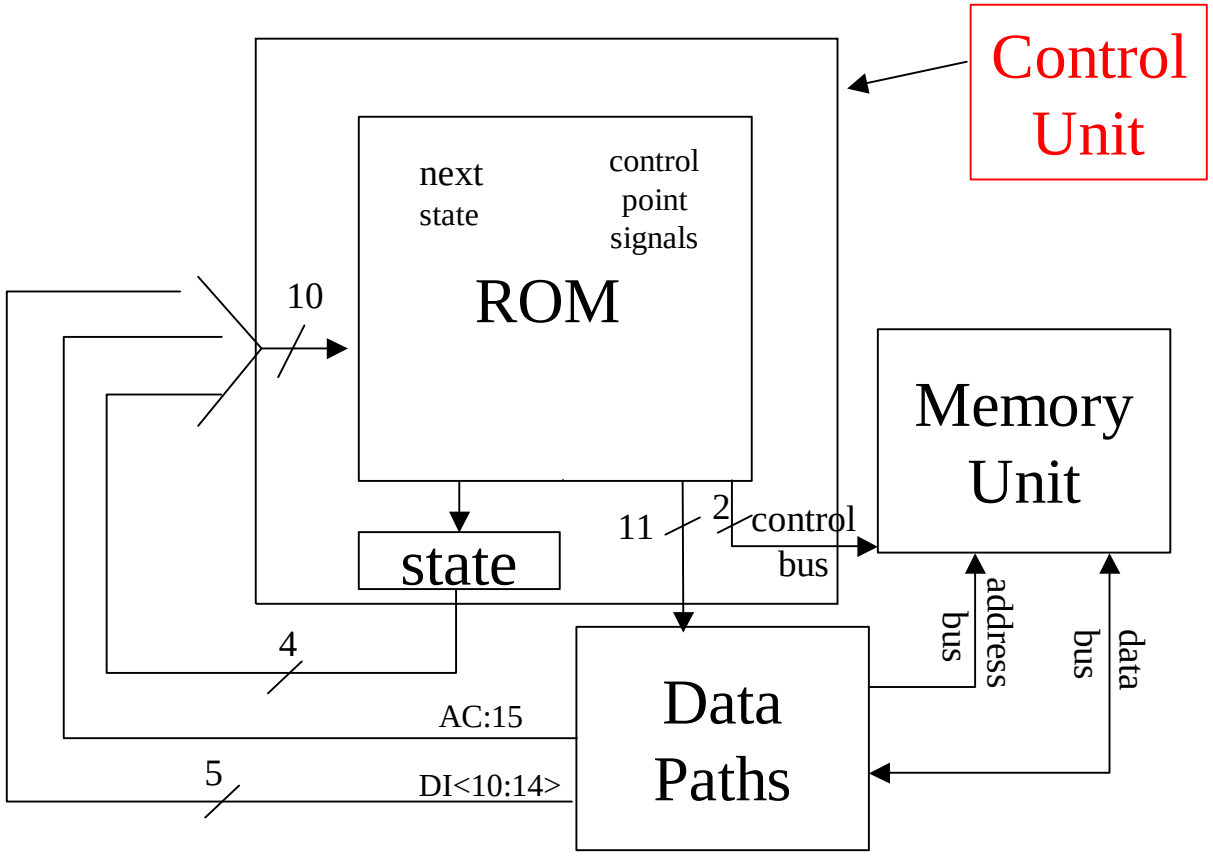
Building the Easy-I C-Unit
2 Approaches

- Harwired
  - Apply well known sequential circuit techniques
- Micro-programmed
  - Treat state transition table as a program
  - Build a new abstraction layer



The Microprogramming abstraction level

Building the Easy-I C-Unit
Hardwired Approach



Easy I

Control Unit State Transition Table (Part II)

Current State	opcode	AC:15	Next State	ALU op	Mem OP	PC sel	PC is	DI le	AC le	AO sel	AO le	EDB sel
0101	xx xxx	x	0110	XXX	000	11	X	0	0	1	1	X
0110	xx xxx	x	0111	XXX	010	10	1	0	0	0	1	1
1000	xx xxx	x	1001	XXX	000	11	X	0	0	1	1	X
1001	xx xxx	x	1010	XXX	001	11	X	1	0	X	0	X
1010	xx xxx	x	0010	XXX	000	10	1	0	1	0	1	X
1011	xx xxx	0	0010	XXX	000	10	1	0	0	0	1	X
1011	xx xxx	1	1100	XXX	000	10	1	0	0	0	1	X
1100	xx xxx	x	0010	XXX	000	10	0	0	0	1	1	X
1101	xx xxx	x	0010	XXX	000	10	0	0	0	1	1	X

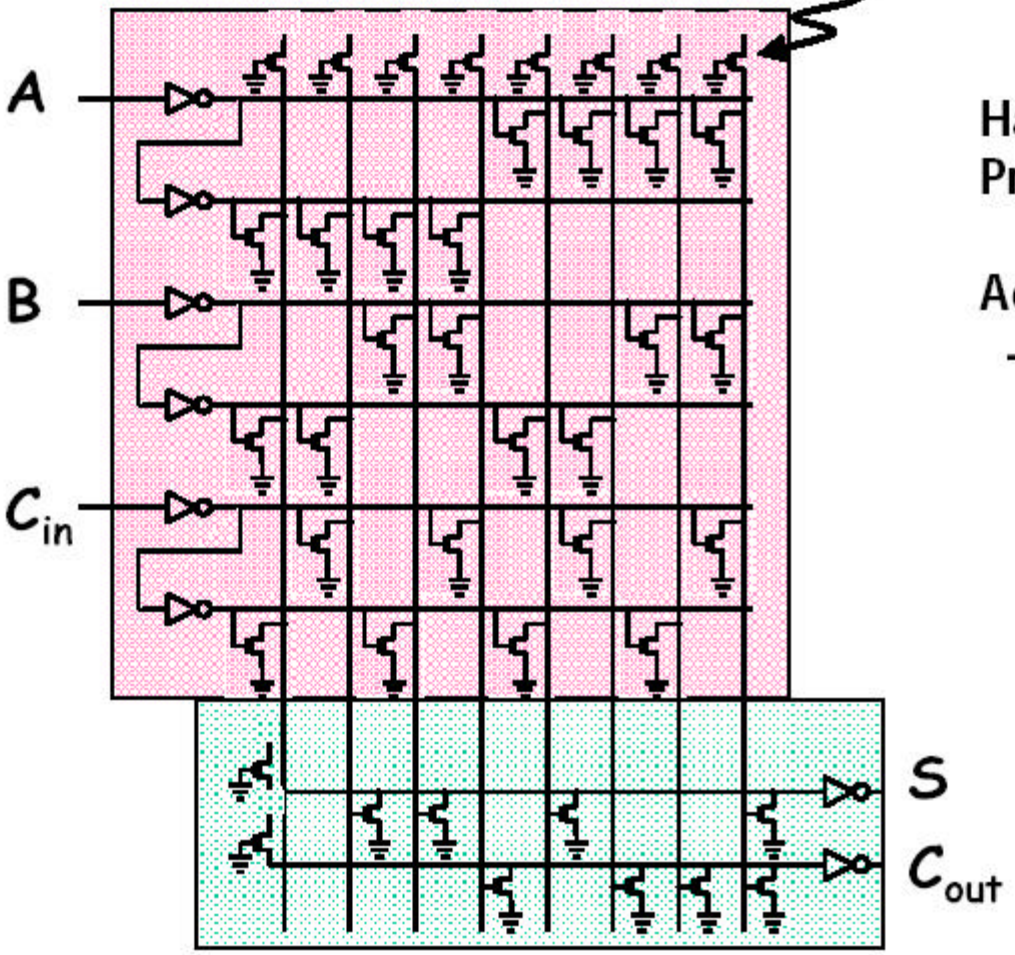
10-bit ROM address

64 ROM Addresses with identical content

18-bit ROM outputs

ROM Implementation Technology

PFET with gate tied to ground = resistor pullup that makes wire "1" unless one of the NFET pulldowns is on.



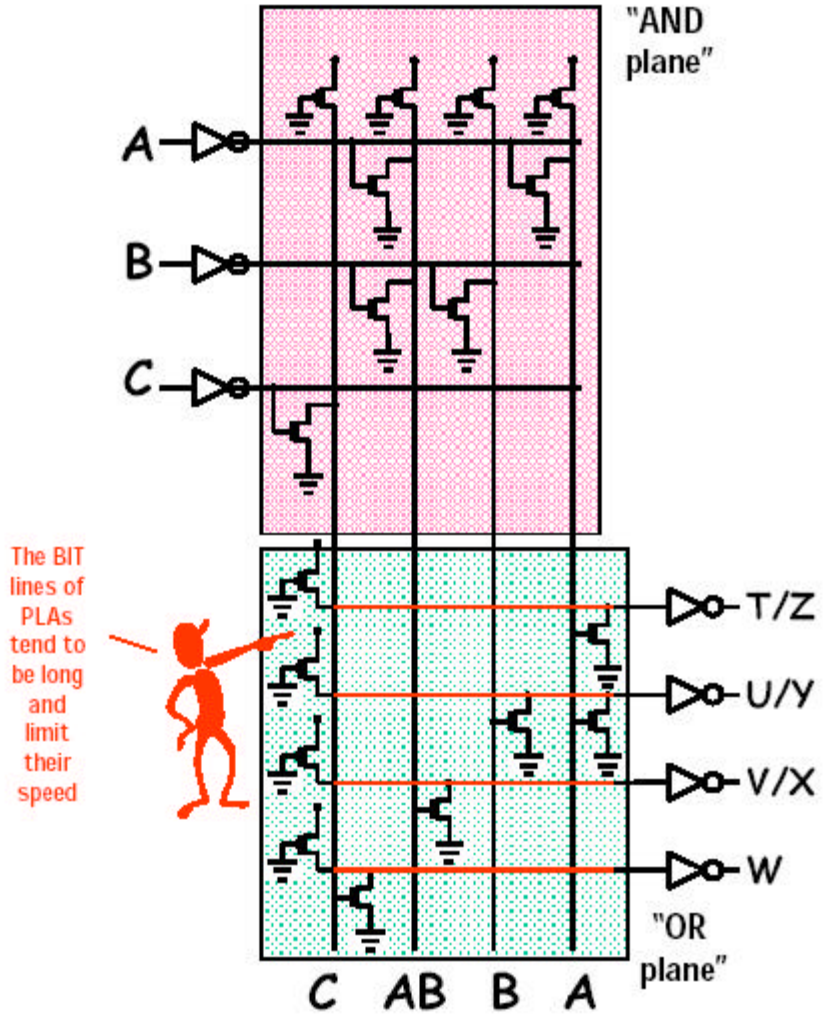
Hardwired AND logic
Programmable OR logic

Advantages:
- Very regular design (can be entirely automated)

Problems:
- Active Pull-ups (Static Power)
- Long metal runs (Large Caps)
- Slow

JARGON: Inputs to a ROM are called ADDRESSES. The decoder's outputs are called WORD LINES, and the outputs lines of the selector are called BIT LINES.

PLA 7-sided Die implementation



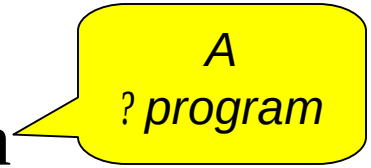
PLAs like ROMs support the synthesis of arbitrary logic functions using SOP implementations.

However, they allow for
- minimal realizations
- smaller (faster) arrays

Regular structure
- automatic generation
- easy design
- still slower than optimized gates

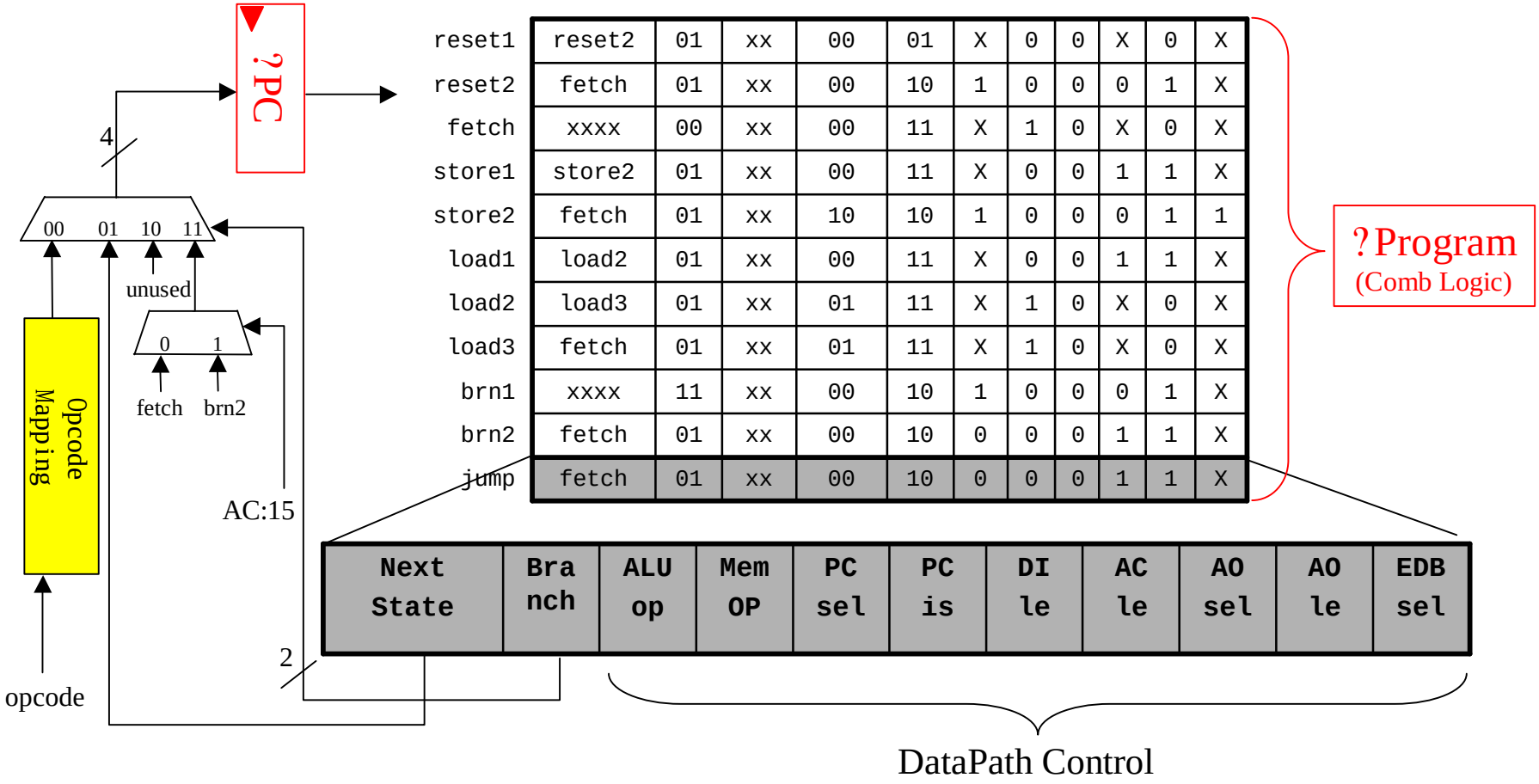
Building the Easy-I C-Unit
2 Approaches

- Harwired
  - Apply well known sequential circuit techniques
- Micro-programmed
  - Treat state transition table as a program
  - Build a new abstraction layer



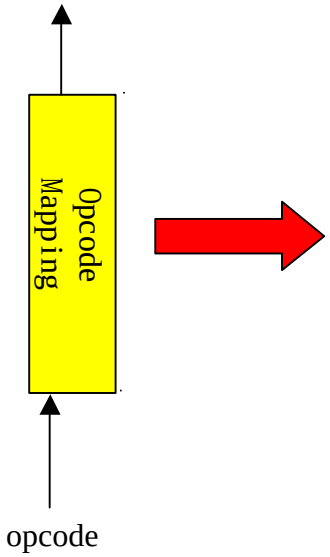
The Microprogramming abstraction level

Building the Easy-I C-Unit
Micro-programmed Approach



Finding the first execute state

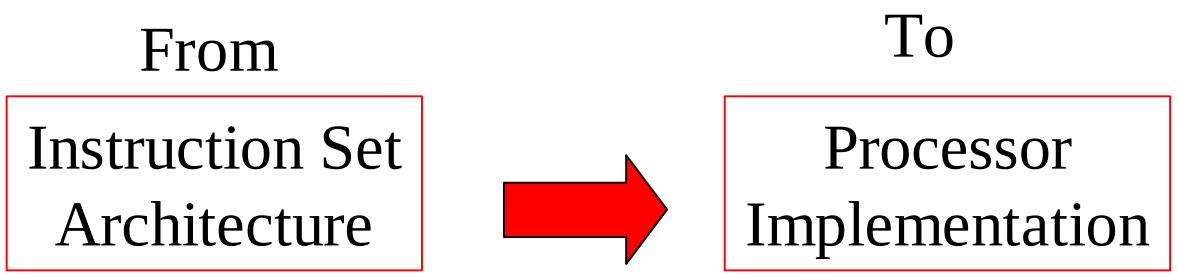
Combinational Logic



Instruction	Opcode	AC:15	First Execute State
Comp	00 000	x	sopr
ShR	00 001	x	sopr
BrN	00 010	1	brn1
Jump	00 011	x	jump
Store	00 100	x	store1
Load	00 101	x	load1
And	00 110	x	aopr
Add	00 111	x	aopr

Summary

What we know?



What Next?