Hola,

Los siguientes problemas provienen del capitulo 10 de la cuarta edición del libro de Sedra. El material relacionado con convertidores es el mismo material que esta en la página de la sexta edición, pero la numeración de las figuras cambia.

Los problemas sugeridos son desde el 60 al 67. Las figuras corresponden como sigue: en el documento que estamos usando el capitulo es el 9, en el documento original es el 10. Las figuras asociadas al material tienen numeración desde la 36 a la 44 en el material nuevo, y corresponden a las figuras 29 a la 37 de los problemas que incluyo. O sea, si el problema hace referencia a la figura 10-32, deben usar la figura 9-39 del documento pdf que esta en la pagina.

Cordialmente,

Manuel Toledo

10.56 Find the output resistance and the dc open-loop voltage gain of the folded cascode amplifier of Fig. 10.27 whose parameters are specified in Exercise 10.30. Assume $|V_A| = 25$ V for all devices.

D*10.57 Design the folded cascode circuit of Fig. 10.27 to obtain a dc open-loop voltage gain of 10,000 V/V and a unity-gain bandwidth of 1 MHz when the total capacitance at the output is 10 pF. Design for $I_B = 2I$, $(W/L)_1 = (W/L)_{4C} = 2(W/L)_{2C}$. Specify the required values of I and $(W/L)_1$. Let $\mu_n C_{ox} = 2\mu_p C_{ox} = 20\ \mu A/V^2$ and $|V_A| = 25$ V. (*Hint:* Use Eq. 10.67.)

D10.58 It is required to design the folded-cascode CMOS op-amp circuit of Fig. 10.27. The load capacitance C_L (including all parasitics) is 10 pF. The total capacitance at the input of each of the common-gate transistors Q_{1C} and Q_{2C} is $C_P = 1$ pF. Design for bias currents $2I = I_B = 100\ \mu A$ and $(W/L)_{1C} = (W/L)_{2C} = 10/10$. To obtain a sufficient phase margin the design should ensure that $f_t \leq f_P/3$, where f_P is the frequency of the nondominant pole due to C_P. Specify the required W/L ratios for the input transistors to obtain the largest possible f_t. What is the value of f_t realized? Assume that $\mu_n C_{ox} = 2\ \mu_p C_{ox} = 20\ \mu A/V^2$.

D10.59 A folded-cascode BiCMOS amplifier having the topology of Fig. 10.28 is designed to operate at high frequencies. The bias currents are $2I = I_B = 400\ \mu A$, and the W/L ratio for the input stage transistors is 300/10. Find f_t for a load capacitance C_L (including all the output node parasitics) of 2 pF. To maintain an acceptable phase margin, the parasitic pole created at the input to the cascode transistors Q_{1C} and Q_{2C} must be at least three times higher in frequency than f_t. What is the largest parasitic capacitance C_P that can be tolerated? Assume $\mu_p C_{ox} = 10\ \mu A/V^2$.

Section 10.9: Data Converters—An Introduction

10.60 An analog signal in the range 0 to +10 V is to be digitized with a quantization error of less than 1% of full scale. What is the number of bits required? What is the resolution of the conversion? If the range is to be extended to ±10 V with the same requirement, what is the number of bits required? For an extension to a range of 0 to +15 V, how many bits are required to provide the same resolution? What is the corresponding resolution and quantization error?

***10.61** Consider Fig. 10.31. On the staircase output of the S/H circuit sketch the output of a simple low-pass RC circuit with a time constant that is (a) one-third of the sampling interval; (b) equal to the sampling interval.

Section 10.10: D/A Converter Circuits

***10.62** Consider the DAC circuit of Fig. 10.32 for the cases $N = 2$, 4, and 8. What is the tolerance, expressed as $\pm x\%$, to which the resistors should be selected so as to limit the resulting output error to the equivalent of $\pm\frac{1}{2}$ LSB?

10.63 The BJTs in the circuit of Fig. P10.63 have their base–emitter junction areas scaled in the ratios indicated. Find I_1 to I_4 in terms of I.

10.64 A problem encountered in the DAC circuit of Fig. 10.34 is the large spread in transistor EBJ areas required when N is large. As an alternative arrangement consider using the circuit in Fig. 10.34 for 4 bits only. Then, feed the current in the collector of the terminating transistor Q_t to the circuit of Fig. P10.63 (in place of the current source I), thus producing currents for 4 more bits. In this way, an 8-bit DAC can be implemented with a maximum spread in areas of 8. What is the total area of emitters needed in terms of the smallest device? Contrast this with the usual 8-bit circuit. Give the complete circuit of the converter thus realized.

D*10.65 The circuit in Fig. 10.32 can be used to multiply an analog signal by a digital one by feeding the analog signal to the V_{ref} terminal. In this case

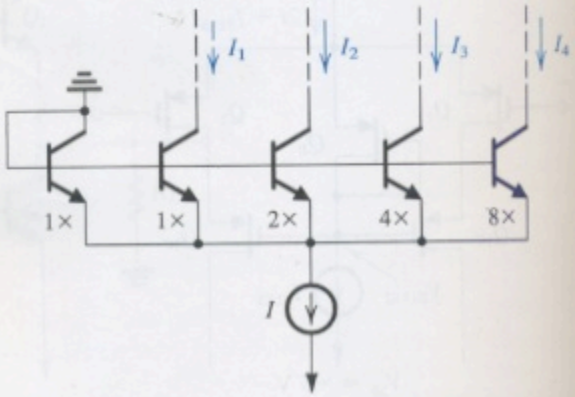


Fig. P10.63

the D/A converter is called a **multiplying DAC** or MDAC. Given an input sine-wave signal of $0.1 \sin \omega t$ volts, use the circuit of Fig. 10.32 together with an additional op amp to obtain $v_O = 10D \sin \omega t$ where D is the digital word given by Eq. (10.72) and $N = 4$. How many discrete sine-wave amplitudes are available at the output? What is the smallest? What is the largest? To what digital input does a 10-V peak-to-peak output correspond?

10.66 What is the input resistance seen by V_{ref} in the circuit of Fig. 10.33?

Section 10.11: A/D Converter Circuits

10.67 A 12-bit dual-slope ADC of the type illustrated in 10.36 utilizes a 1-MHz clock and has $V_{ref} = 10$ V. Its analog input voltage is in the range 0 to -10 V. The fixed interval T_1 is the time taken for the counter to accumulate a count of 2^N. What is the time required to convert an input voltage equal to the full-scale value? If the peak voltage reached at the output of the integrator is 10 V, what is the integrator time constant? If through aging, R increases by 2% and C decreases by 1%, what does V_{peak} become? Does the conversion accuracy change?

10.68 The design of a 4-bit flash ADC as shown in Fig. 10.38 is being considered. How many comparators are required? For an input signal in the range of 0 to +10 V, what are the reference voltages needed? Show how they can be generated using a 10-V reference and several 1-kΩ resistors (how many?). If a comparison is possible in 50 ns and the associated logic requires 35 ns, what is the maximum possible conversion rate? Indicate the digital code you expect at the output of the comparators and at the output of the logic for an input of (a) 0 V, (b) +5.1 V, and (c) +10 V.

10-60

$\frac{1}{2}$ LSB must be less than 1%

i.e $\frac{1}{2}\frac{1}{2^N} \leq \frac{1}{100} \Rightarrow N \geq 5.6$

$\therefore$ N = 6 bits

Resolution $\frac{10\,V}{2^6} = 0.156\,V$

For same resolution need 7 bits

STill 7 bits

resolution = $\frac{15}{2^7} = 0.117\,V$

Q = $\frac{1}{2}$ LSB = $\frac{1}{2}\frac{15}{2^7} = 0.059\,V$.

61 — 10

--- $\tau = \frac{1}{3}T$

$\tau = T$

10-62 Require error in MSB $\leq \frac{1}{2}$ LSB

$$\frac{V}{R} - \frac{V}{R\left(1+\frac{x}{100}\right)} \leq \frac{1}{2}\frac{V}{2^{N-1}R}$$

$$\frac{1+\frac{x}{100}-1}{1+\frac{x}{100}} \leq \frac{1}{2^N} \quad \text{or} \quad \frac{x}{100}\left(2^N-1\right) \leq 1$$

$$\Rightarrow \quad x = \frac{1}{2^N-1} \times 100$$

$N=2 \quad x = 33.3\,\%$

$N=4 \quad x = 6.67\,\%$

$N=8 \quad x = 0.39\,\%$

10-63 Since V_{BE}'s are equal, collector currents are scaled with respect to emitter areas

$I_1 + I_1 + I_2 + I_3 + I_4 = I$

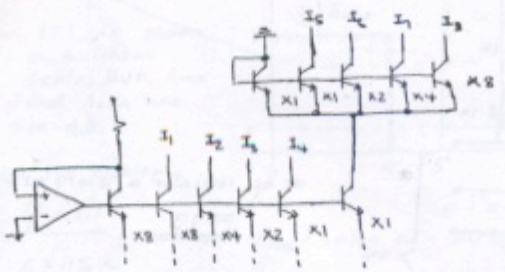
$I_1(1+1+2+4+8) = I \Rightarrow I_1 = I/16$

$I_2 = I/8$

$I_3 = I/4 \qquad I_4 = I/2$

64 — 10

Circuit is sketched below



$A_{tot} = 8+8+4+2+1+1+1+1+2+4+8$

$\Rightarrow 40$

For 8-bits binary weighted

$A_{tot} = (1 + 1+2+4+\cdots+2^{N-1}+2^{N-1})$

(Φ_1 ↖ , ↗ Φ_{ref})

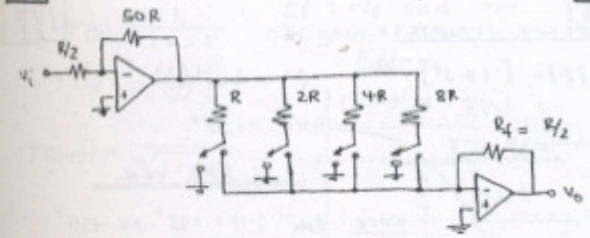
$= 2^{N-1}+1 \quad \{1+2+4+\cdots+2^{N-1}\}$

$= 2^{N-1}+1+2^N-1 = 2^{N-1}+2^N$

$N=8$

$A_{tot} = 2^7 + 2^8 = 384$

65 — 10



$2^N - 1$ discrete outputs $= 2^4 - 1$

$= 15$

Smallest sine wave $= \frac{10}{2^4} = 0.625V$

largest $= 10 \times \frac{G_{eq}}{G_{fi}} = 10 \cdot \frac{1+\frac{1}{2}+\frac{1}{4}+\frac{1}{8}}{2}$

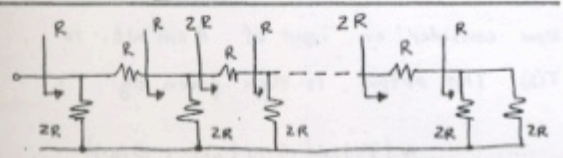
$= 5\,\frac{1}{8}(1+2+4+8) = \frac{5}{8}(2^4-1)$

$= 9.375\,V$

10 V pk-pk $\Rightarrow$ 5 V pk or $\frac{1}{2}$ FS

$\therefore D = 1000$

66



$R_{in} = R$

67 — 10

$T_C = \frac{1}{f_{clk}} = 1\,\mu s$

$T_1 = 2^{12} T_C = 4.096\,ms$

$T = T_1 + T_2 = T_1\left(1+\frac{V_A}{V_{ref}}\right)$

$= 2T_1 = 8.19\,ms$

$V_{peak} = 10 = \frac{V_A}{\tau} T_1$

$\Rightarrow \tau = \frac{V_A}{V_{peak}} T_1 = 4.096\,ms$

$\Delta\tau = -1\%$ and causes a -1% change in V_{peak}

$\Rightarrow V_{peak} = 9.9\,V$

No. Final count does not depend on τ

68 $2^N - 1$ comparators $= 15$

comparators are biased 1LSB apart starting from $\frac{1}{2}$ LSB

Thus, $V_{refn} = \left(\frac{2n-1}{2}\right)$ LSB

1 LSB $= \frac{10}{2^4} = 0.625\,V$

and references are 0.3125, 0.9375, 1.5625, 2.1875

2.8125 ..... 9.0625