BICMOS

INEL 4207 - M. Toledo

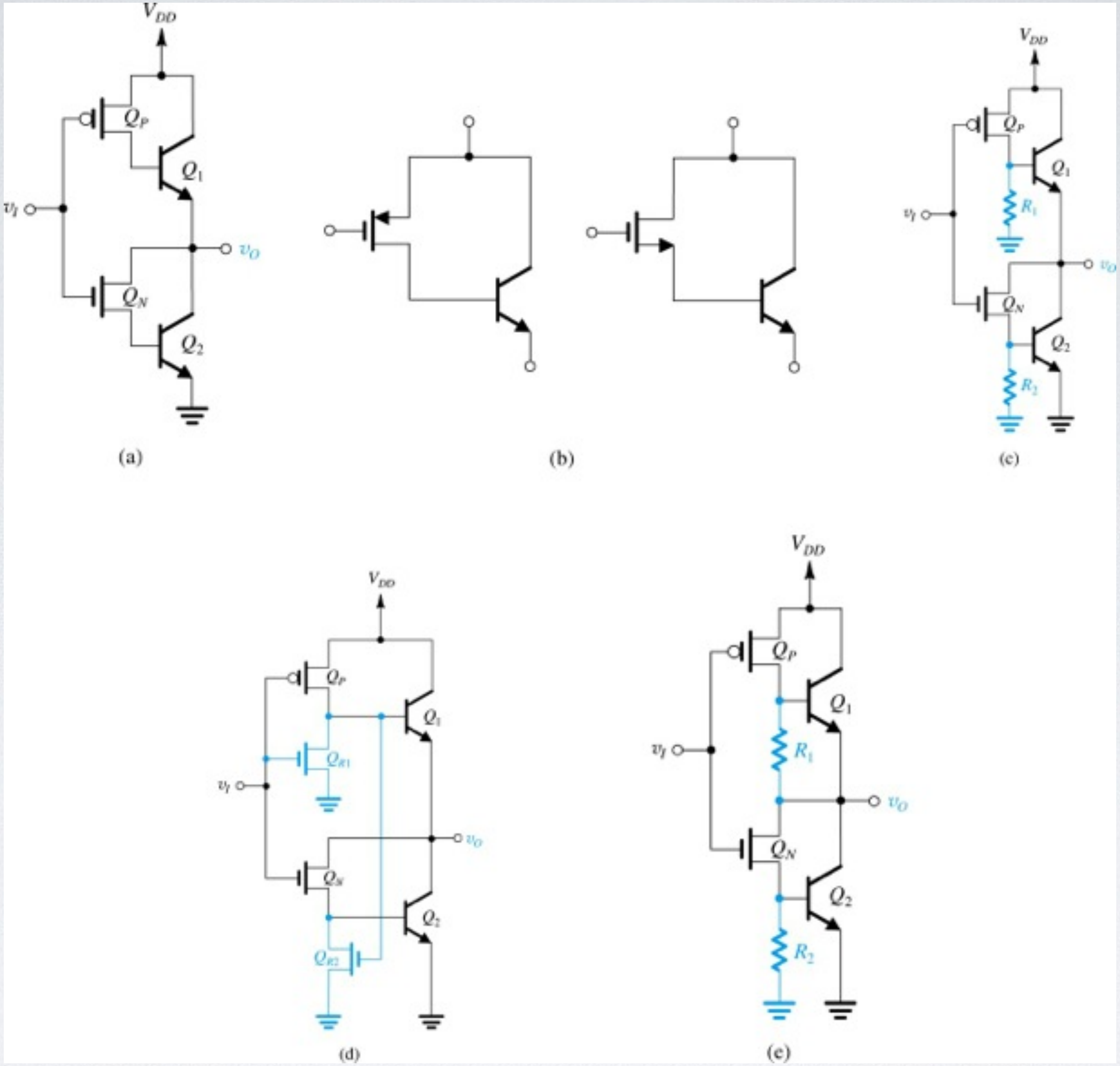


Figure 15.37 Development of the BiCMOS inverter circuit. **(a)** The basic concept is to use an additional bipolar transistor to increase the output current drive of each of Q_N and Q_P of the CMOS inverter. **(b)** The circuit in **(a)** can be thought of as utilizing these composite devices. **(c)** To reduce the turn-off times of Q_1 and Q_2, "bleeder resistors" R_1 and R_2 are added. **(d)** Implementation of the circuit in (**c**) using NMOS transistors to realize the resistors. **(e)** An improved version of the circuit in (**c**) obtained by connecting the lower end of R_1 to the output node.

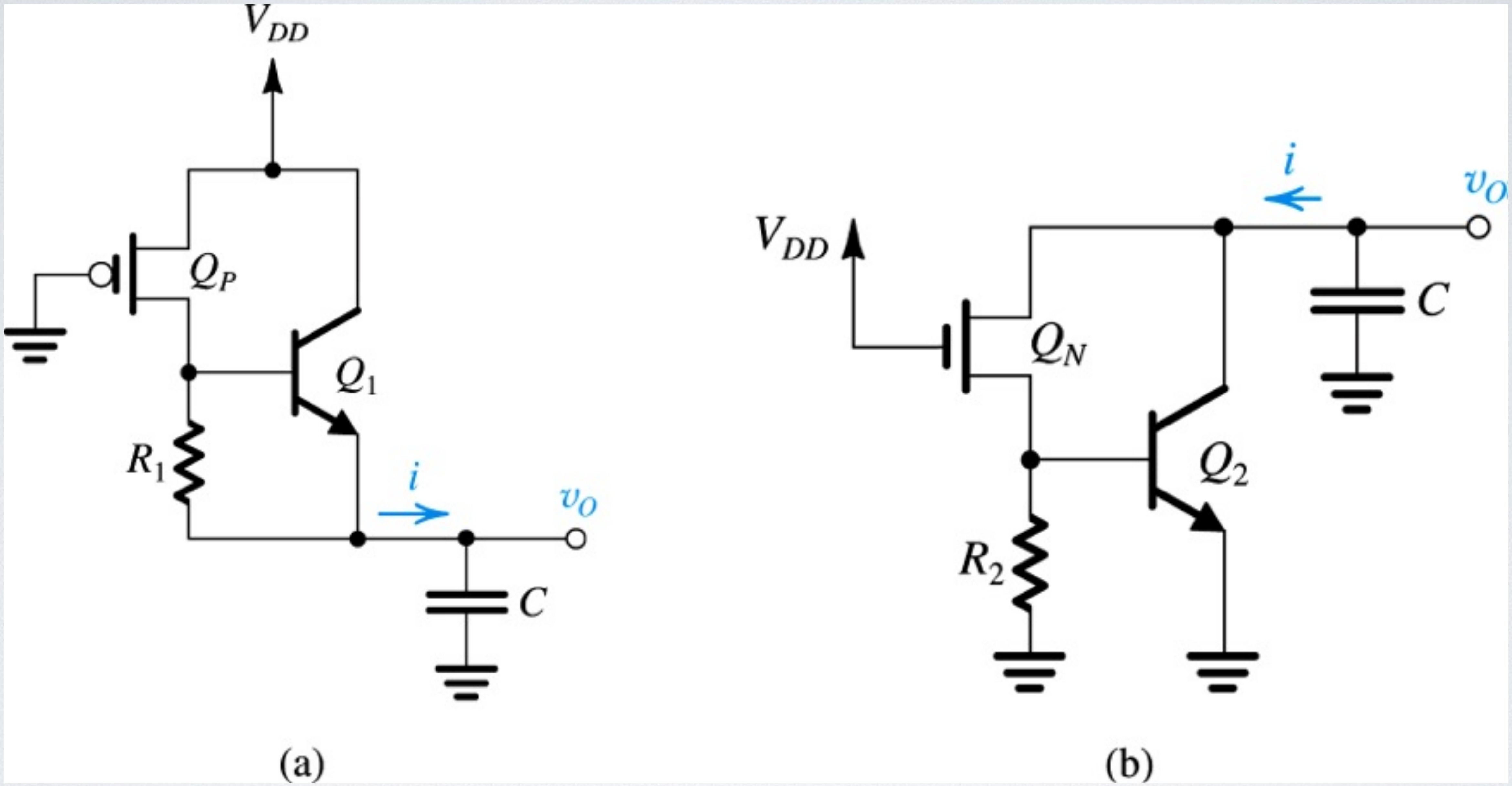


Figure 15.38 Equivalent circuits for charging and discharging a load capacitance *C*. Note that *C* includes all the capacitances present at the output node.

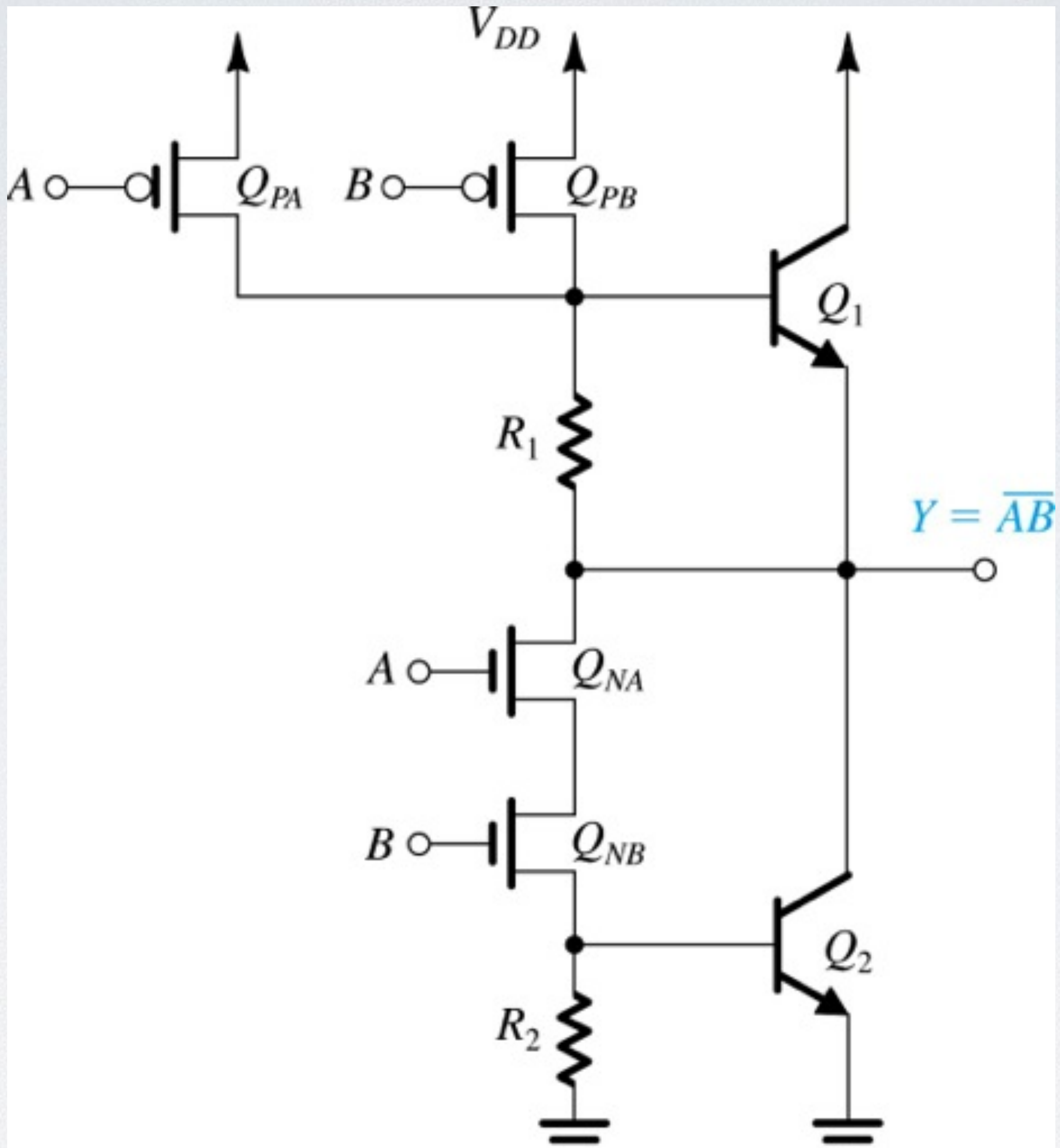
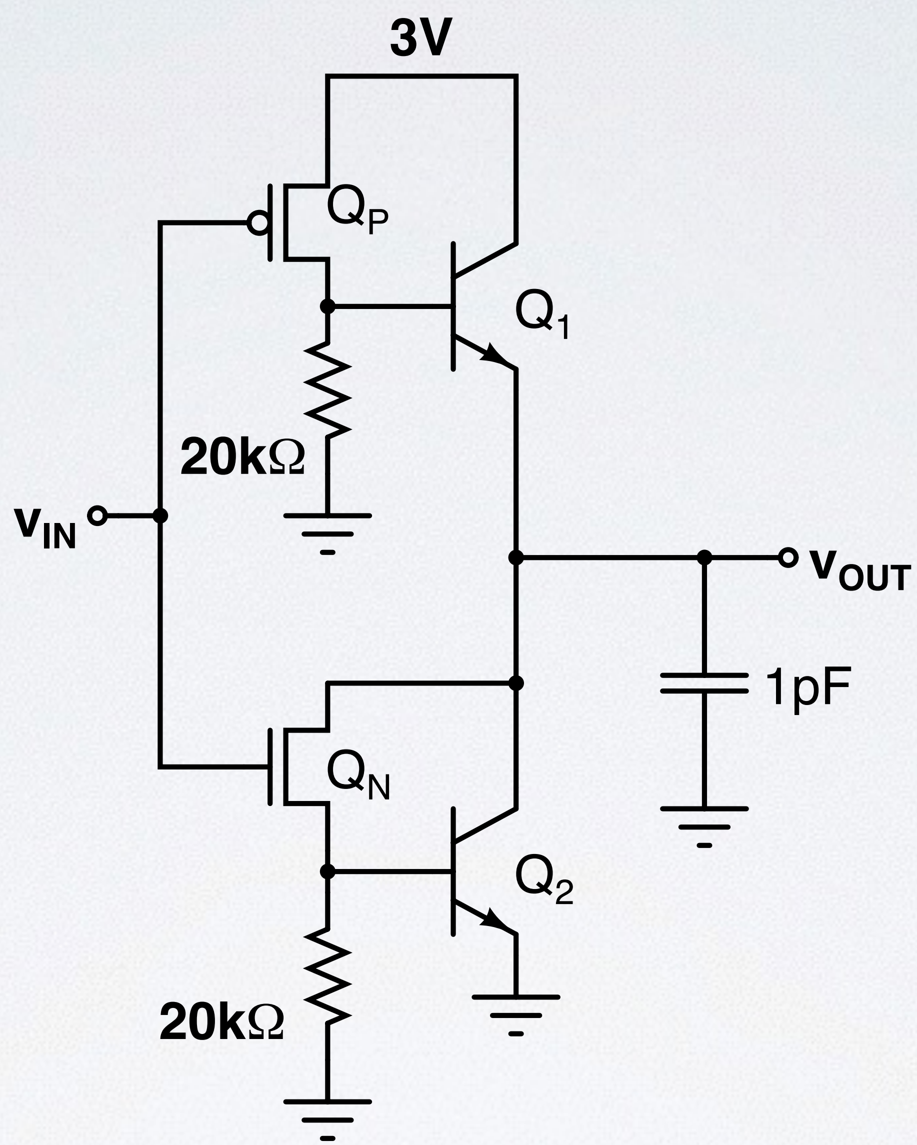
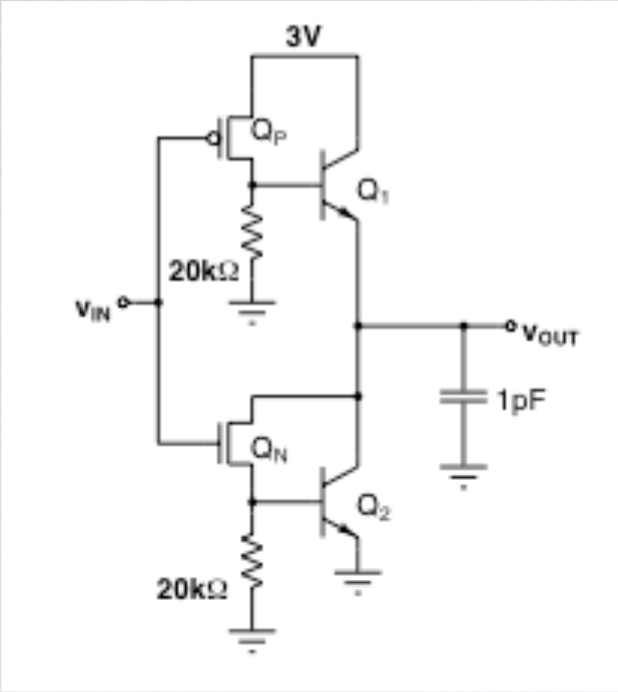


Figure 15.39 A BiCMOS two-input NAND gate.



For the above BiCMOS circuit, estimate the time t_d that it takes to discharge C_L from its initial voltage $v_{out,i}$ (the largest value of v_{out} that the circuit can reach) to $v_{out,i}/2$. Assume that $v_{BE} = 0.7V$ and $\beta = 20$ for the bipolar transistors, $k_n = 300\mu A/V^2$ for Q_N and $k_p = 100\mu A/V^2$ for Q_P. For both MOSFETs the threshold voltage is $|V_{t0}| = 0.5V$ and $\gamma = 0$. Use $v_{IN} = 3V$.



1. Find $v_{out,i}$

$$i_{C1} = 0 \rightarrow i_{B1} = 0 \rightarrow i_{D,P} = i_{20k\Omega}$$

$$\frac{3V - v_{SD,P}}{20k\Omega} = \left(0.1mA/V^2\right)\left(2(3V - 0.5V)v_{DS,P} - v_{DS,P}^2\right)$$

$$\frac{3V - v_{SD,P}}{2} = 5v_{DS,P} - v_{DS,P}^2$$

$$v_{SD,P} = 5.2V, \boxed{0.29V} \Rightarrow \boxed{v_{OUT} \simeq 3V - 0.3V - 0.7 = 2V}$$

2. Find the initial capacitor current

The initial voltage across the capacitor is $\boxed{v_{out,i} = 2.0V}$. At point 1, $v_{OUT} =$ $2.0V$ and

$$\begin{aligned} v_{DS,N} &= 2.0V - 0.7V = 1.3V \\ v_{GS,N} - V_{t0} &= 3V - 0.7V - 0.5V = 1.8V \\ i_{D1} &= (0.3mA/V^2)[2(1.8V)1.3V - (1.3V)^2] = 0.897mA \\ i_1 &= \beta(i_{D1} - 0.7V/20k\Omega) + i_{D1} = 20(0.897mA - 0.035mA) + 0.897 = \boxed{18.147mA} \end{aligned}$$

3. Find the capacitor current when $v_{out} = v_{out,i}/2$

At point 2, $v_{out} = 2.0V/2 = 1.0V$ and

$$\begin{aligned} v_{DS,N} &= 1.0V - 0.7V = 0.3V \\ v_{GS,N} - V_{t0} &= 3V - 0.7V - 0.5V = 1.8V \\ i_{D2} &= (0.3mA/V^2)[2(1.8V)0.3V - (0.3V)^2] \simeq 0.3mA \\ i_2 &= \beta(i_{D2} - 0.7V/20k\Omega) + i_{D2} \\ &= 20(0.3mA - 0.035mA) + 0.3mA = \boxed{5.6mA} \end{aligned}$$

4. Find i_{ave} and t_d

$$i_{av} = \frac{18.15mA + 5.6mA}{2} \simeq 11.9mA$$

$$t_d = 1pF \frac{1.0V}{11.9mA} = \boxed{84.2ps}$$

The threshold voltage of the BiCMOS inverter of Fig. 15.37(e) is the value of v_I at which both Q_N and Q_P are conducting equal currents and operating in the saturation region. At this value of v_I, Q_2 will be on, causing the voltage at the source of Q_N to be approximately 0.7 V. It is required to design the circuit so that the threshold voltage is equal to $V_{DD}/2$. For $V_{DD} = 5$ V, $|V_t| = 0.6$ V, and assuming equal channel lengths for Q_N and Q_P and that $\mu_n \simeq 2.5\,\mu_p$, find the required ratio of widths, W_p/W_n.

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Ans. 1

$$v_I = 2.5V$$
$$v_{SG,P} - |V_t| = 5V - 2.5V - 0.6V = 1.9V$$
$$v_{GS,N} - V_t = 2.5V - 0.7V - 0.6V = 1.2V$$
$$\frac{2.5\mu_p C_o x}{2}\frac{W_n}{L}(1.2V)^2 = \frac{\mu_p C_o x}{2}\frac{W_p}{L}(1.9V)^2$$
$$\frac{W_p}{W_n} = \boxed{0.997}$$