RS FLIP FLOP

BASIC OPERATION

INEL 4207 Digital Electronics - M. Toledo

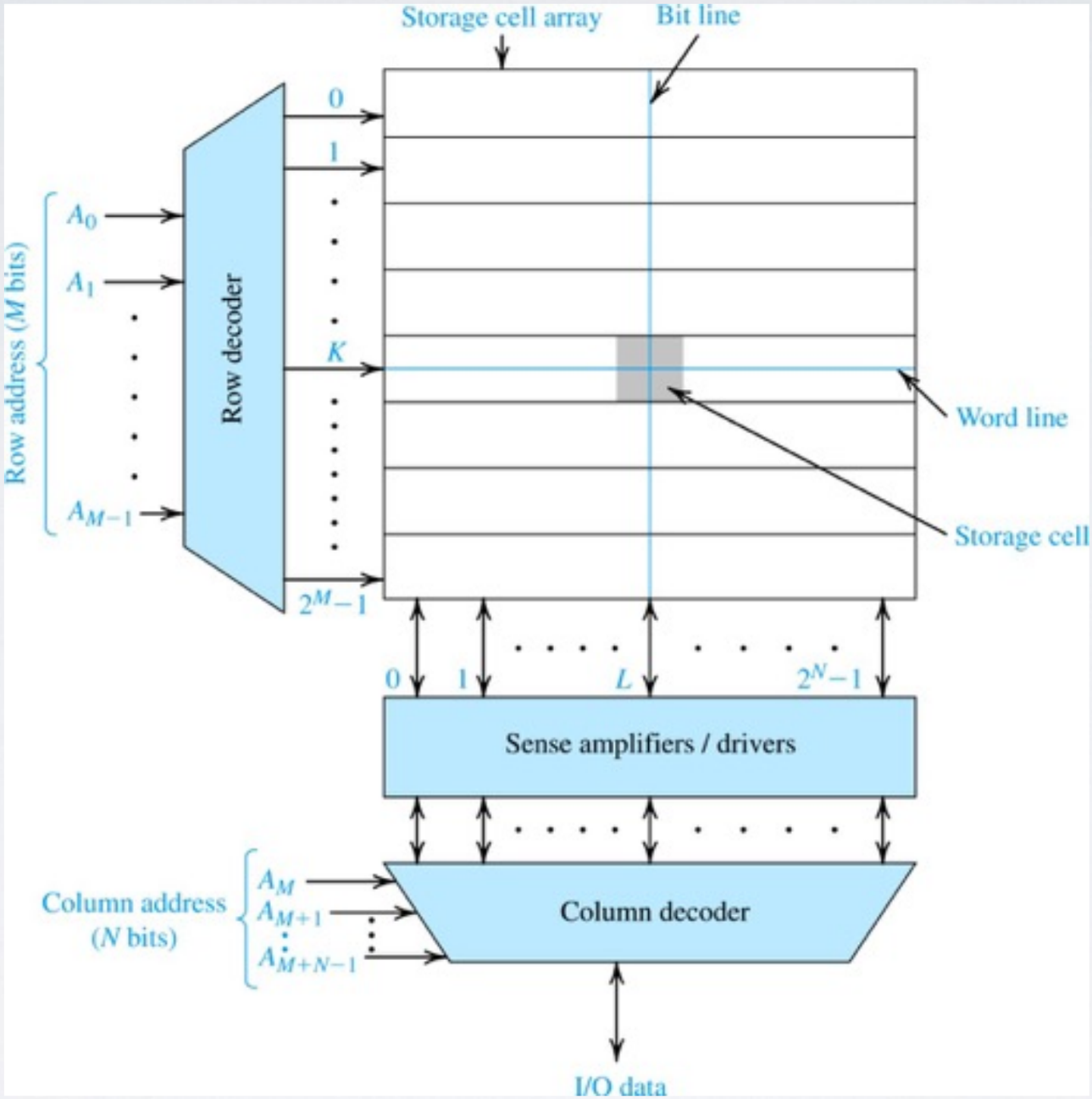
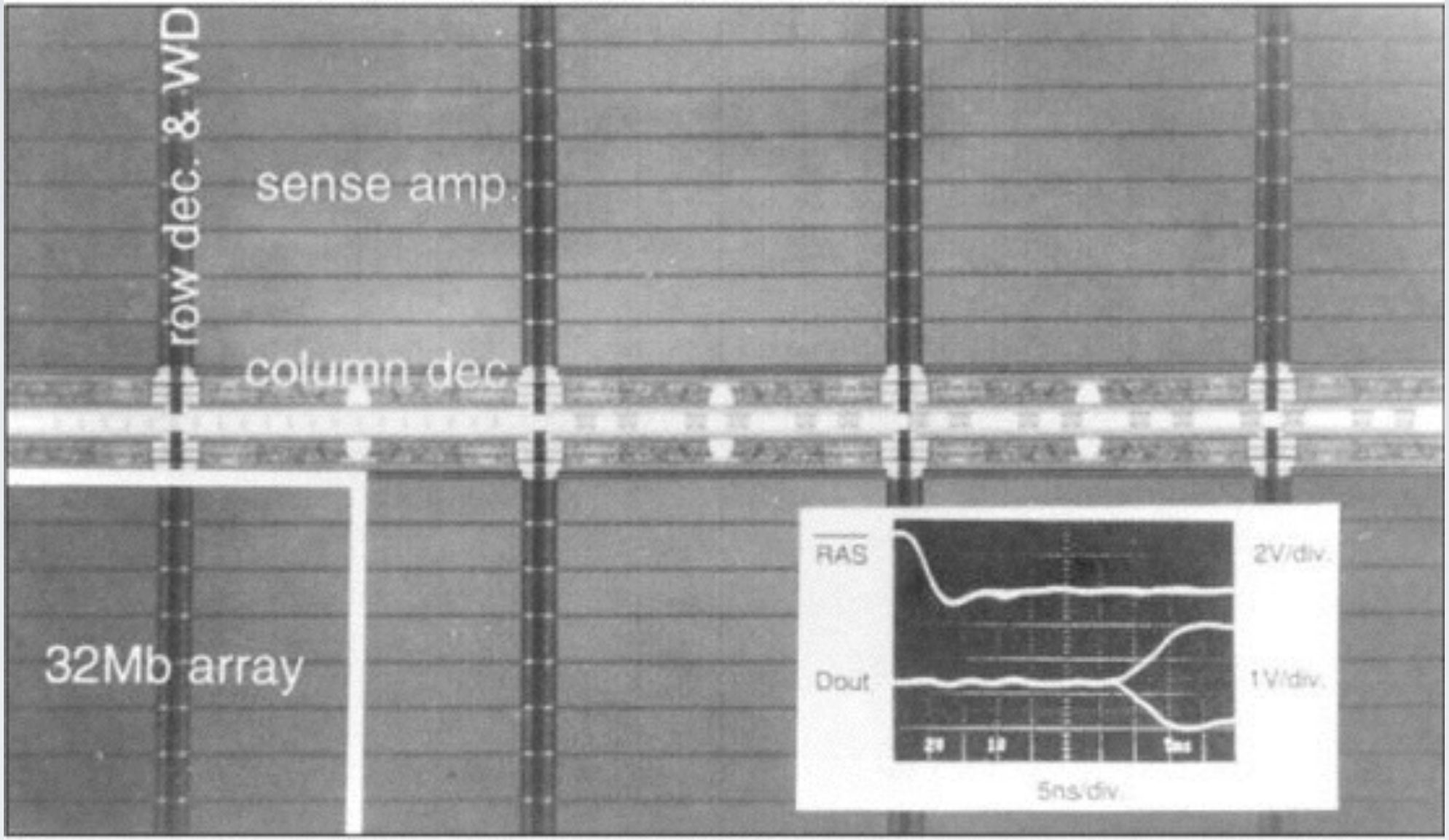


Figure 16.11 A 2^{M+N} -bit memory chip organized as an array of 2^M rows × 2^N columns.



(a)

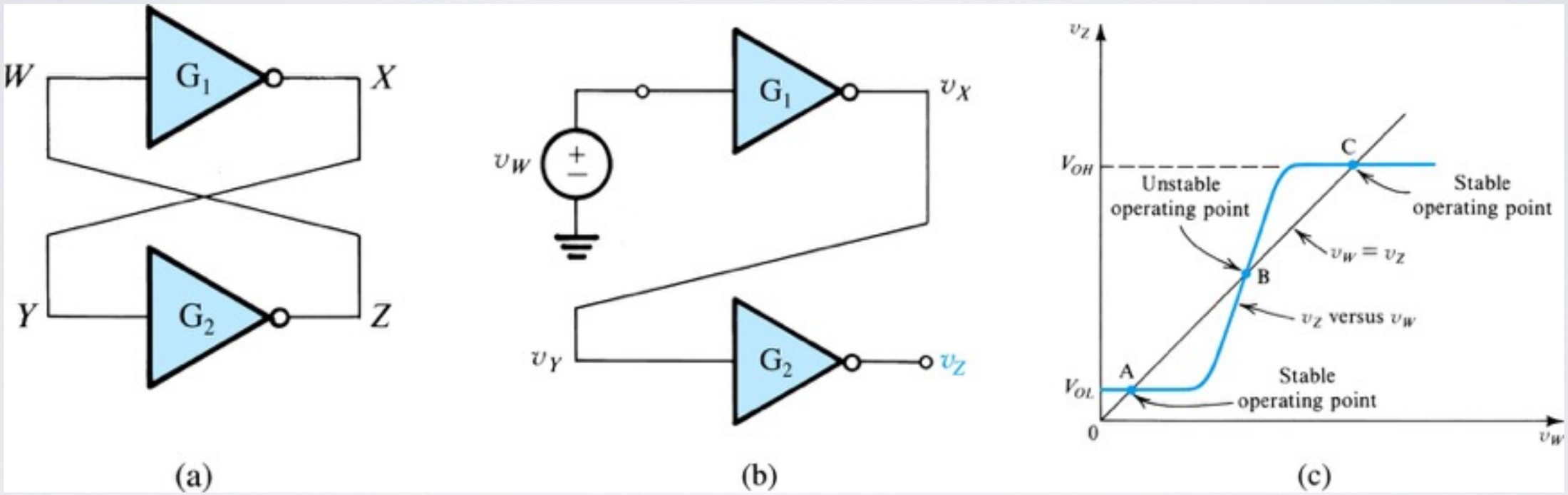
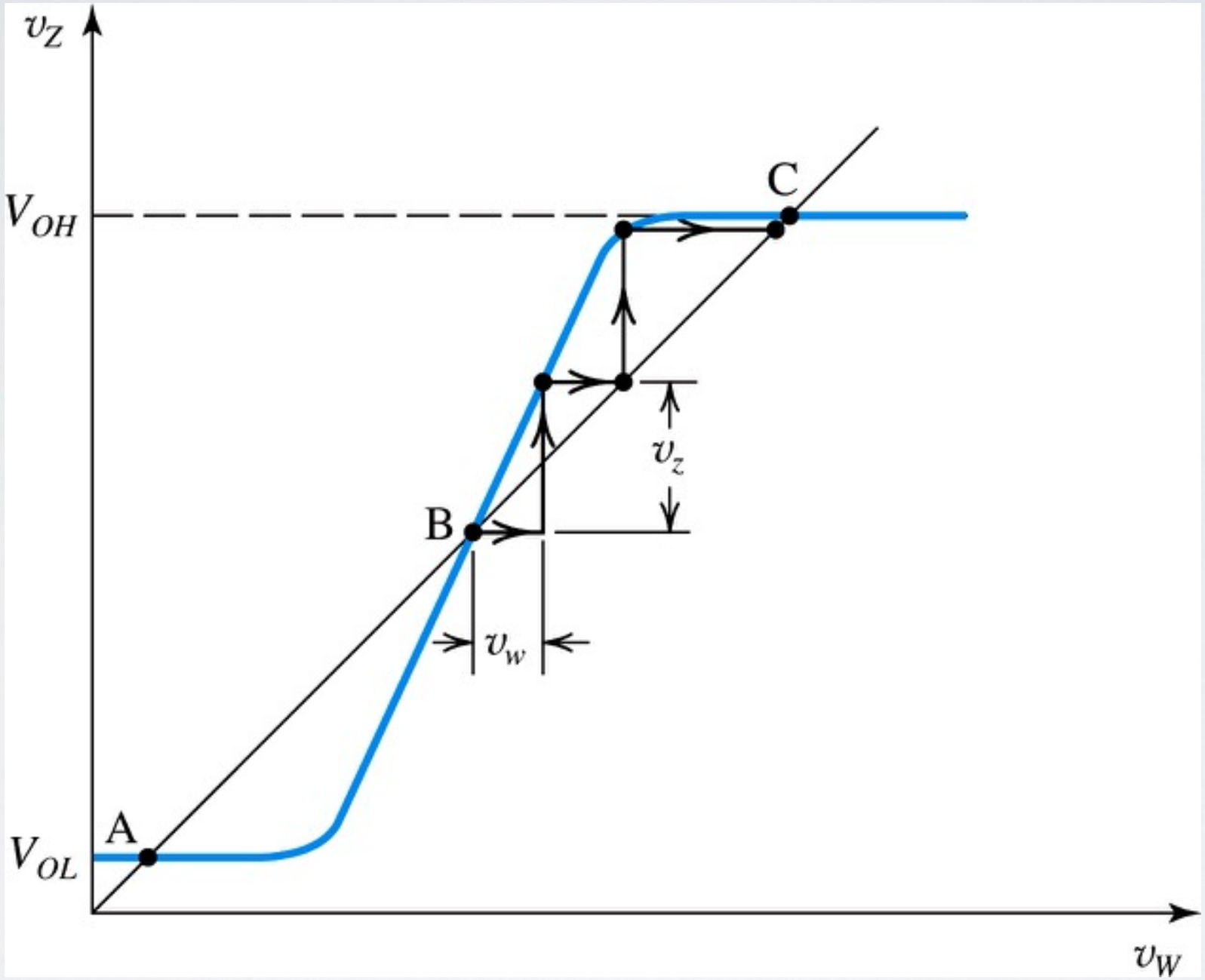
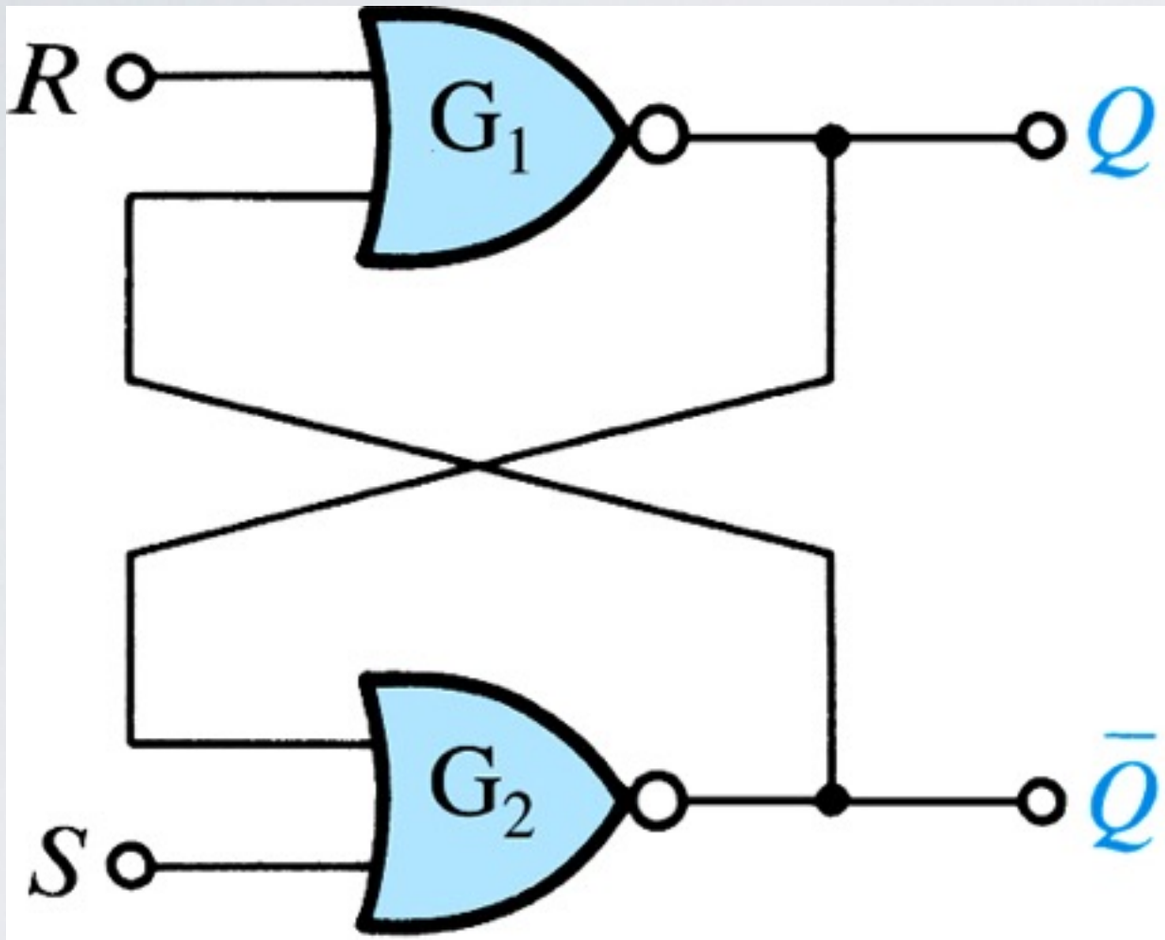


Figure 16.1 (a) Basic latch. (b) The latch with the feedback loop opened. (c) Determining the operating point(s) of the latch.


v_Z
V_{OH}
C
v_z
B
v_w
A
V_{OL}
v_W

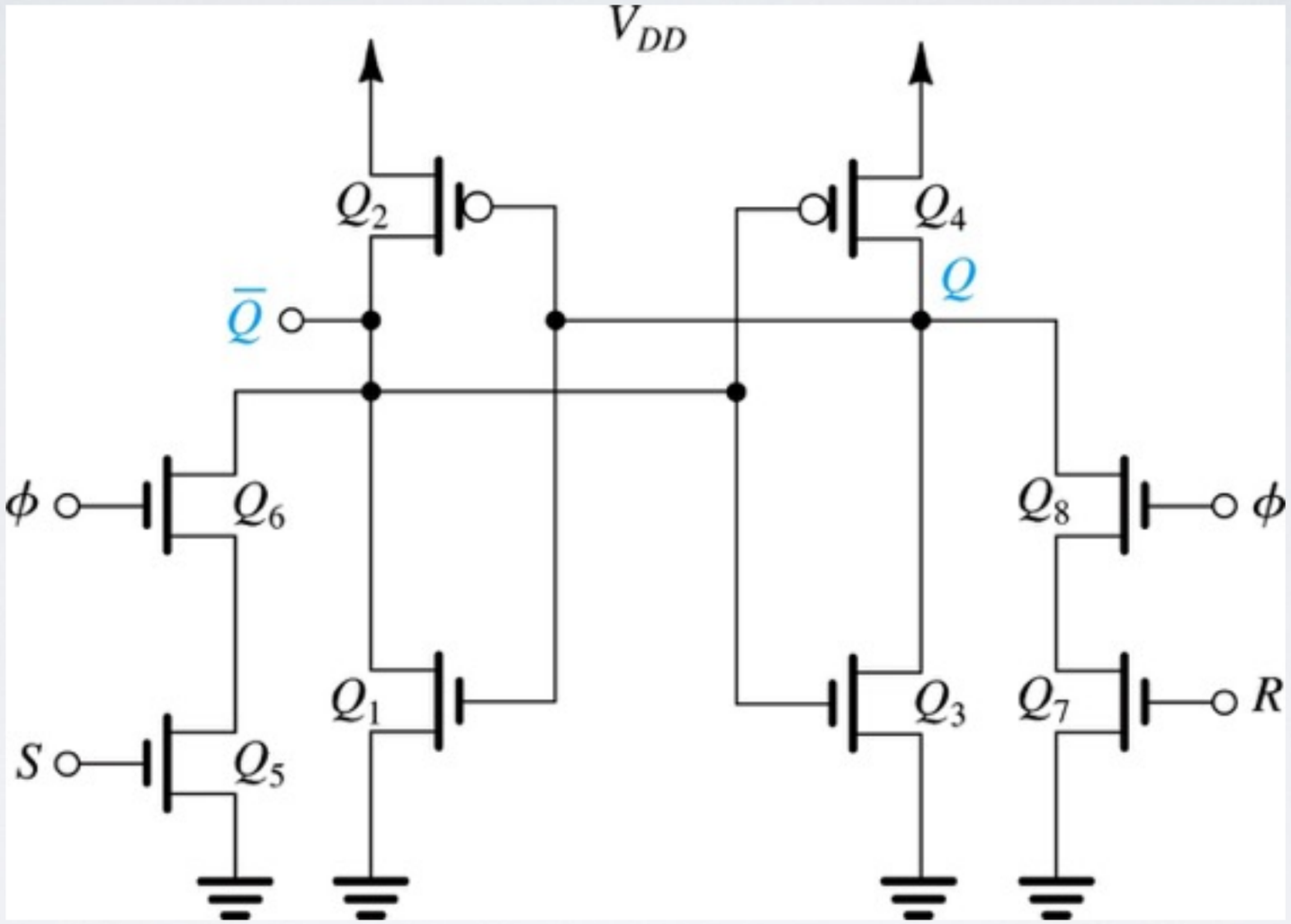


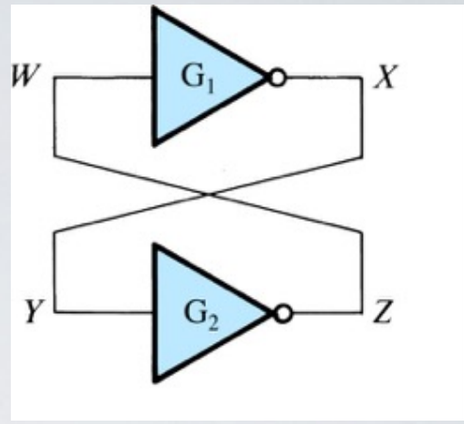
(a)

R	S	Q_{n+1}
0	0	Q_n
0	1	1
1	0	0
1	1	Not used

(b)

Figure 16.3 (a) The set/reset (SR) flip-flop and (b) its truth table.





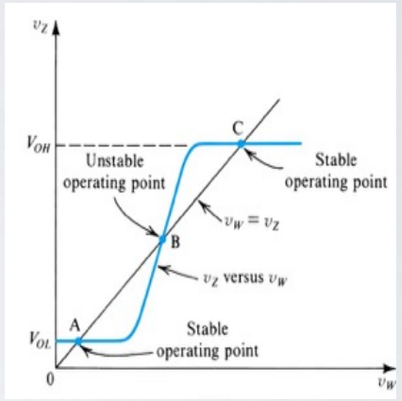


Fig. 16.4 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

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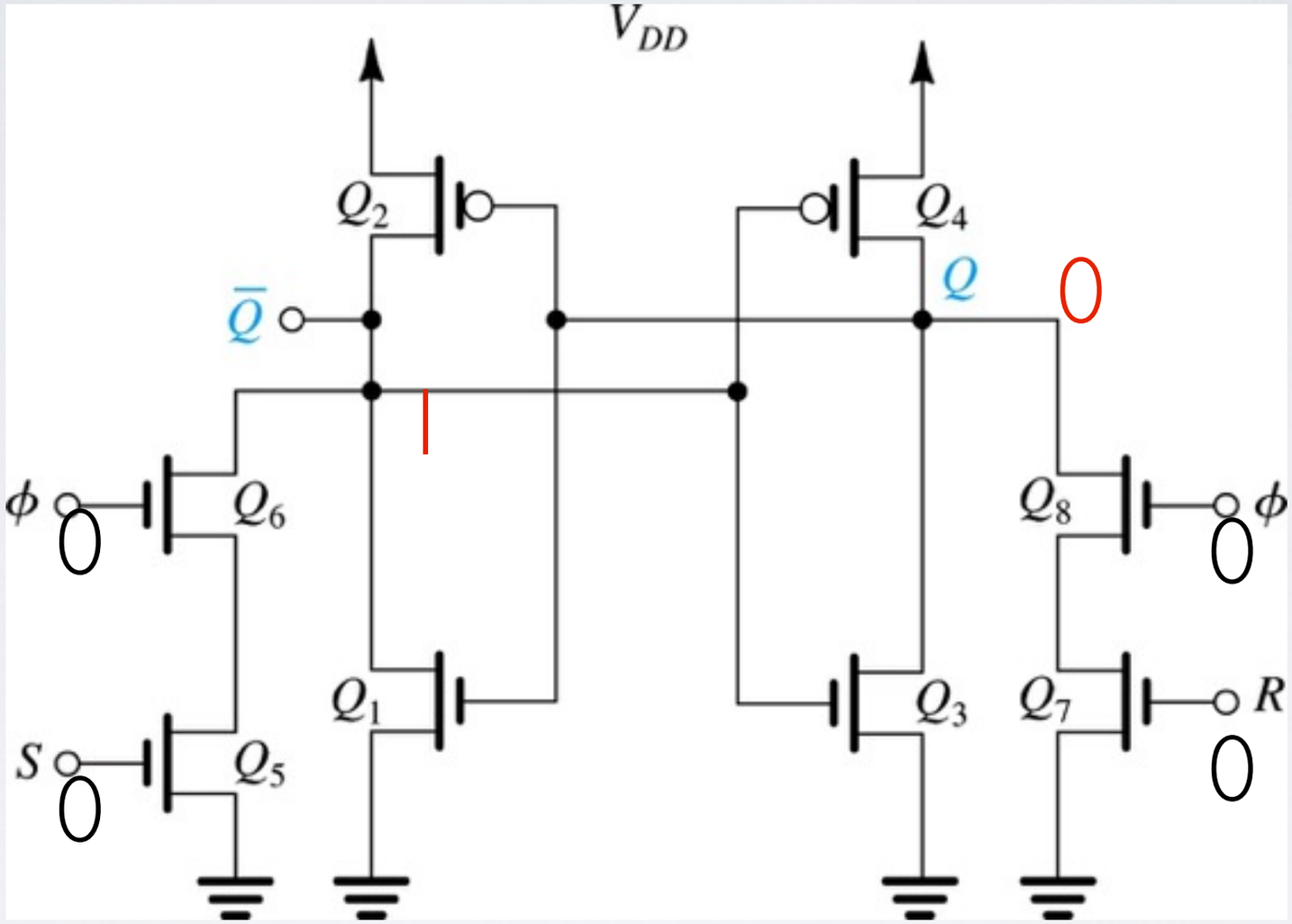
Assume Q=0, Q' = 1



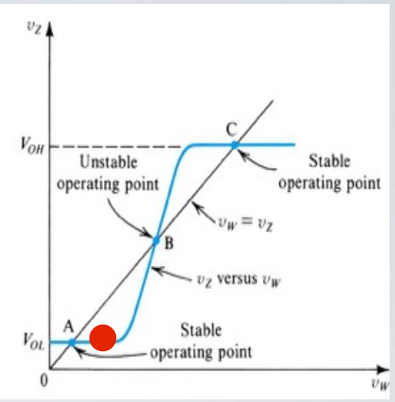


Fig. 16.4 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

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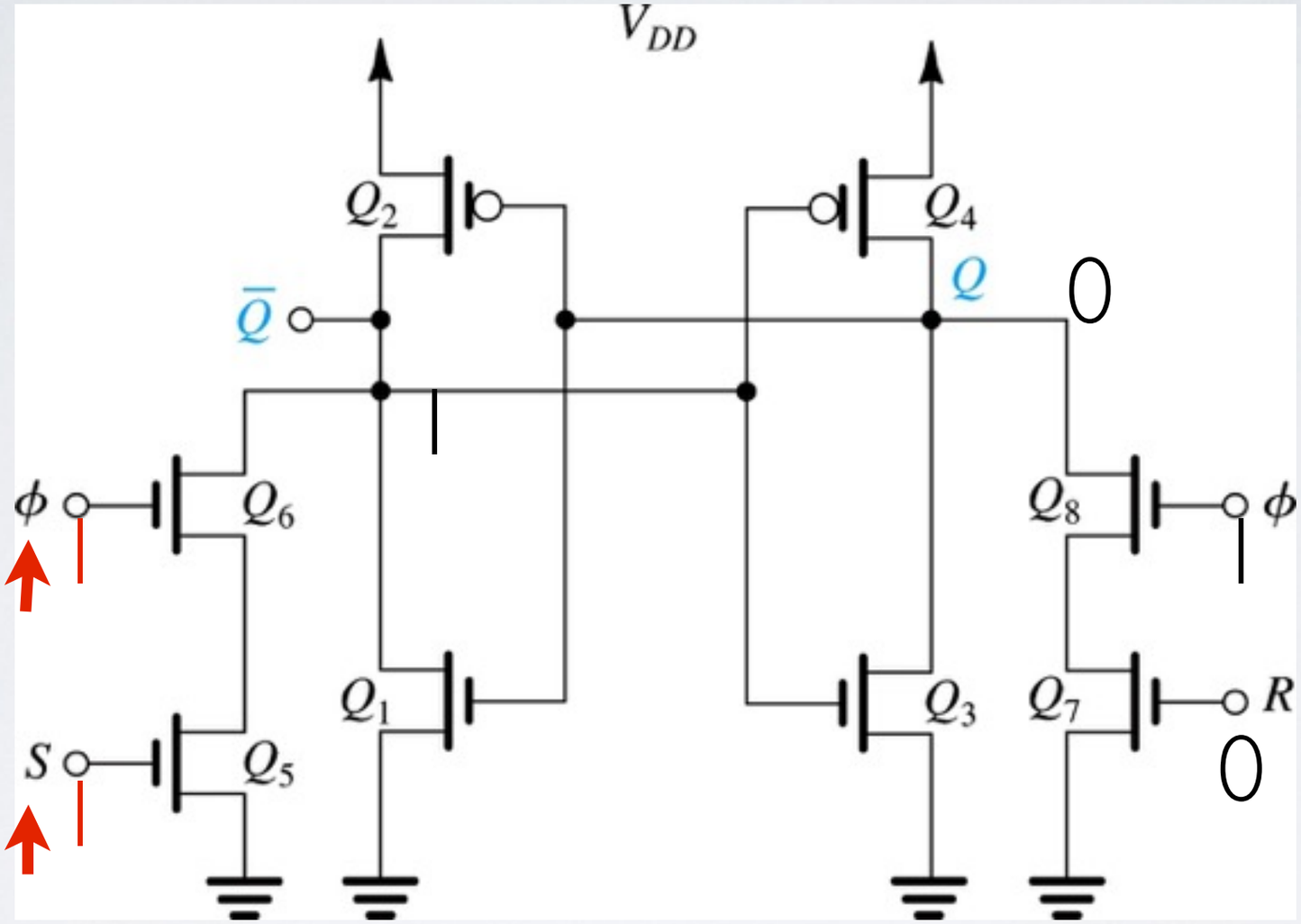
Assume Q=0, Q' = 1
Clock and S go high



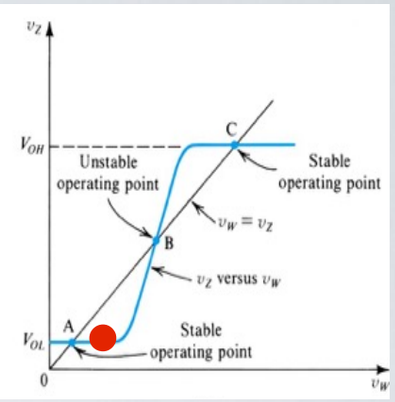


Fig. 16.4 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

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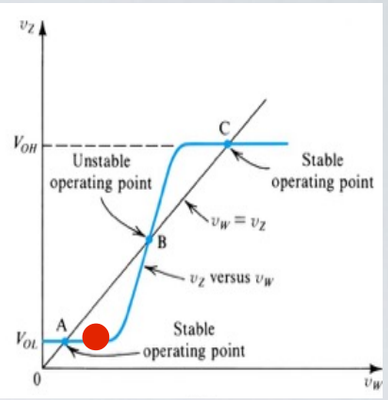
Assume Q=0, Q' = 1
Clock and S go high
Q' is pulled down



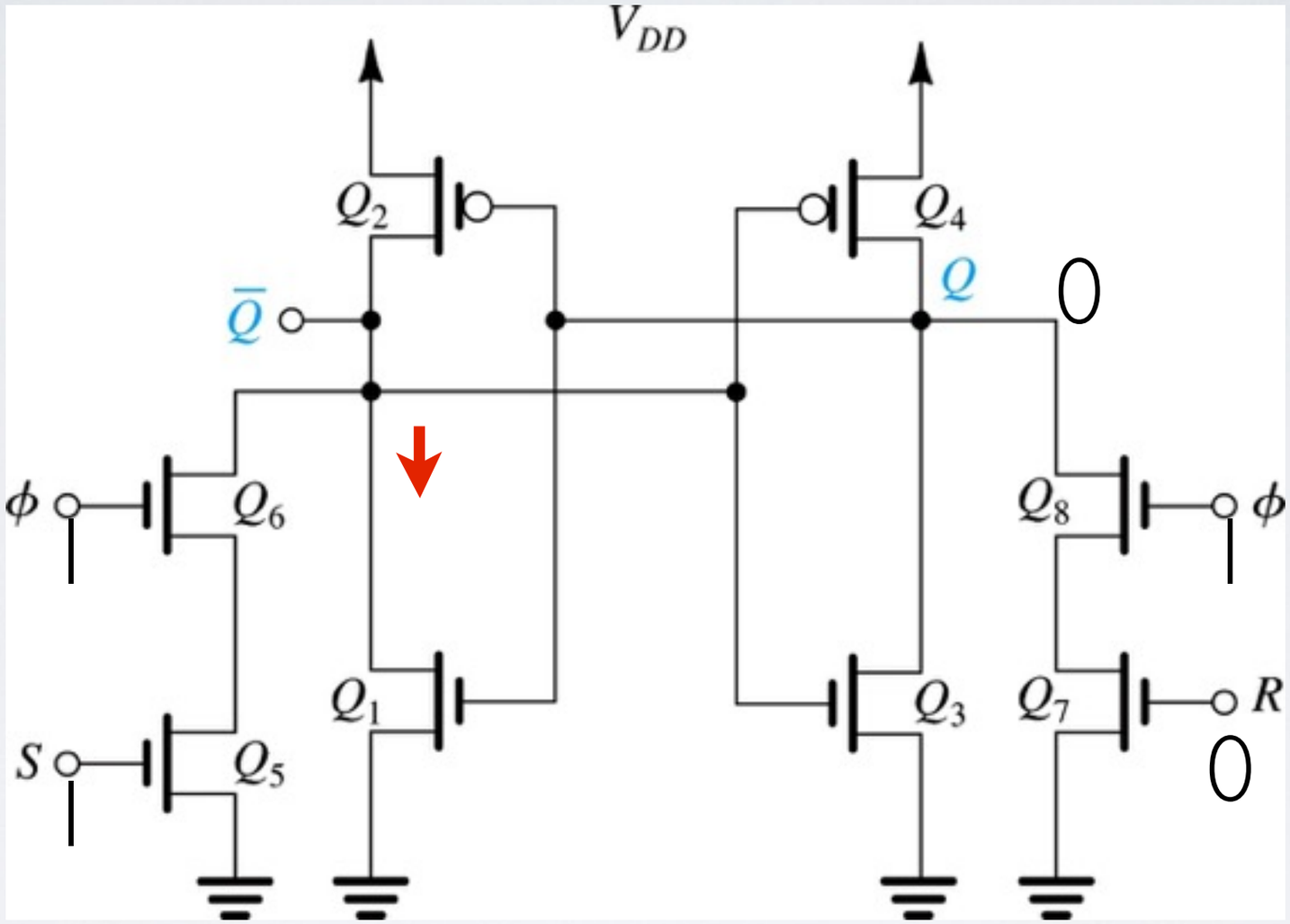


Fig. 16.4 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

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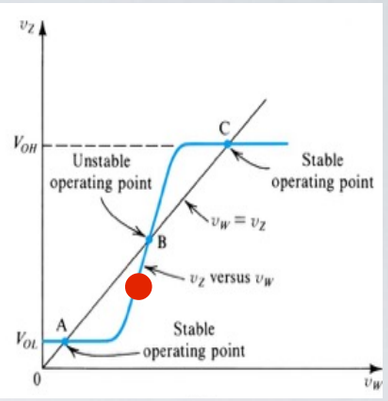
Assume Q=0, Q' = 1
Clock and S go high
Q' is pulled down
voltage at Q increases



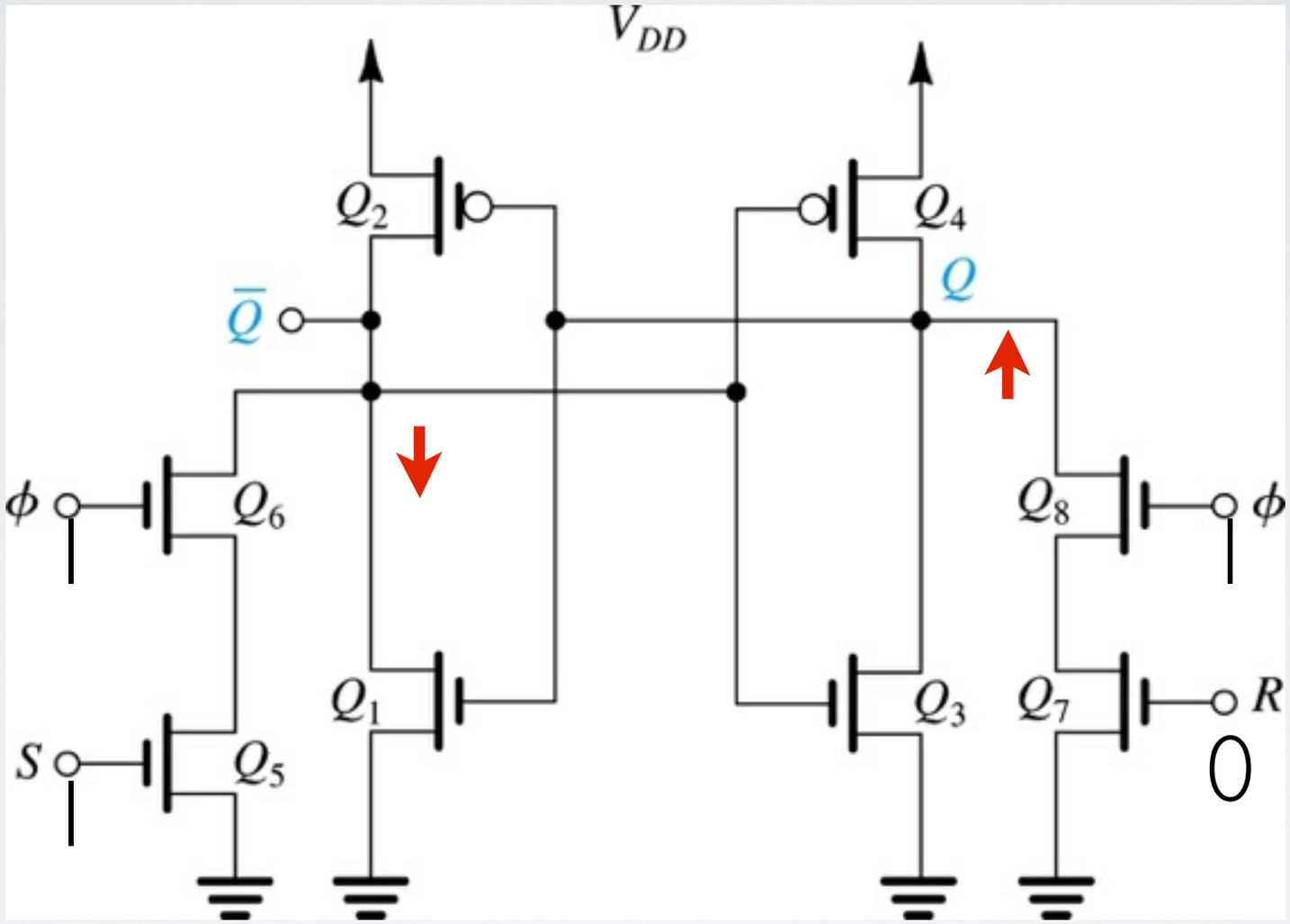


Fig. 16.4 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

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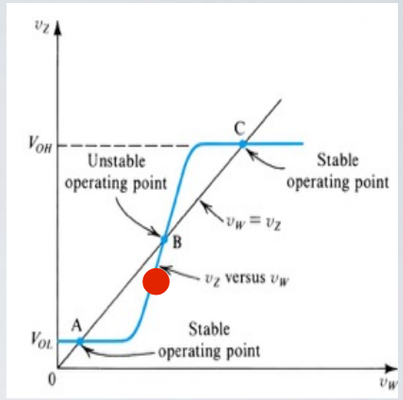
Assume Q=0, Q' = 1
Clock and S go high
Q' is pulled down
voltage at Q increases
Q' reaches critical point



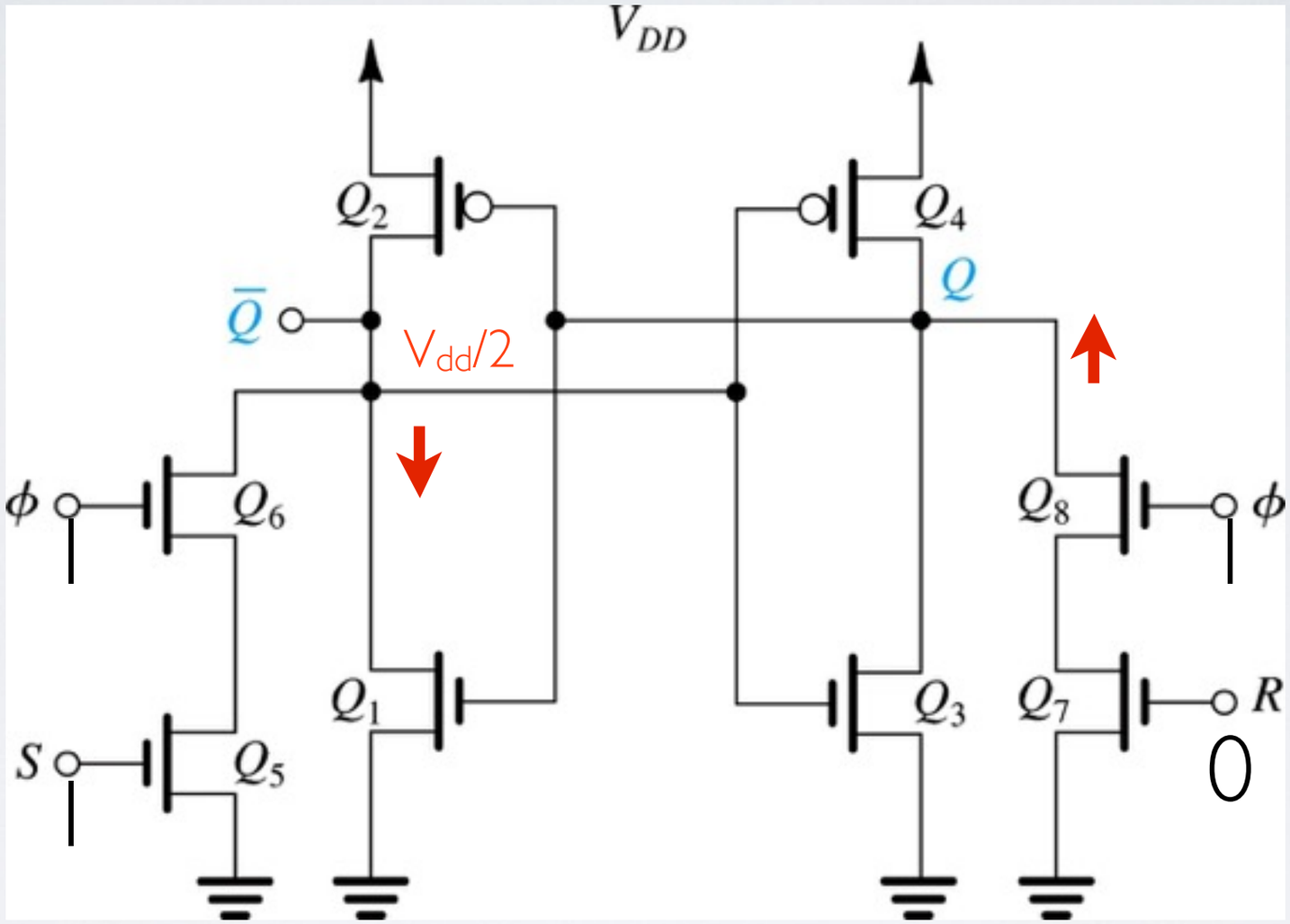


Fig. 16.4 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

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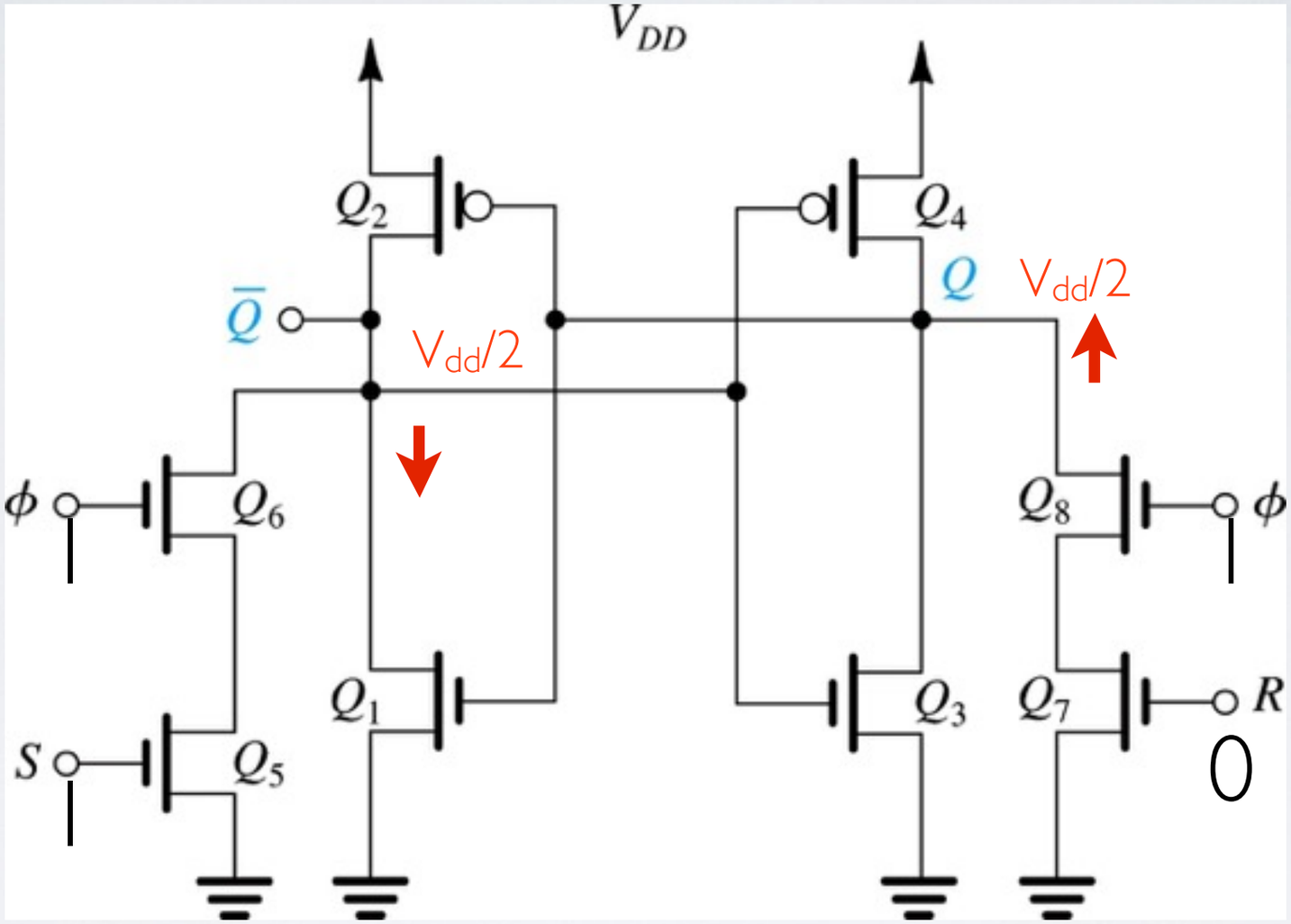
Assume Q=0, Q' = 1
Clock and S go high
Q' is pulled down
voltage at Q increases
Q' reaches critical point
Q reaches critical point



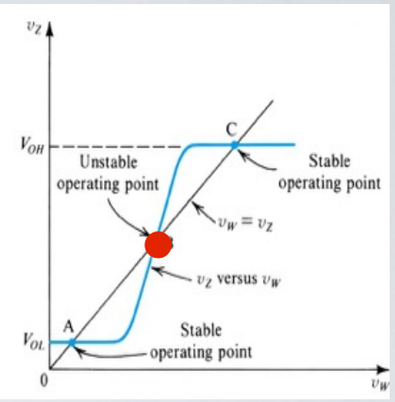


Fig. 16.4 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

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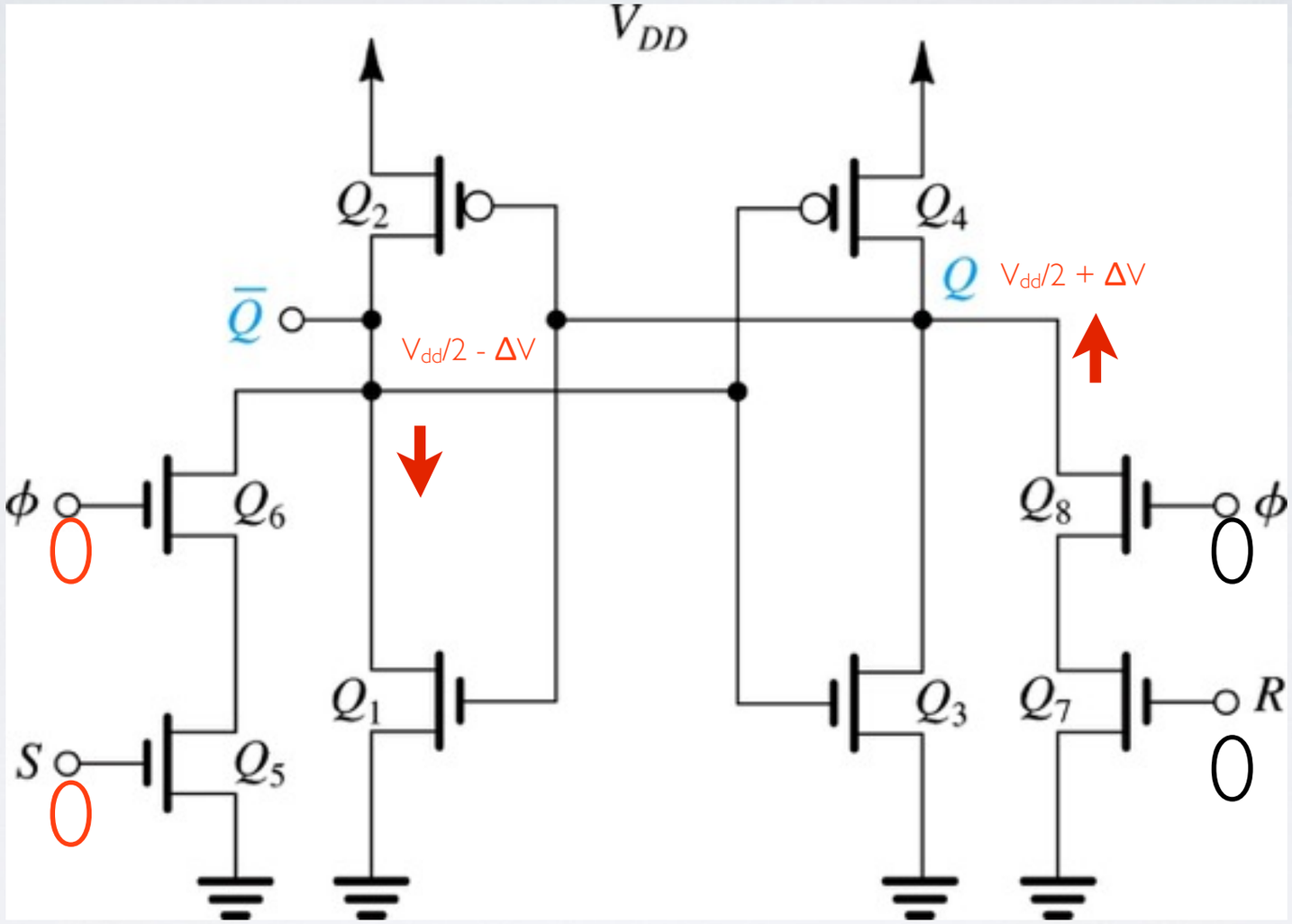
Assume Q=0, Q' = 1
Clock and S go high
Q' is pulled down
voltage at Q increases
Q' reaches critical point
Q reaches critical point
S is be removed



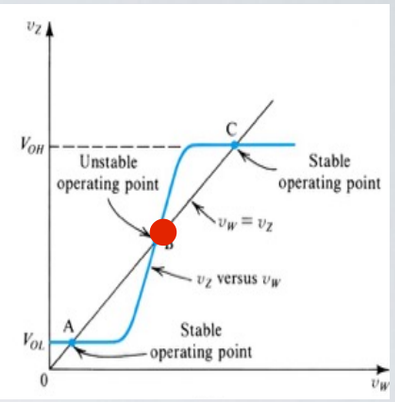


Fig. 16.4 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

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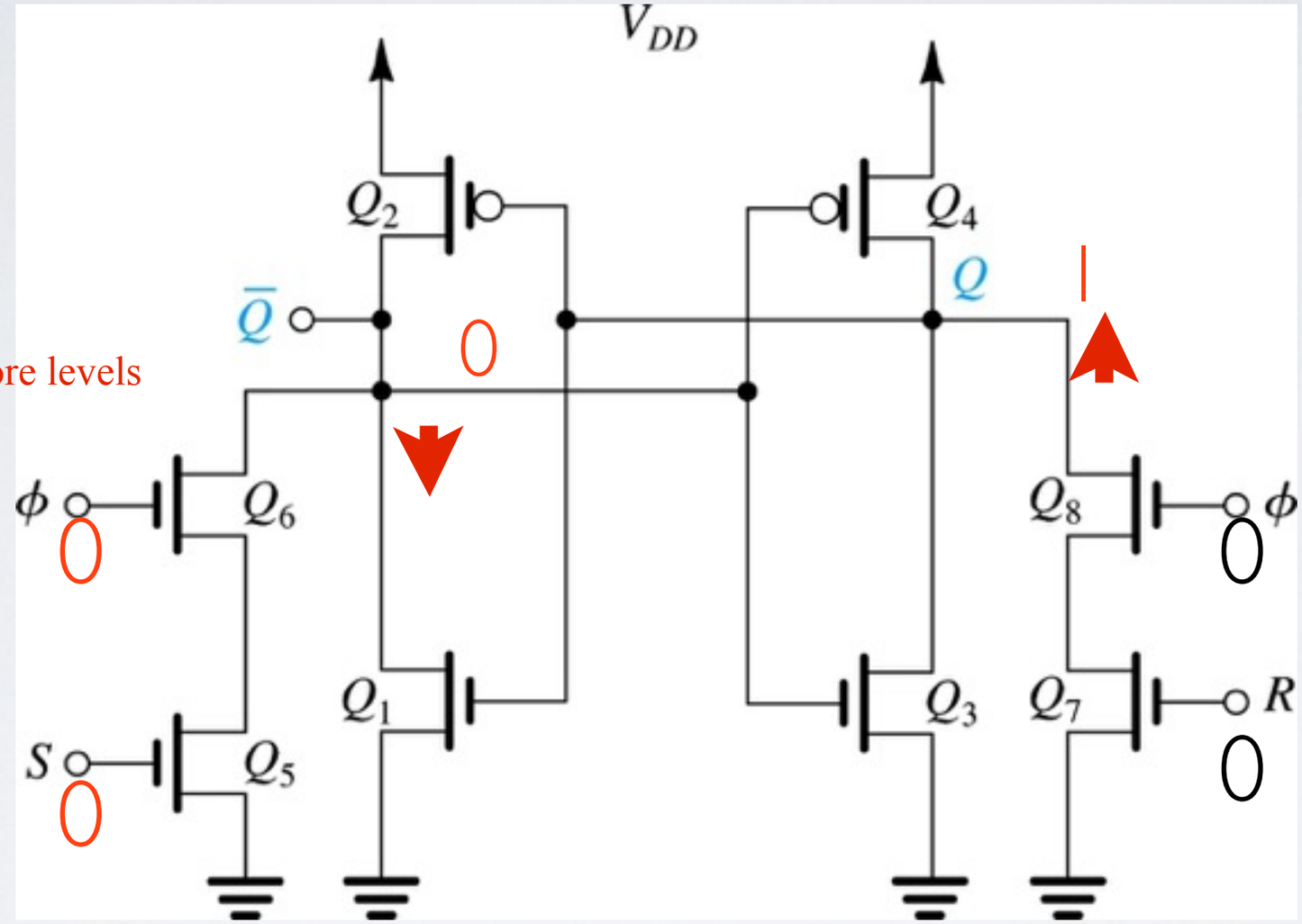
Assume Q=0, Q' = 1
Clock and S go high
Q' is pulled down
voltage at Q increases
Q' reaches critical point
Q reaches critical point
S is be removed
Regenerative action restore levels



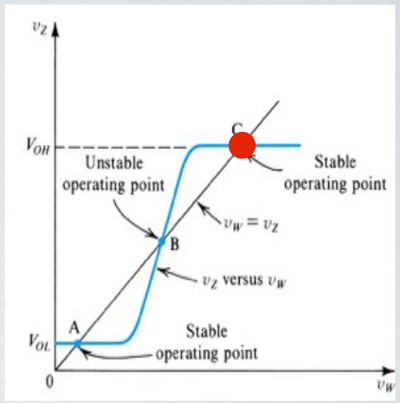


Fig. 16.4 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

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Assume Q=0, Q' = 1
Clock and S go high
Q' is pulled down
voltage at Q increases
Q' reaches critical point
Q reaches critical point
S is be removed
Regenerative action restore levels
FF is SET

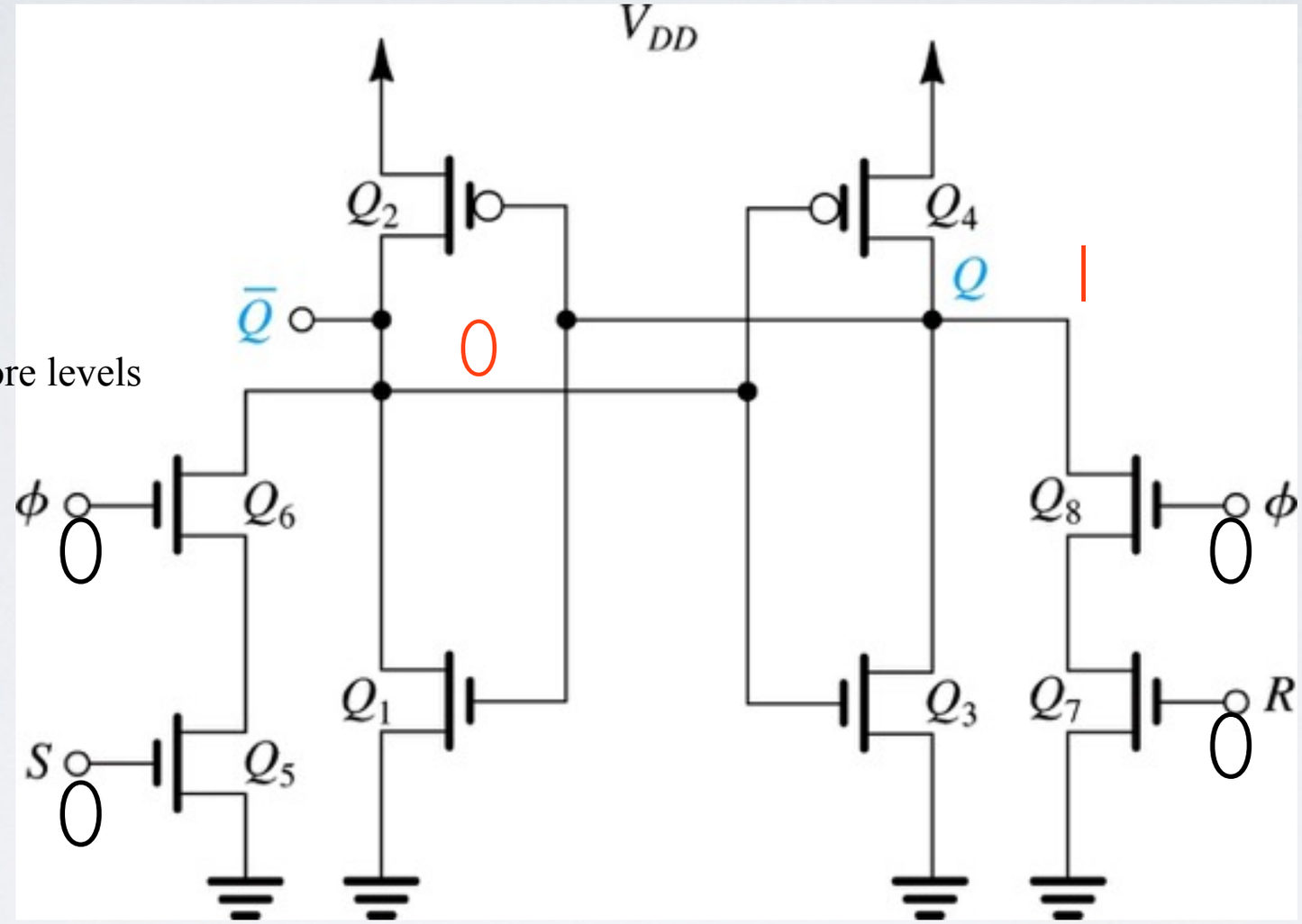

Fig. 16.4 CMOS implementation of a clocked SR flip-flop. The clock signal is denoted by ϕ.

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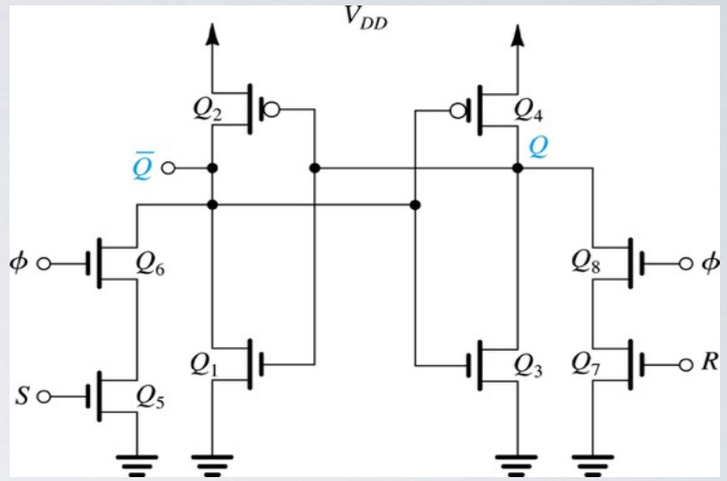
EXAMPLE



The CMOS SR flip-flop in Fig. 16.4 is fabricated in a 0.18-μm process for which $\mu_n C_{ox} = 4\ \mu_p C_{ox} = 300\ \mu A/V^2$, $V_{tn} = |V_{tp}| = 0.5V$, and $V_{DD} = 1.8V$. The inverters have $(W/L)_n = 0.27\mu m/0.18\mu m$ and $(W/L)_p = 4\ (W/L)_n$. The four NMOS transistors in the set-reset circuit have equal W/L ratios.

(a) Determine the minimum value required for this ratio to ensure that the flip-flop will switch.

(b) Also, determine the minimum width the set pulse must have for the case in which the W/L ratio of each of the four transistors in the set-reset circuit is selected at twice the minimum value found in (a). Assume that the total capacitance at each of the Q and Q nodes and ground is **20fF**.

EXAMPLE

$\mu_n C_{ox} = 4\ \mu_p C_{ox} = 300\ \mu A/V^2$, $V_{tn} = |V_{tp}| = 0.5V$, and **$V_{DD} = 1.8V$**. The inverters have **$(W/L)_n = 0.27\mu m/0.18\mu m$** and **$(W/L)_p = 4\ (W/L)_n$**. (a) Determine the minimum value of $(W/L)_{5,6,7,8}$ required to ensure that the flip-flop will switch.

Solution:

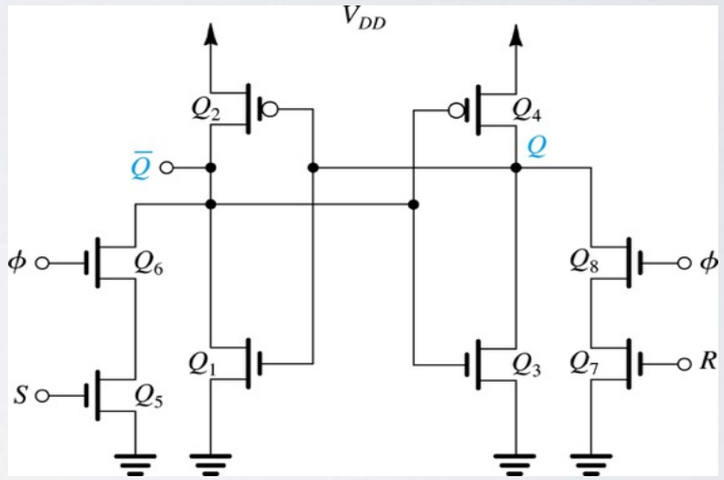
- Assume $Q = 0$ and that you want to *Set* the flip flop
- Replace Q_5 and Q_6 with an equivalent transistor Q_{eq} for which $(W/L)_{eq} = (W/L)_{5,6}/2$
- Assume that v_Q does not change, i.e. remains fixed at $0V$
- Observe that Q_2 operates in triode mode when $V_{\bar{Q}} = V_{DD}/2 = 0.9V$ because $v_{SD,2} = 0.9V < v_{SG_2} - V_{tp} = 1.8V - 0.5V = 1.3V$. Likewise, Q_{eq} operates in triode mode.
- Equate $i_{D,2}$ and $i_{D,eq}$

$$\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_{eq}\left[2(1.3V)0.9V - (0.9V)^2\right] =$$

$$\frac{1}{4}\frac{\mu_n C_{ox}}{2}\left(\frac{0.27\mu m}{0.18\mu m}\right)(4)\left[2(1.3V)0.9V - (0.9V)^2\right]$$

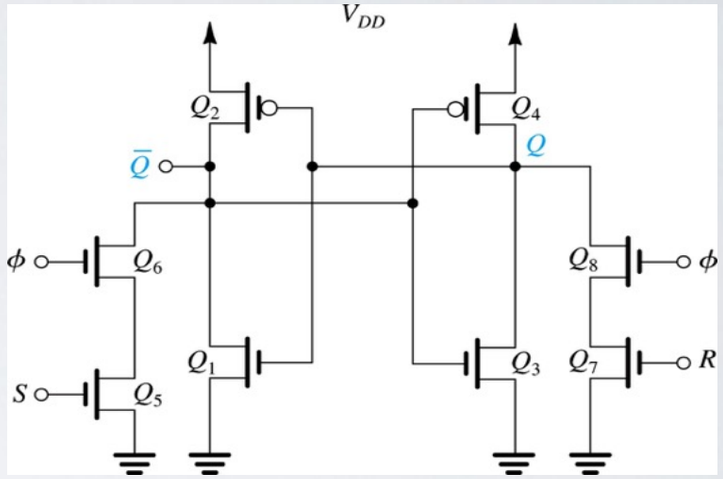
- Simplify to obtain

$$\boxed{\left(\frac{W}{L}\right)_{eq} = \frac{1}{2}\left(\frac{W}{L}\right)_{5,6,7,8} = \frac{0.27\mu m}{0.18\mu m}}$$



EXAMPLE

(b) Also, determine the minimum width the set pulse must have for the case in which the W/L ratio of each of the four transistors in the set-reset circuit is selected at twice the minimum value found in (a). Assume that the total capacitance at each of the Q and Q nodes and ground is **20fF**.



Solution: Set $(W/L)_5 = (W/L)_6 = (W/L)_7 = (W/L)_8 = 1.08um/0.18um$.

Set

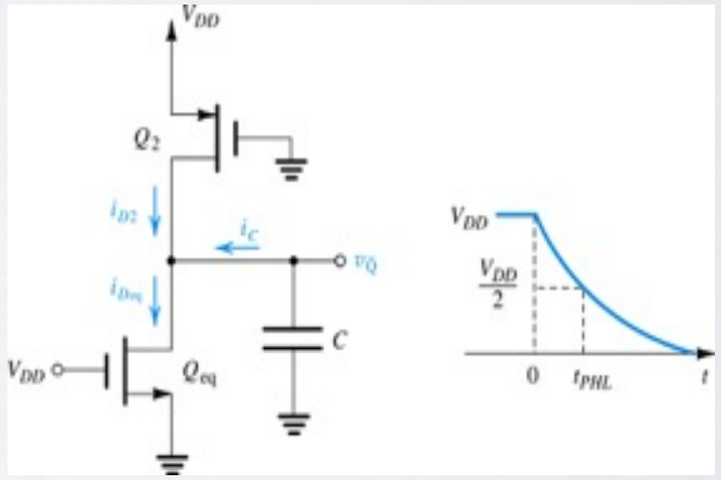
$$t_S = t_{PHL} + t_{PLH}$$

where

t_{PHL} is the time it takes for $v_{Q'}$ to go from V_{DD} to $V_{DD}/2$

and

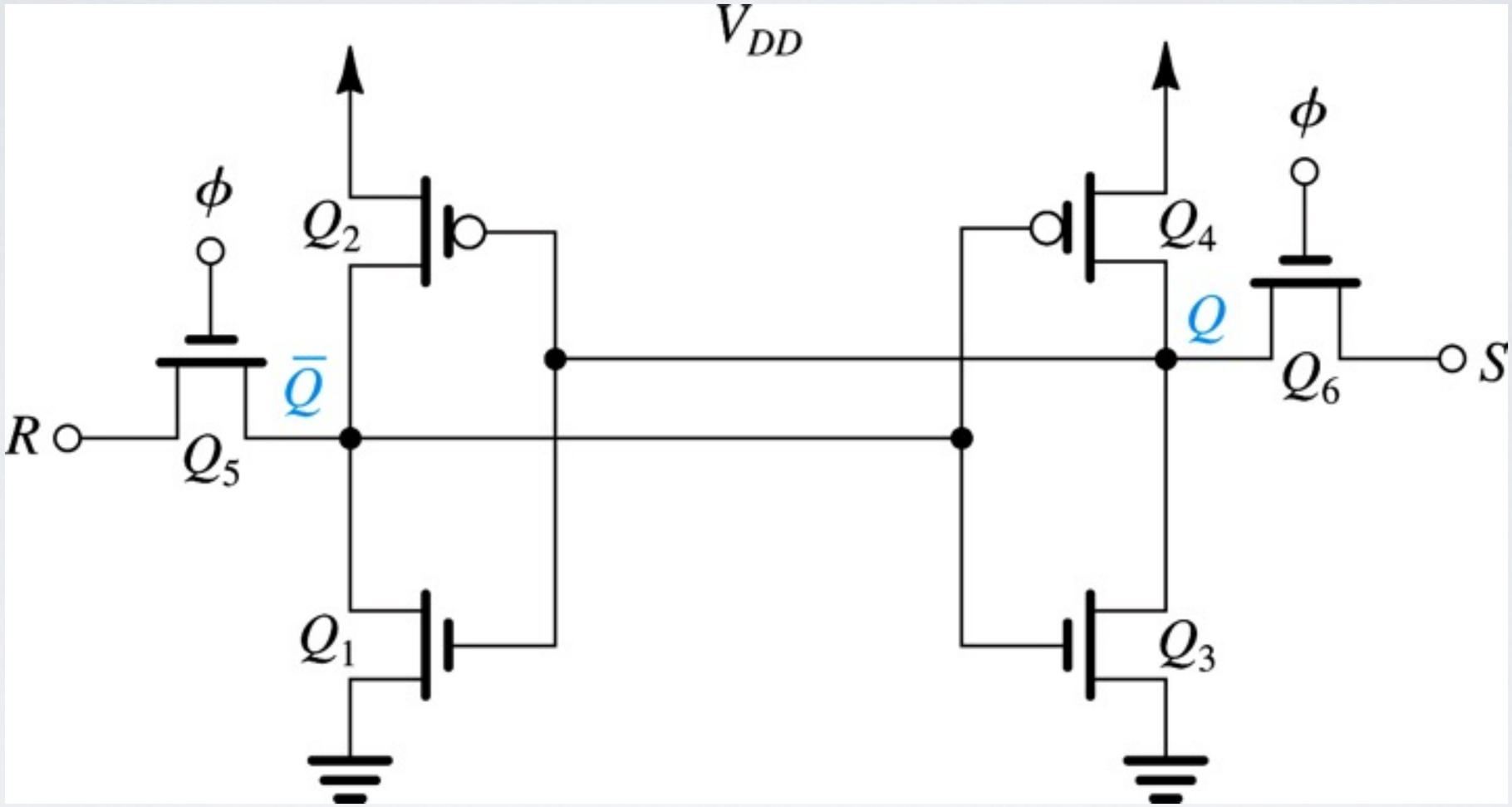
t_{PLH} is the time it takes for v_Q to go from 0V to $V_{DD}/2$



To find t_{PHL}, use $i_C = i_{D,eq} - i_{D2}$. At t = 0, $v_{Q'} = V_{DD}$ and Q_2 is off, Q_{eq} is saturated and $i_{C1} = 760.5uA$. At $t = t_{PHL}$, $v_{Q'} = V_{DD}/2$, $i_{D2} = 344.25uA$, $i_{Deq} = 688.5uA$ and $i_{C2} = 344.25uA$. So $i_{C,AVE} = 552.4uA$ and $t_{PHL} = (20fF)(0.9V)/552\ uA = 32.6ps$.

To find t_{PLH}, you can use the formula from ch. 14 that use α to get $t_{PLH} = 49.5ps$.

$T_{min} = t_{PHL} + t_{PLH} = 82.1ps$



A simpler CMOS implementation of the clocked SR flip-flop. This circuit is popular as the basic cell in the design of static random-access memory (SRAM) chips.

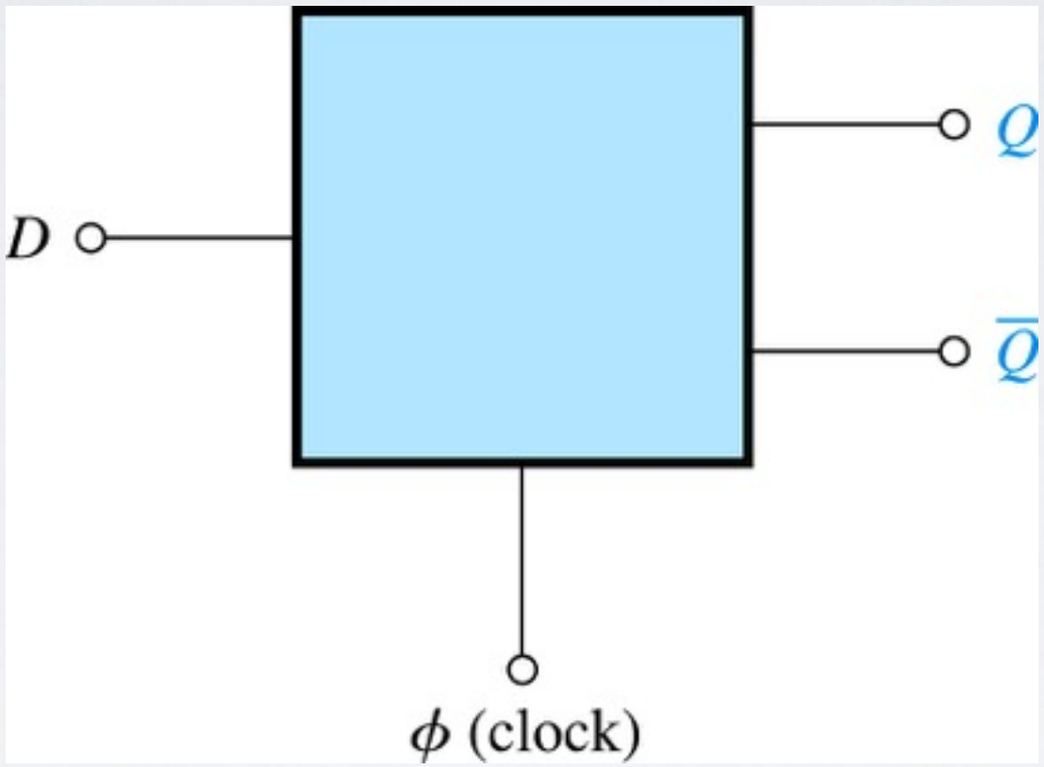


Figure 16.8 A block diagram representation of the D flip-flop.

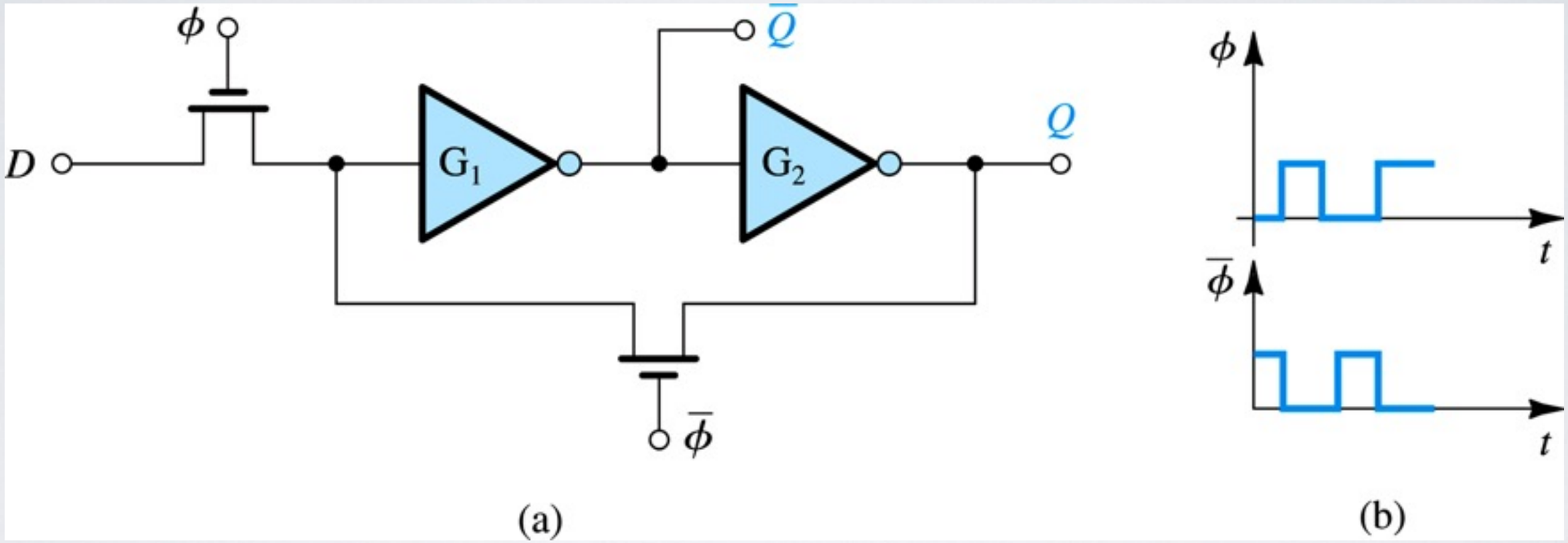


Figure 16.9 A simple implementation of the *D* flip-flop. The circuit in (a) utilizes the two-phase non-overlapping clock whose waveforms are shown in (b).

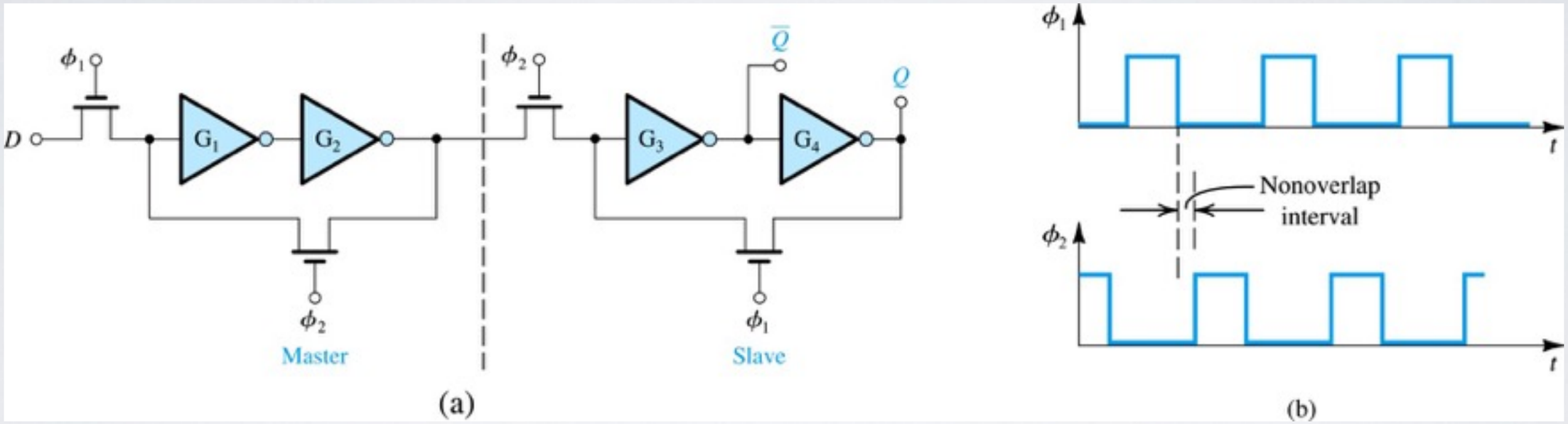


Figure 16.10 (a) A master–slave D flip-flop. The switches can be, and usually are, implemented with CMOS transmission gates. (b) Waveforms of the two-phase non-overlapping clock required.