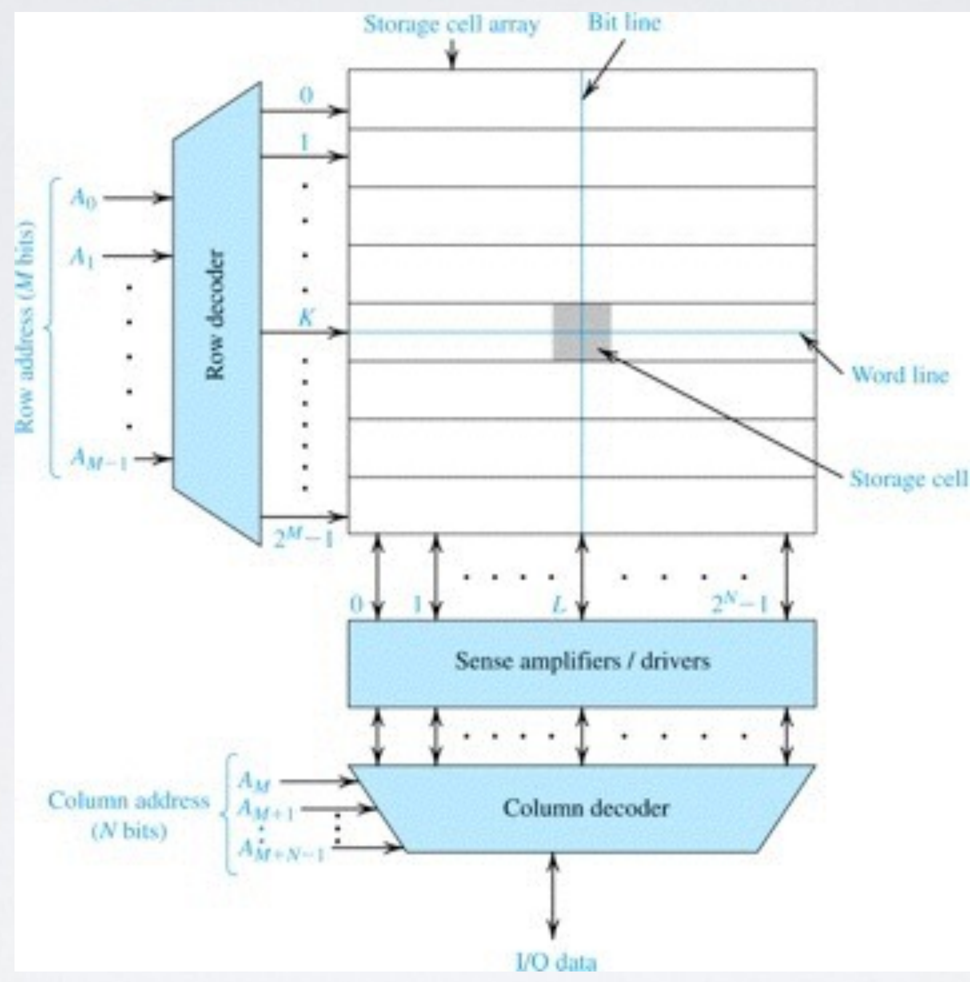
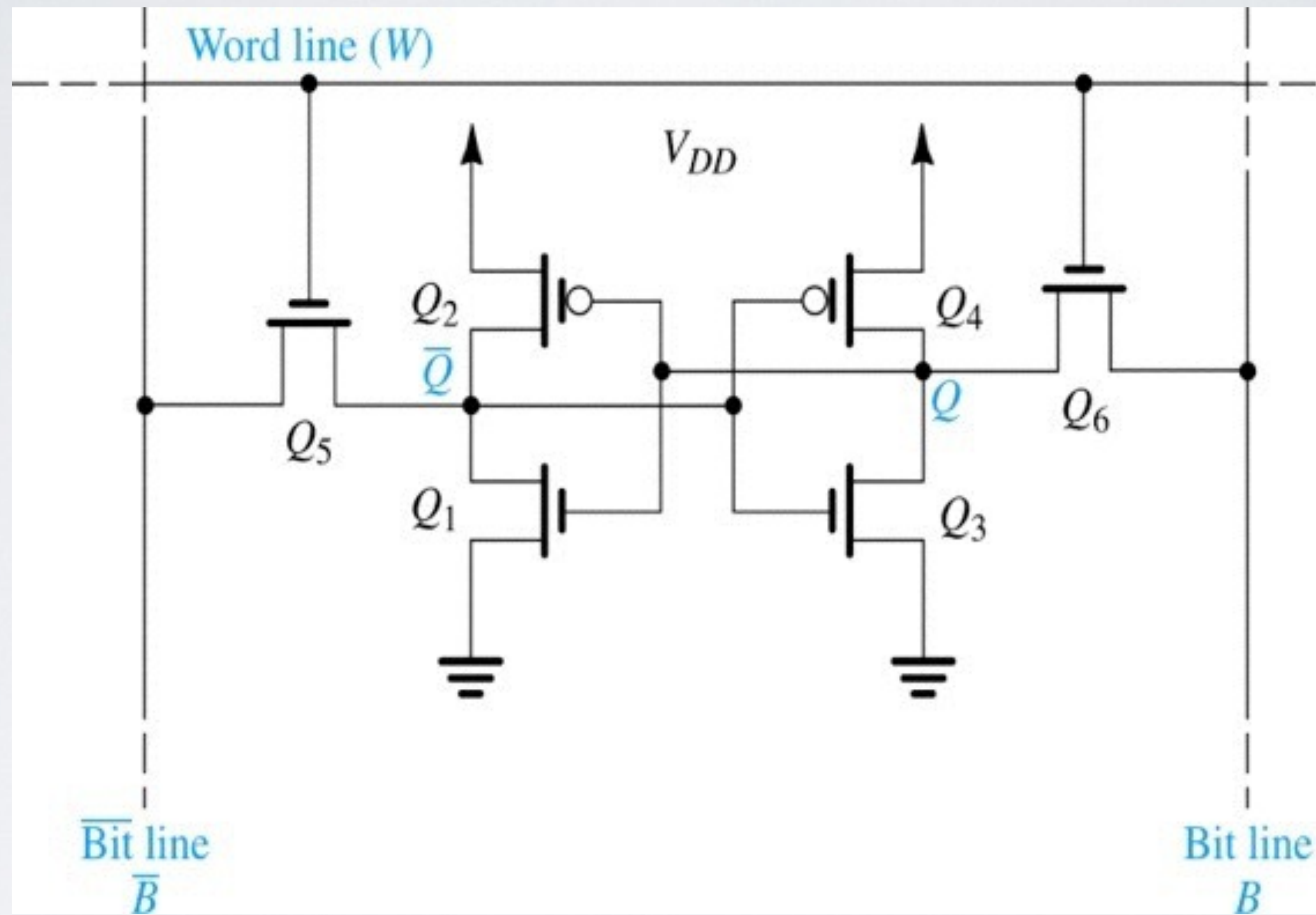
STATIC & DYNAMIC RAMS

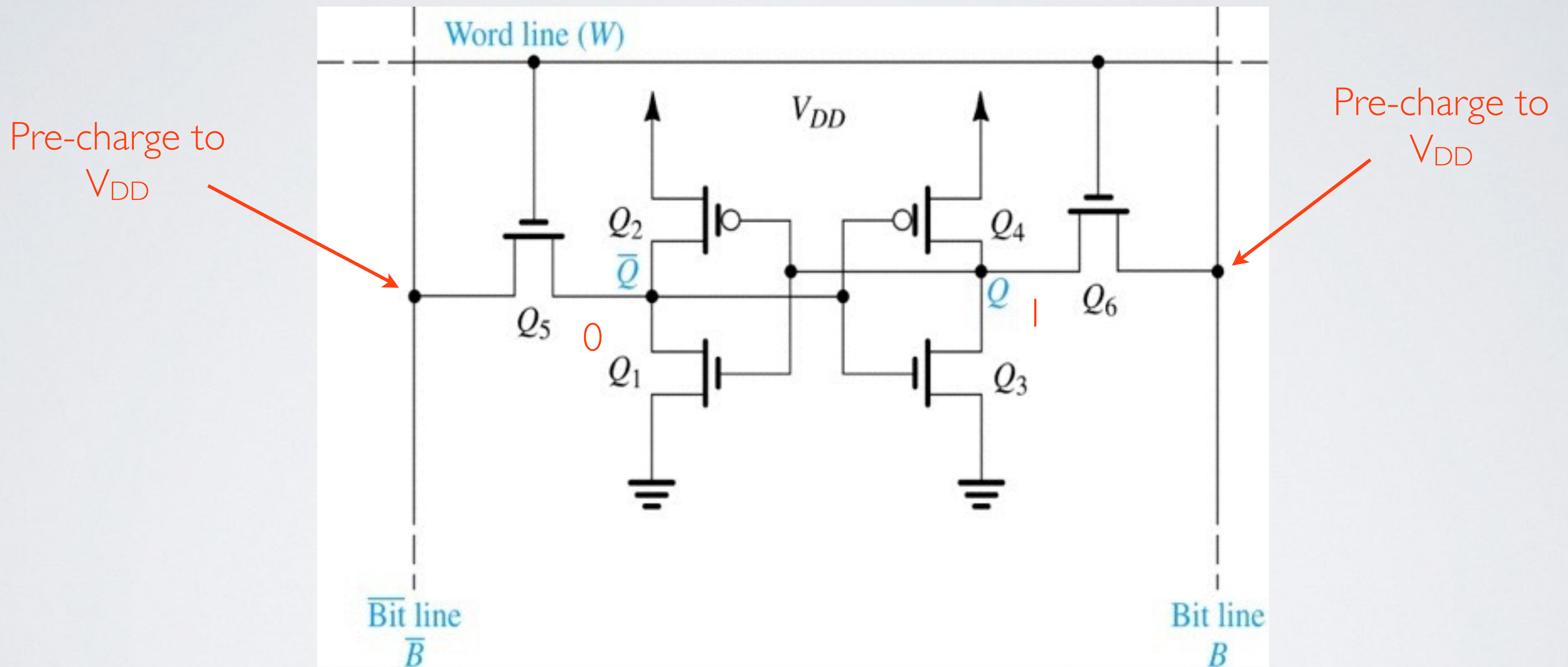
INEL4207 - Digital Electronics - M. Toledo


Storage cell array
Bit line
Row address (M bits)
A_0
A_1
A_{M-1}
Row decoder
0
1
K
2^M-1
Word line
Storage cell
0
1
L
2^N-1
Sense amplifiers / drivers
Column address
(N bits)
A_M
A_{M+1}
A_{M+N-1}
Column decoder
I/O data

READING



READING



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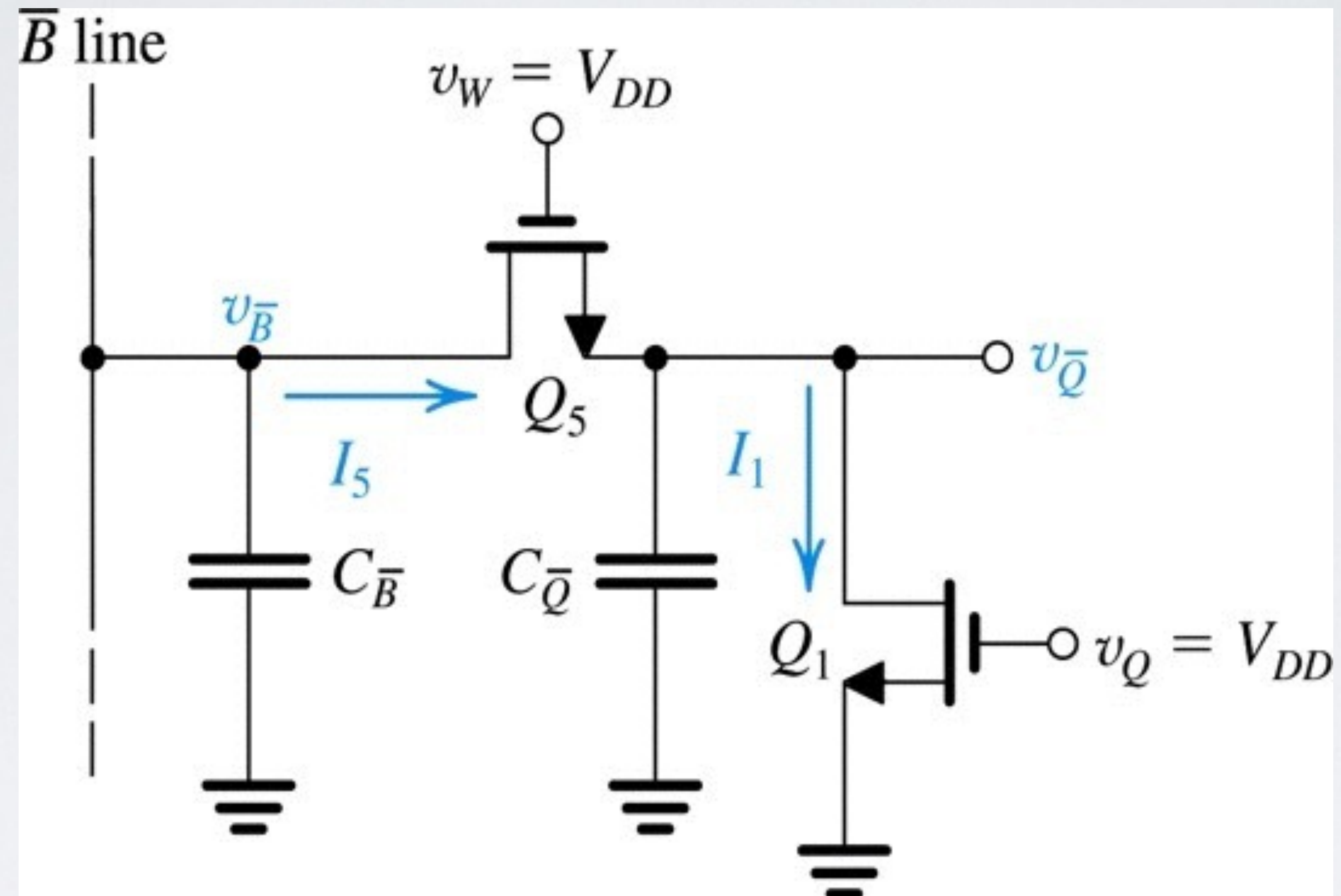

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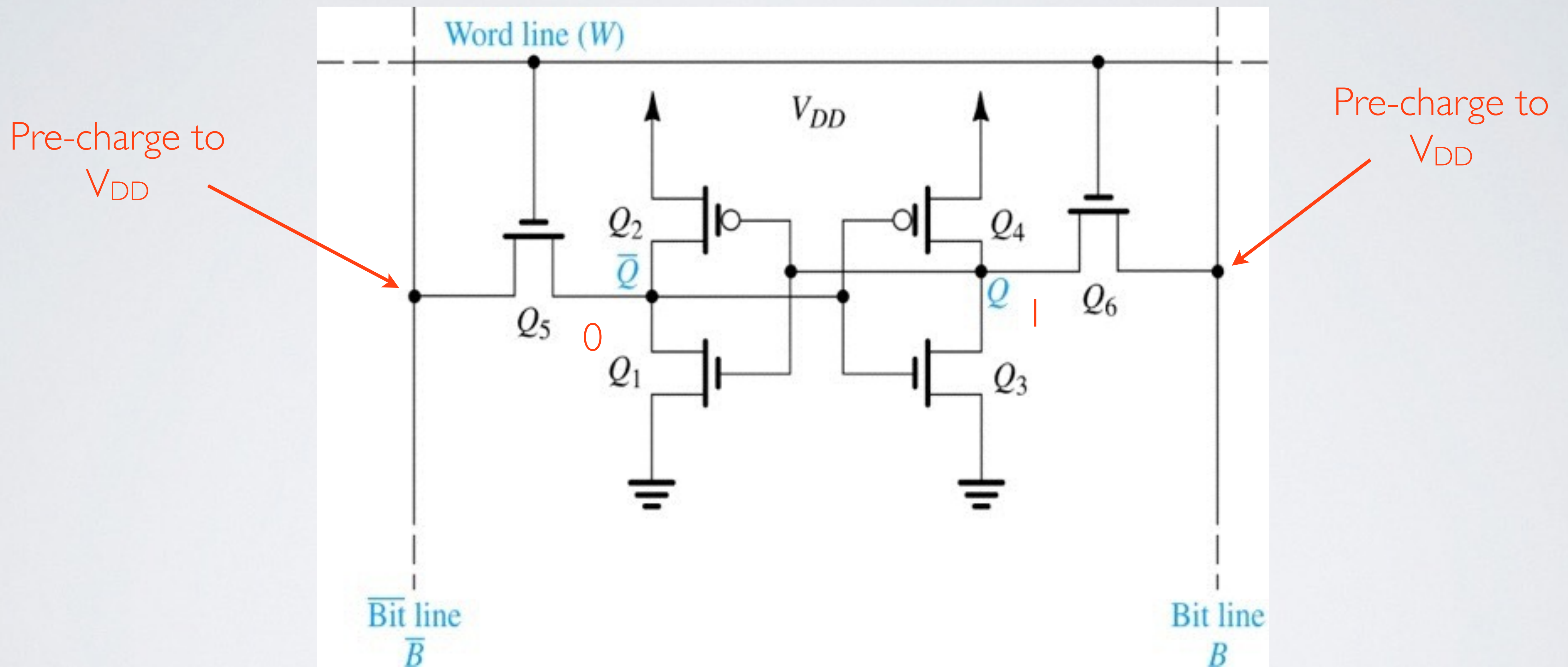

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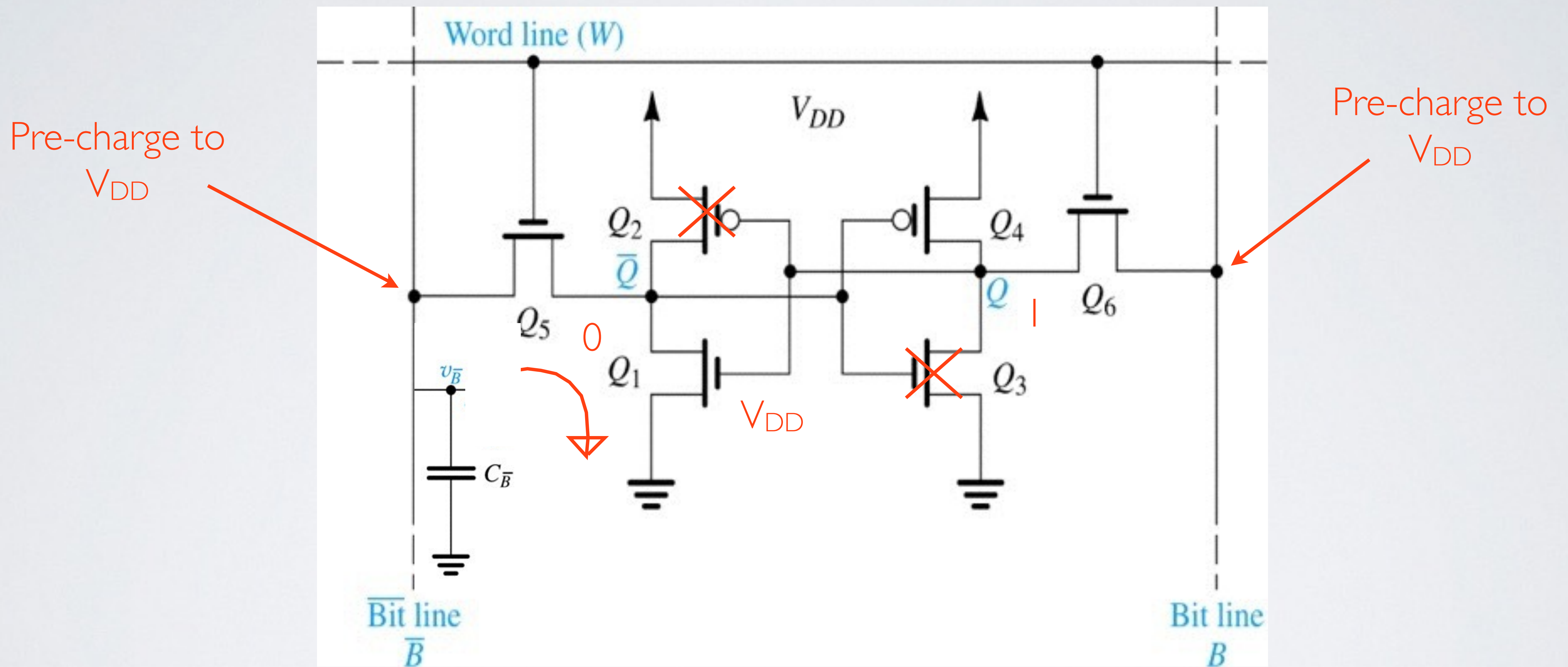


READING

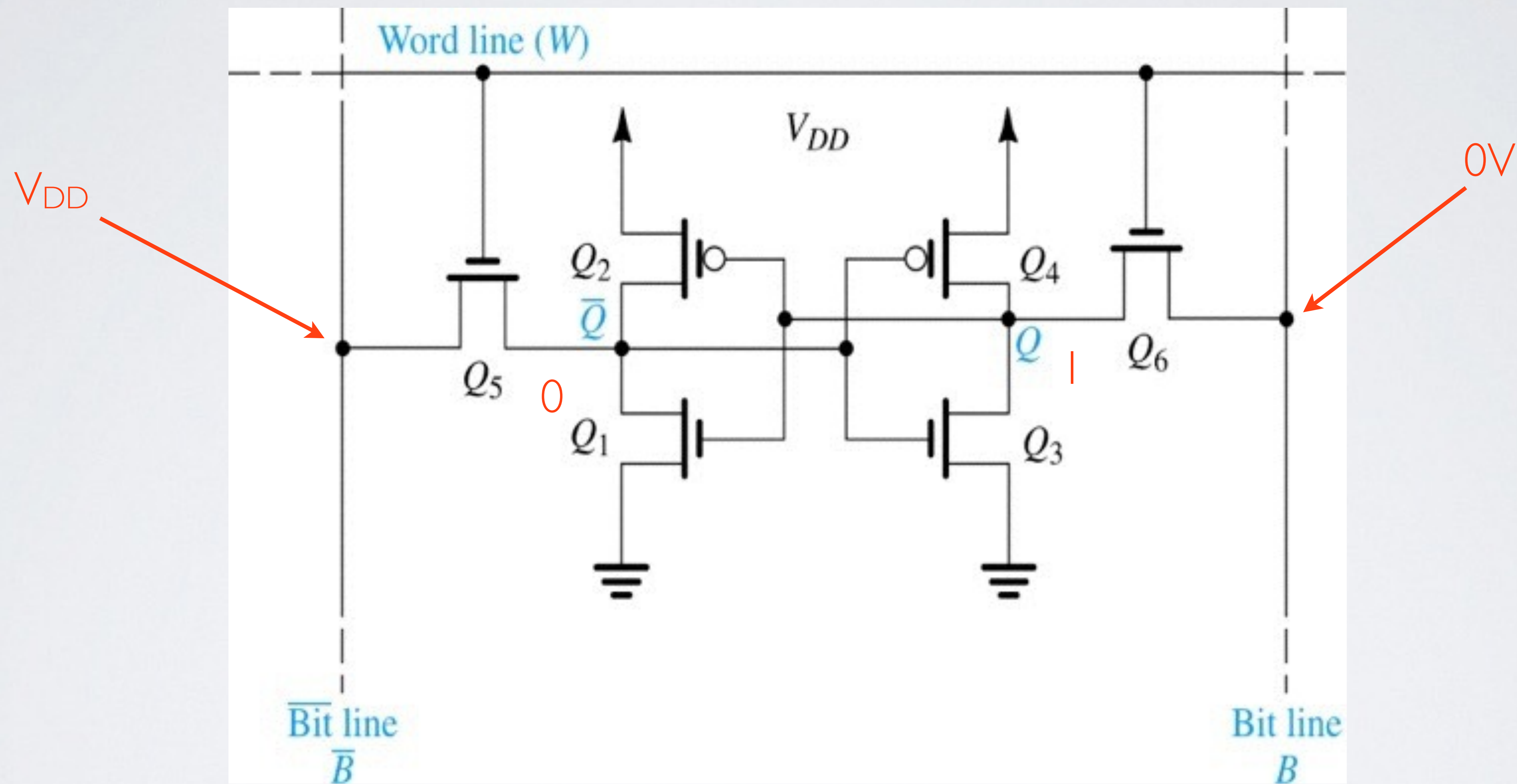
Example

A CMOS SRAM cell shown in the previous slide is fabricated in a 0.18-μm process for which $\mathbf{V_{tn} = |V_{tp}| = 0.5V}$ and $\mathbf{V_{DD} = 1.8V}$. The inverters have $\mathbf{(W/L)_n = 0.27\mu m/0.18\mu m}$. Assume that a cell containing a 1 must be read.

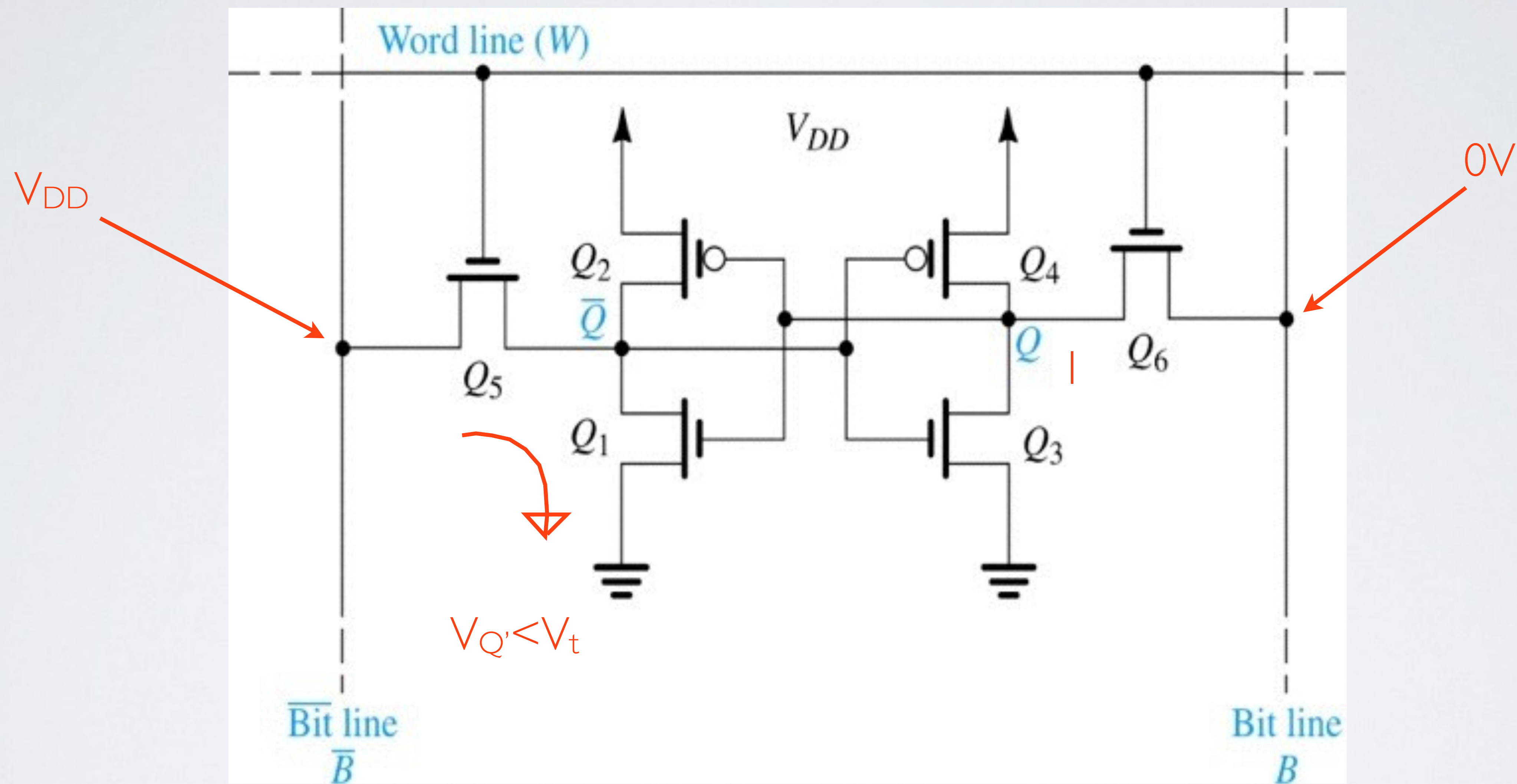
(a) Determine the maximum value of $(W/L)_5$ to ensure that the cell will not change state.

(b) Determine the read delay Δt in two cases: (i) $(W/L)_5 = 2.5$ and (i) $(W/L)_5 = 1.5$. Let $\mu_n C_{ox} = 300\mu A/V^2$, $C_{\mathbf{B'}} = 2pF$, and the minimum change in voltage required by the sense amplifier be $\Delta V = 0.2V$.

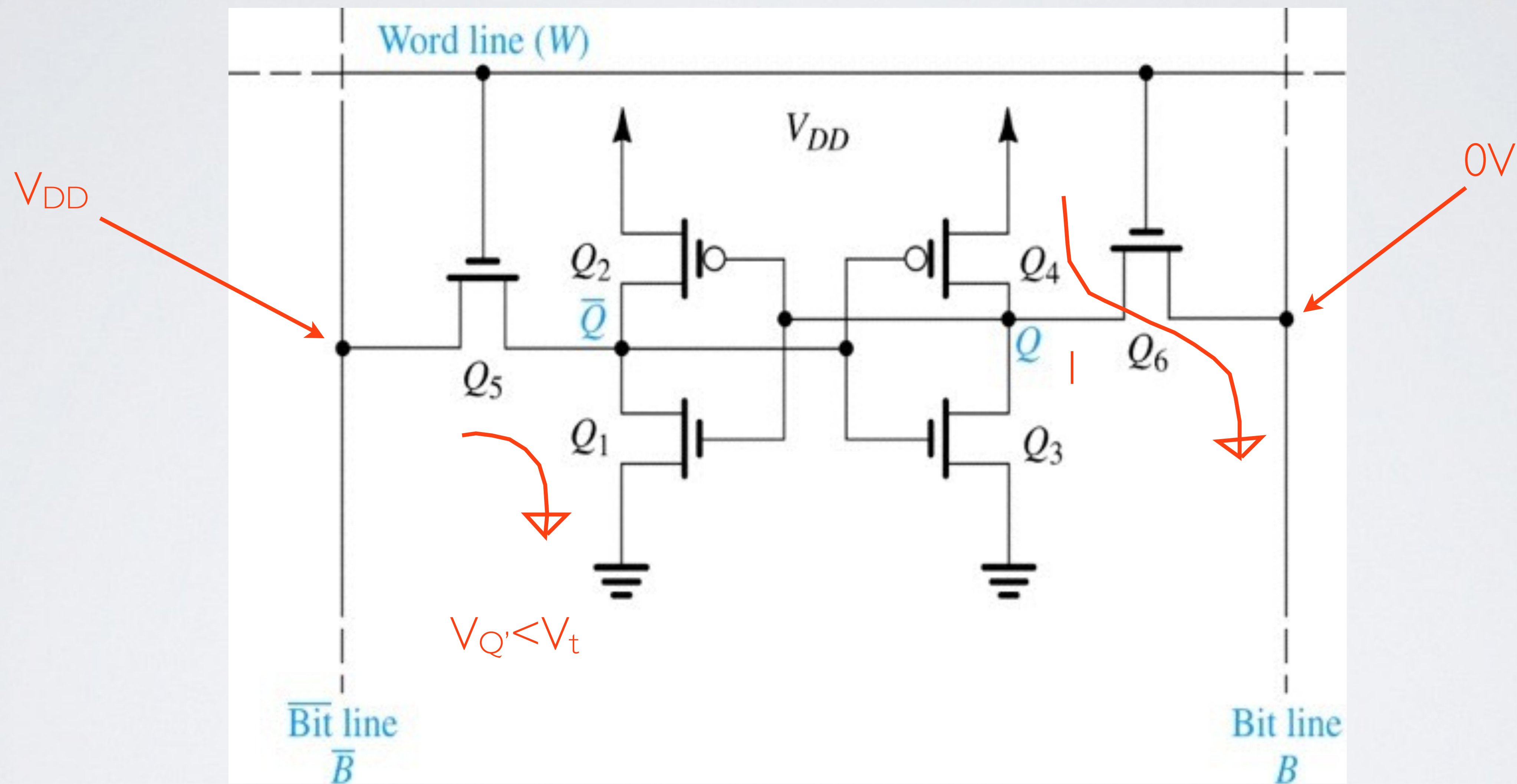
WRITING



WRITING



WRITING



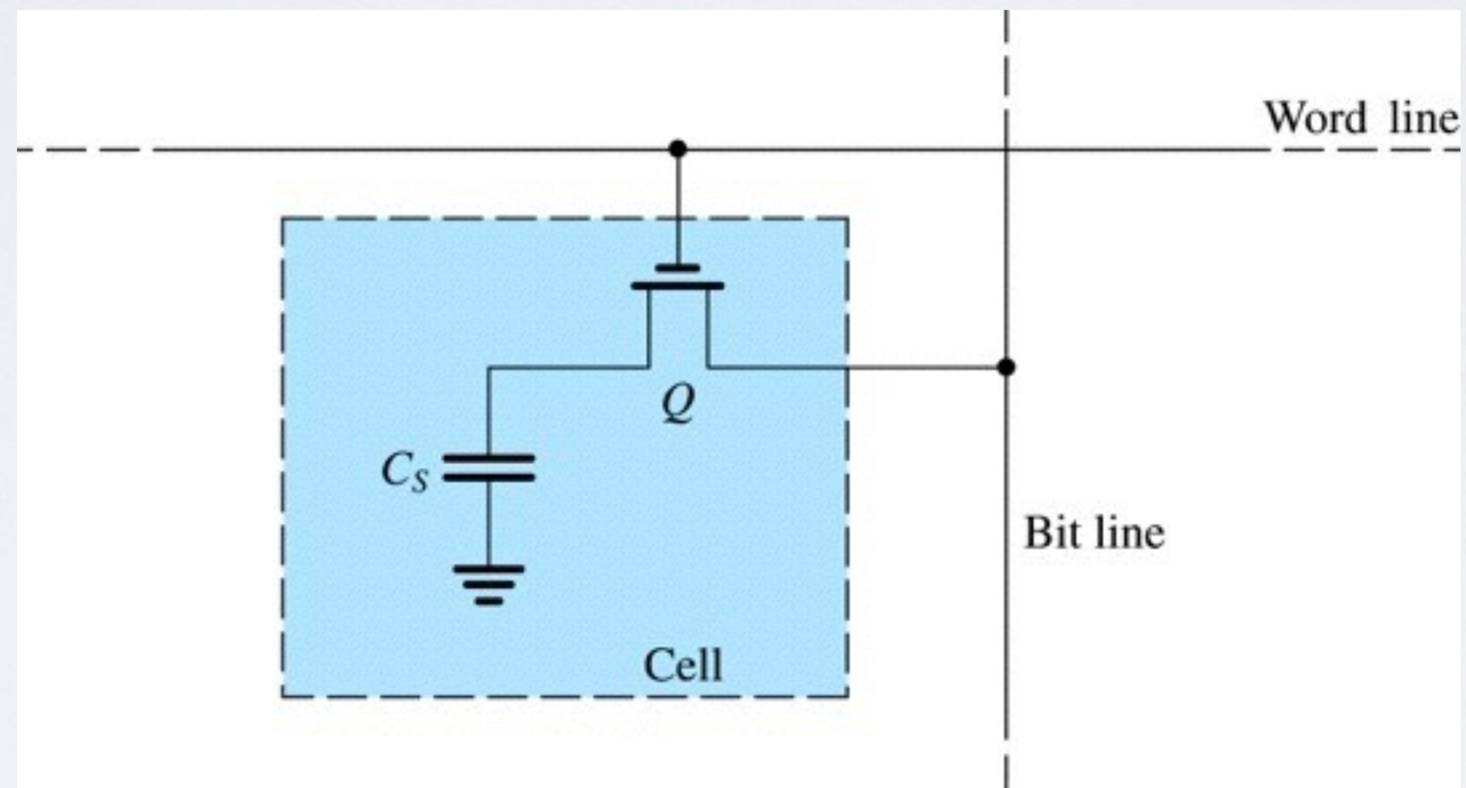
$\therefore$ Select $(W/L)_4$ so that $V_Q < V_t$

WRITING

Example

A 0 must be stored on the SRAM cell described in the previous example, which initially contains a 1. Determine the maximum value of $(W/L)_4$ needed to ensure that the cell will change state.

DYNAMIC RAM



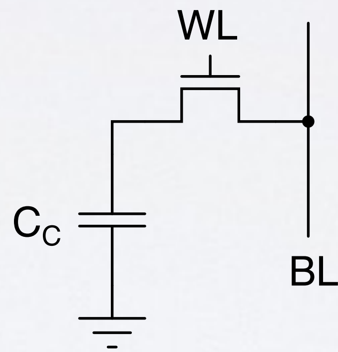
$$C_S V_{CS} + C_B \frac{V_{DD}}{2} = (C_B + C_S)\left(\frac{V_{DD}}{2} + \Delta V\right)$$

$$\Delta V = \frac{C_S}{C_B + C_S}\left(V_{CS} - \frac{V_{DD}}{2}\right)$$

Figure 16.19 When the voltage of the selected word line is raised, the transistor conducts, thus connecting the storage capacitor C_S to the bit-line capacitance C_B.

1. (25 points) For the following dynamic RAM circuit. $C_C = 50fF$, $V_{DD} = 5V$, and $V_t = 1.4V$ (including body effect). There are n cells connected to the bit line, and each cell represents a capacitive load on the bit line of $2fF$. The sense amplifier and other circuitry attached to the bit line has a $20fF$ capacitance, so that the total bit line capacitance is $2n + 20$, in fF.

   Consider a reading process in which the bit line is pre-charged to a voltage of $V_{DD}/2$. What is the maximum number of cells that can be attached to a bit line while ensuring a minimum change on the bit line voltage, once steady state is reached, of $0.1V$?



ANSWER: The bit line capacitance is $C_{BL} = n \times 2fF + 20fF$. Due to charge sharing,

$$V_f\left(C_{BL} + C_C\right) = 2.5V \times C_{BL} + V_{i,C} \times C_C$$

where $V_{i,C}$ represents the initial voltage in the cell.

Let $V_f = 2.5V + \Delta V$ and consider a cell containing a logic-1, so that $V_{i,C} = 5V - 1.4V = 3.6V$. then

$$\Delta V\left(C_{BL} + C_C\right) = 2.5V \times C_{BL} + V_{i,C} \times C_C - 2.5V\left(C_{BL} + C_C\right)$$

$$\Delta V\left(C_{BL} + C_C\right) = 2.5V \times C_{BL} + V_{i,C} \times C_C - 2.5V \times C_{BL} - 2.5V \times C_C$$

$$0.1V\left(n \times 2fF + 20fF\right) = \left(3.6V - 2.5V - 0.1V\right) \times 50fF$$

$$n = \frac{10 \times 50fF - 20fF}{2fF} = 240$$

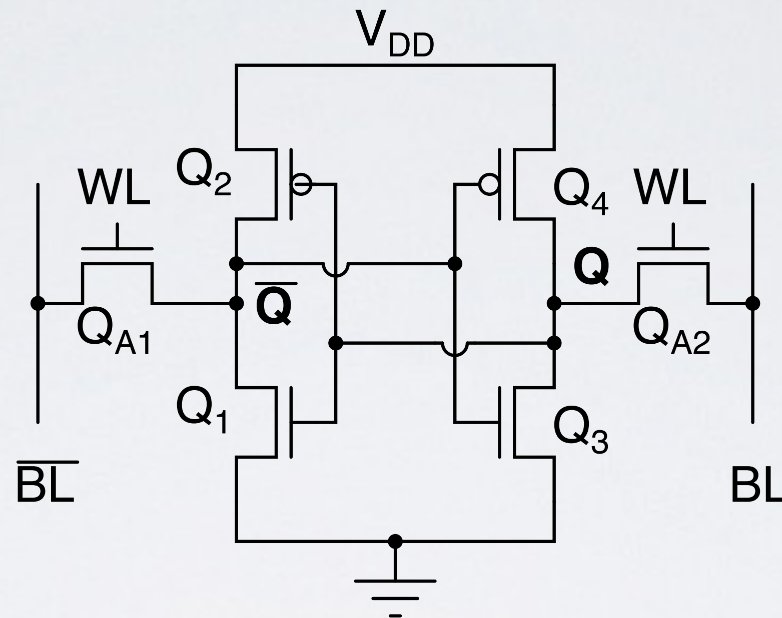
Now repeat, but this time consider a cell containing a logic-0. The procedure is similar, but $V_{i,C} = 0V$.

$$-0.1V\left(n \times 2fF + 20fF\right) = -2.4V \times C_C$$

$$n = \frac{24 \times 50fF - 20fF}{2fF} = 590$$

So $n = \boxed{240}$.

2. (25 points) For the following static RAM circuit, $(W/L)_{1,3} = 2/1$ and $(W/L)_{A1,A2} = 4/5$, $V_{DD} = 3.3V$, $\mu_n C_{OX} = 4\mu_p C_{OX} = 300\mu A/V^2$, $V_{t0} = 0.6V$ for NMOS transistors and $V_{t0} = -0.6V$ for PMOS transistors, $\gamma = 0.5\sqrt{V}$ and $2\phi_F = 0.6V$.



Use the average current method to determine the minimum time needed to read the cell if a change $\Delta V_{BL} = 100mV$ is needed by a sense amplifier. The bit line capacitance is $C_{BL} = 0.1pF$ and a logic-0 is stored in the cell. Assume that the bit line was pre-charged with $3.3V$ and that during the reading process V_Q remains at or below the threshold voltage. Neglect the cell's internal capacitances.

ANSWER: The voltage reduction happens when current flows through Q_{A2} and Q_3. Assume $v_{DS,3} \leq 0.6V$ so that the cell's data is not disturbed. We can use the average current method. At point 1, V_{Q3} is very close to $0V$, Q_{A2} operates in saturation mode, and

$$i_1 = \frac{300\mu A/V^2}{2}\left(\frac{4}{5}\right)(3.3V - 0.6V)^2 = 875\mu A$$

At point 2, $V_{Q3} = 0.6V$. Thus, Q_3 and Q_{A2} operate in triode and saturation mode, respectively, and

$$V_{t,A1} = 0.6V + (0.5\sqrt{V})\left(\sqrt{0.6V + 0.6V} - \sqrt{0.6V}\right) = 0.76V$$

$$I_2 = \frac{300\mu A/V^2}{2}\left(\frac{4}{5}\right)(3.3V - 0.6V - 0.76V)^2 = 452\mu A$$

The average current is $(452\mu A + 875\mu A)/2 = 663\mu A$ and

$$\Delta t = 0.1pF \times \frac{0.1V}{663\mu A} \simeq \boxed{15ps}$$

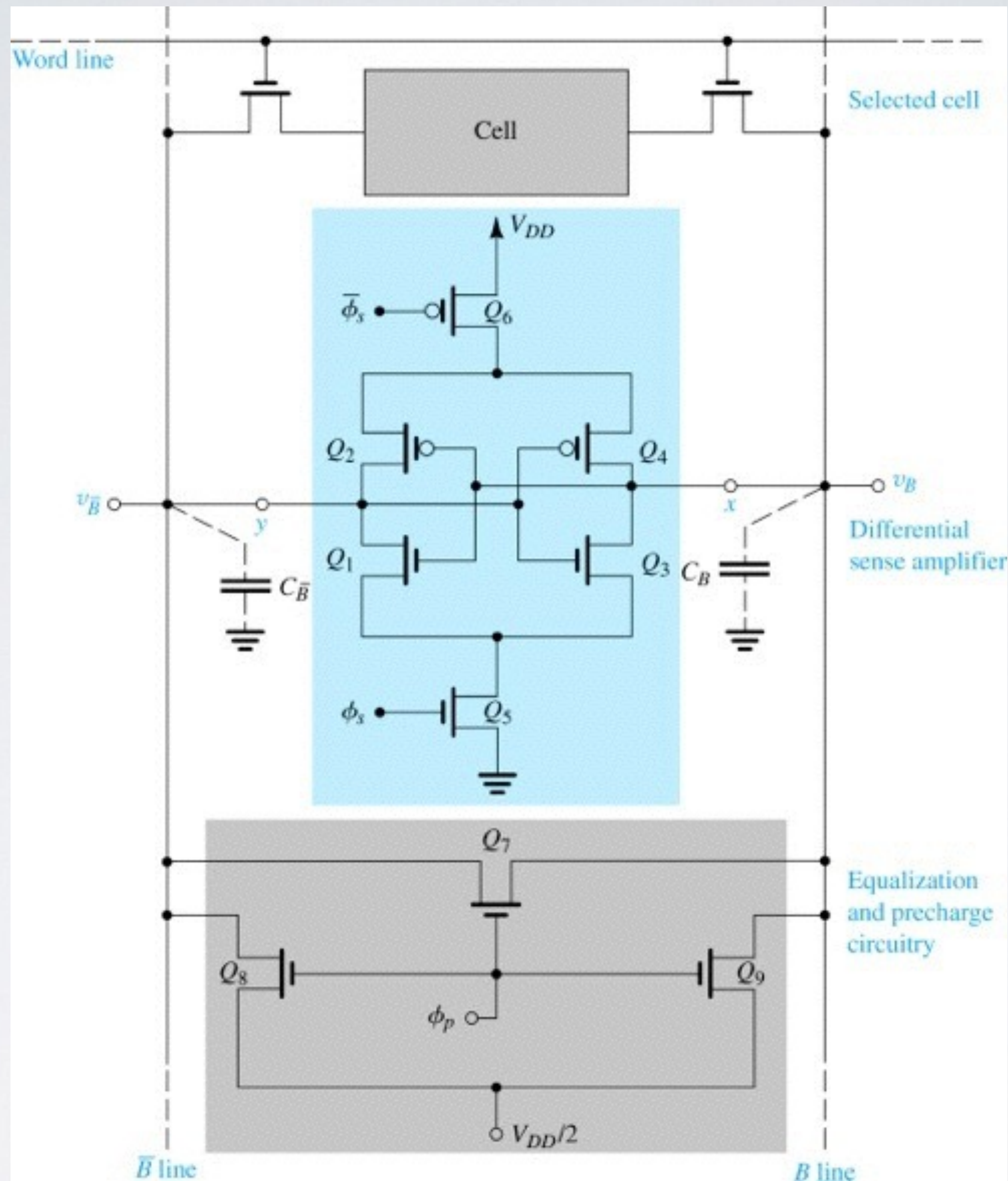


Figure 16.20 A differential sense amplifier connected to the bit lines of a particular column. This arrangement can be used directly for SRAMs (which utilize both the B and $\overline{B}$ lines). DRAMs can be turned into differential circuits by using the "dummy-cell" arrangement shown later (Fig. 16.22).