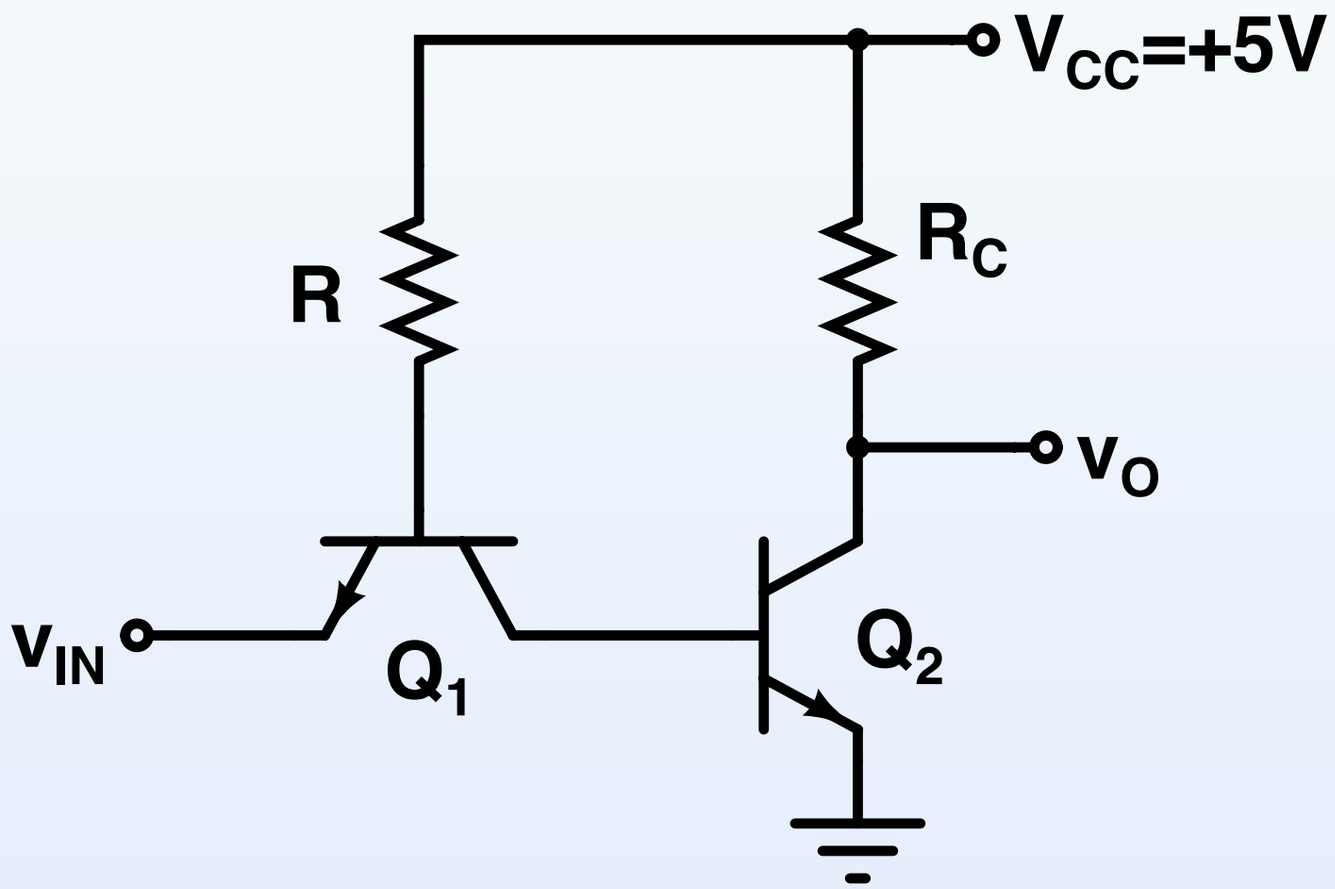
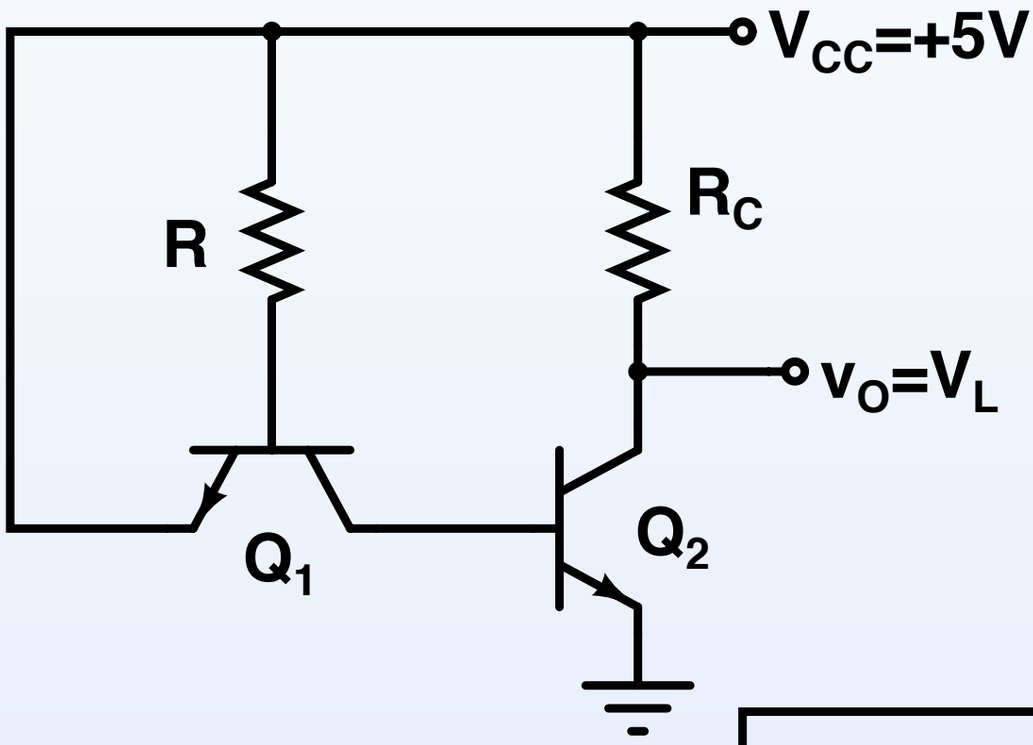
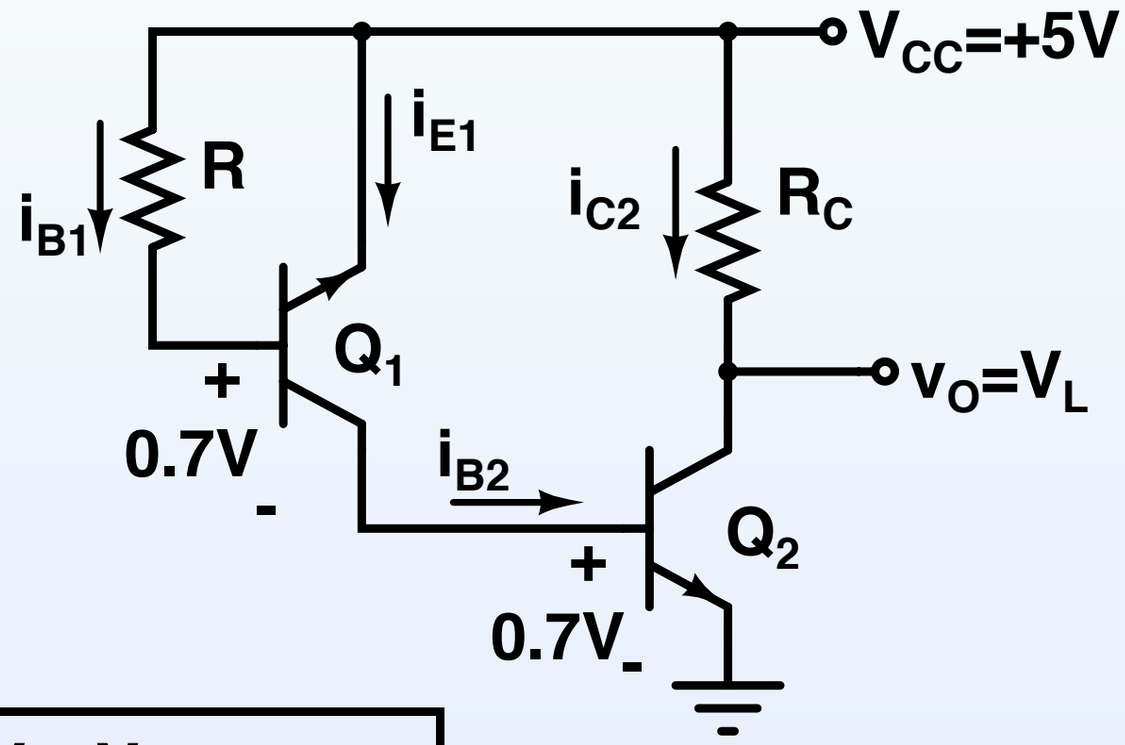
TTL GATES

INEL4207 Digital Electronics

Simple pseudo-TTL Inverter



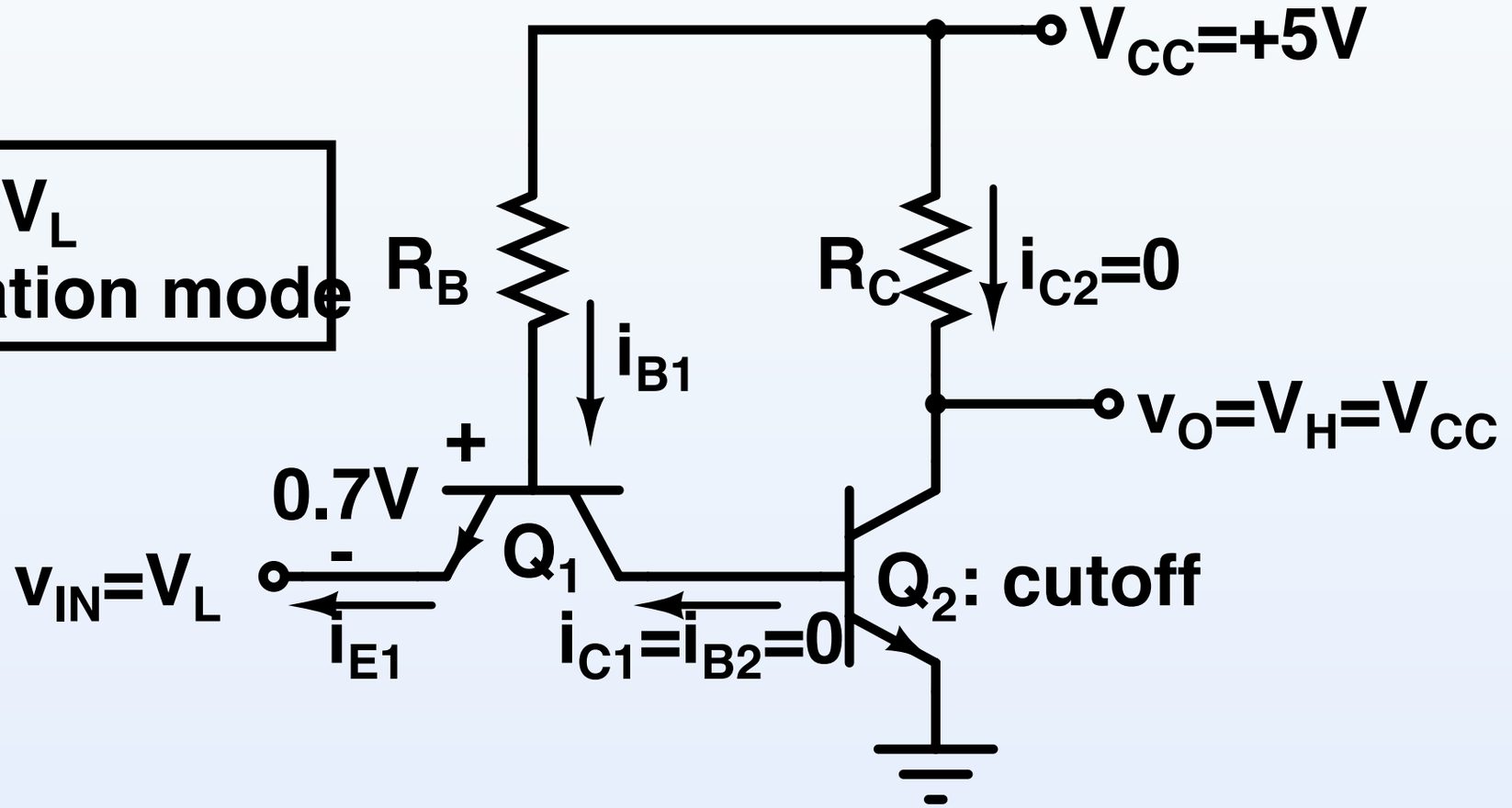


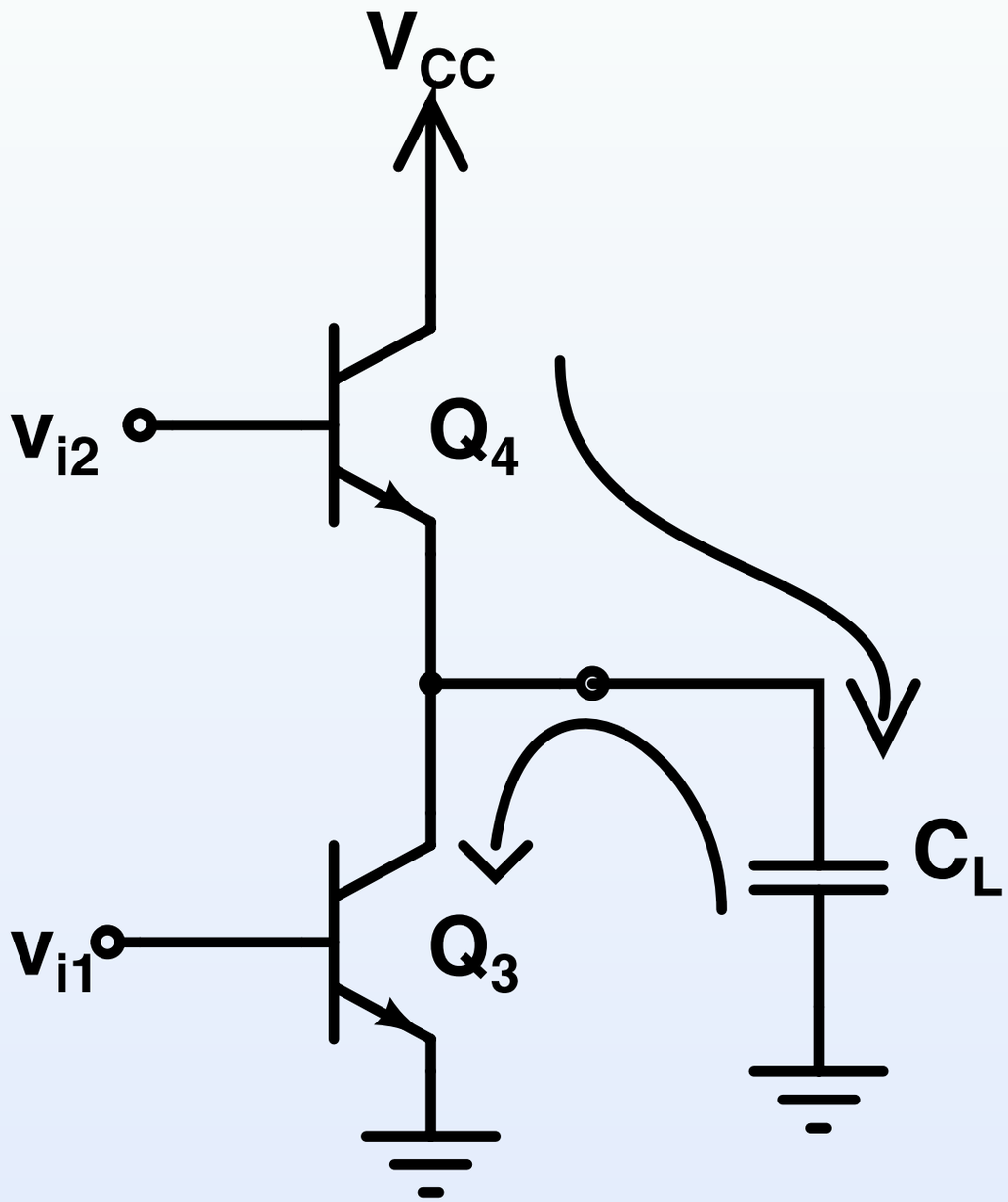


v_{IN}=V_H=V_{CC}

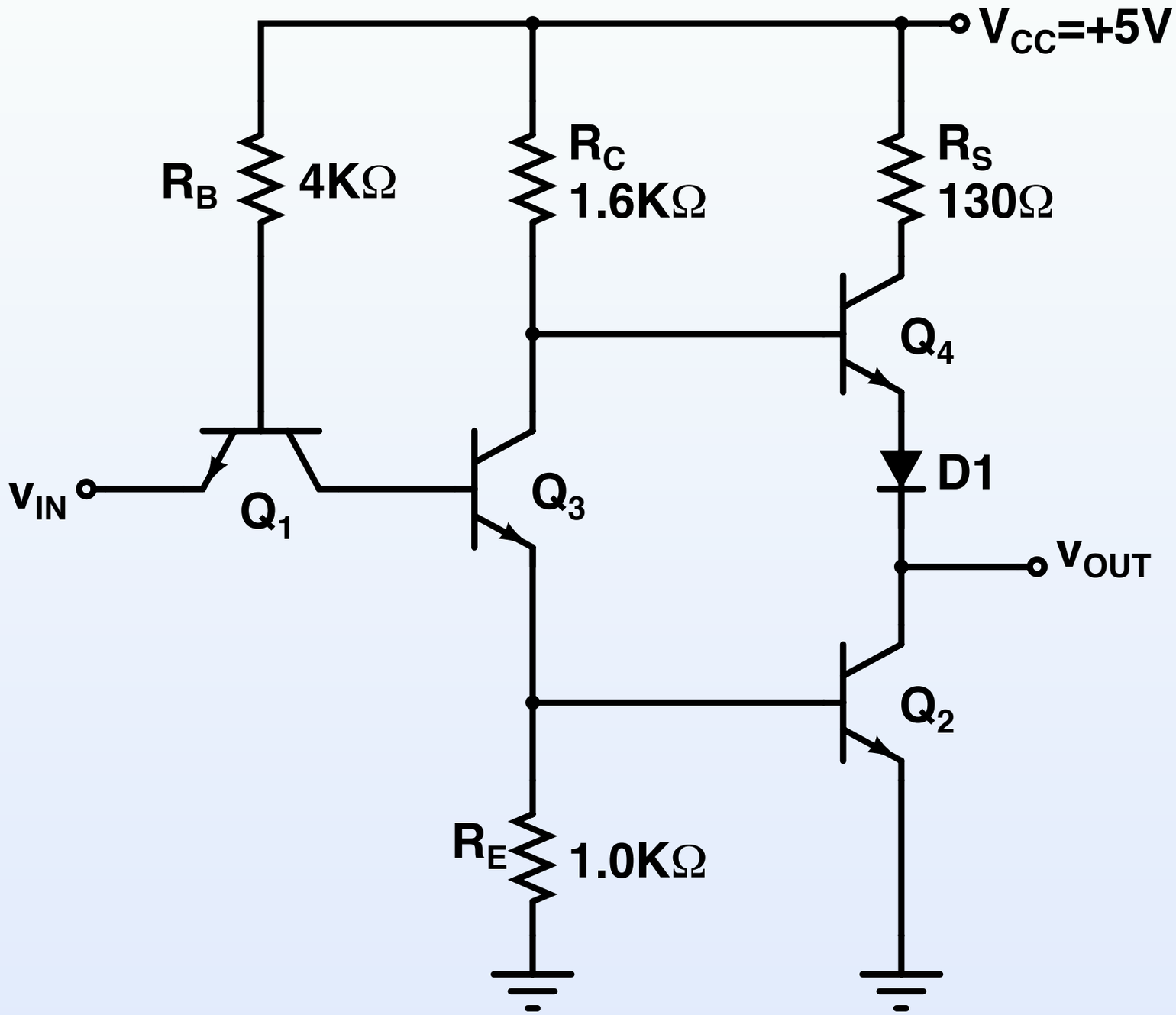
Q_1: reverse-active mode

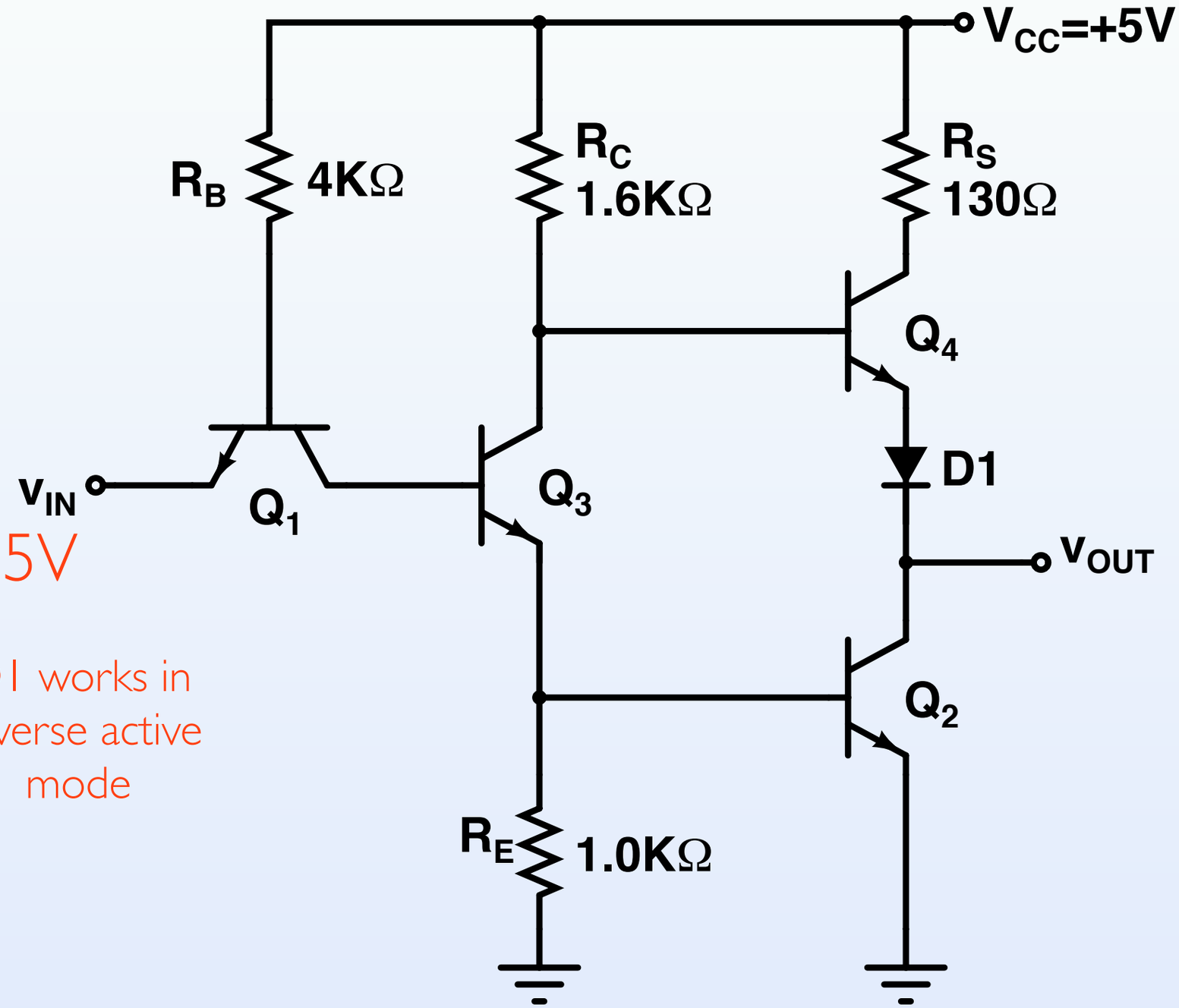
$v_{IN}=V_L$
Q_1: saturation mode




V_{CC}
v_{i2}
Q_4
Q_3
v_{i1}
C_L

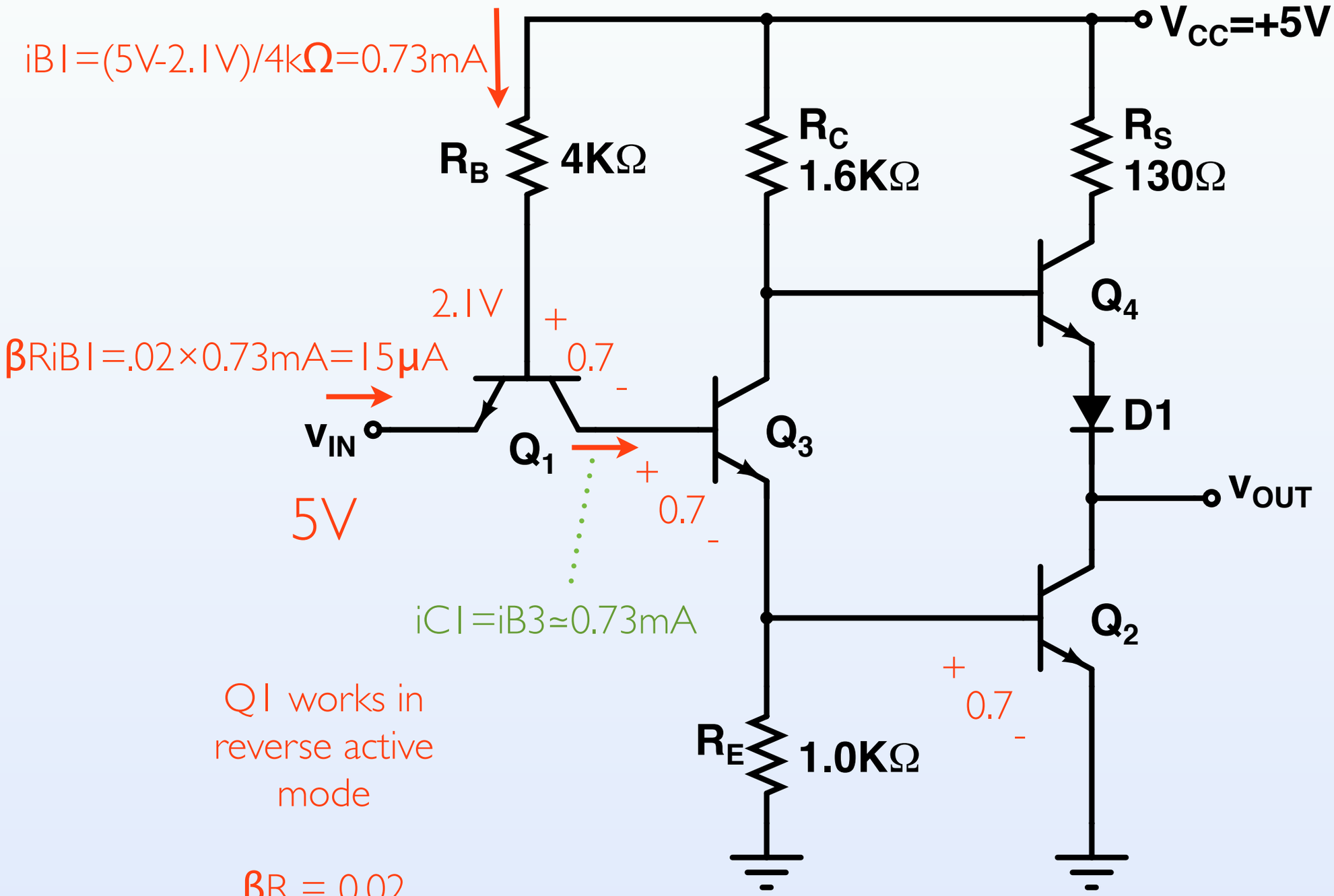
TTL Inverter

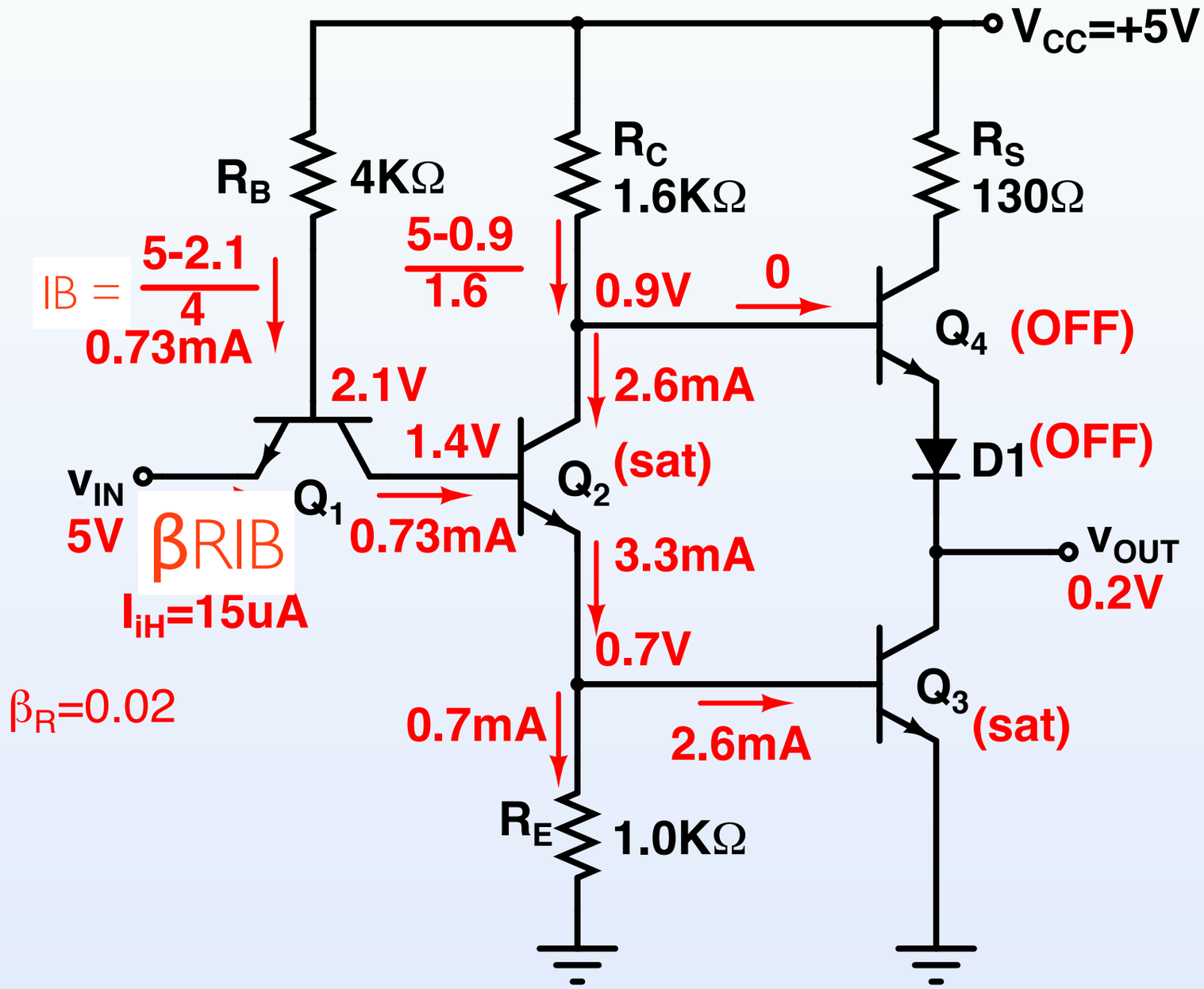


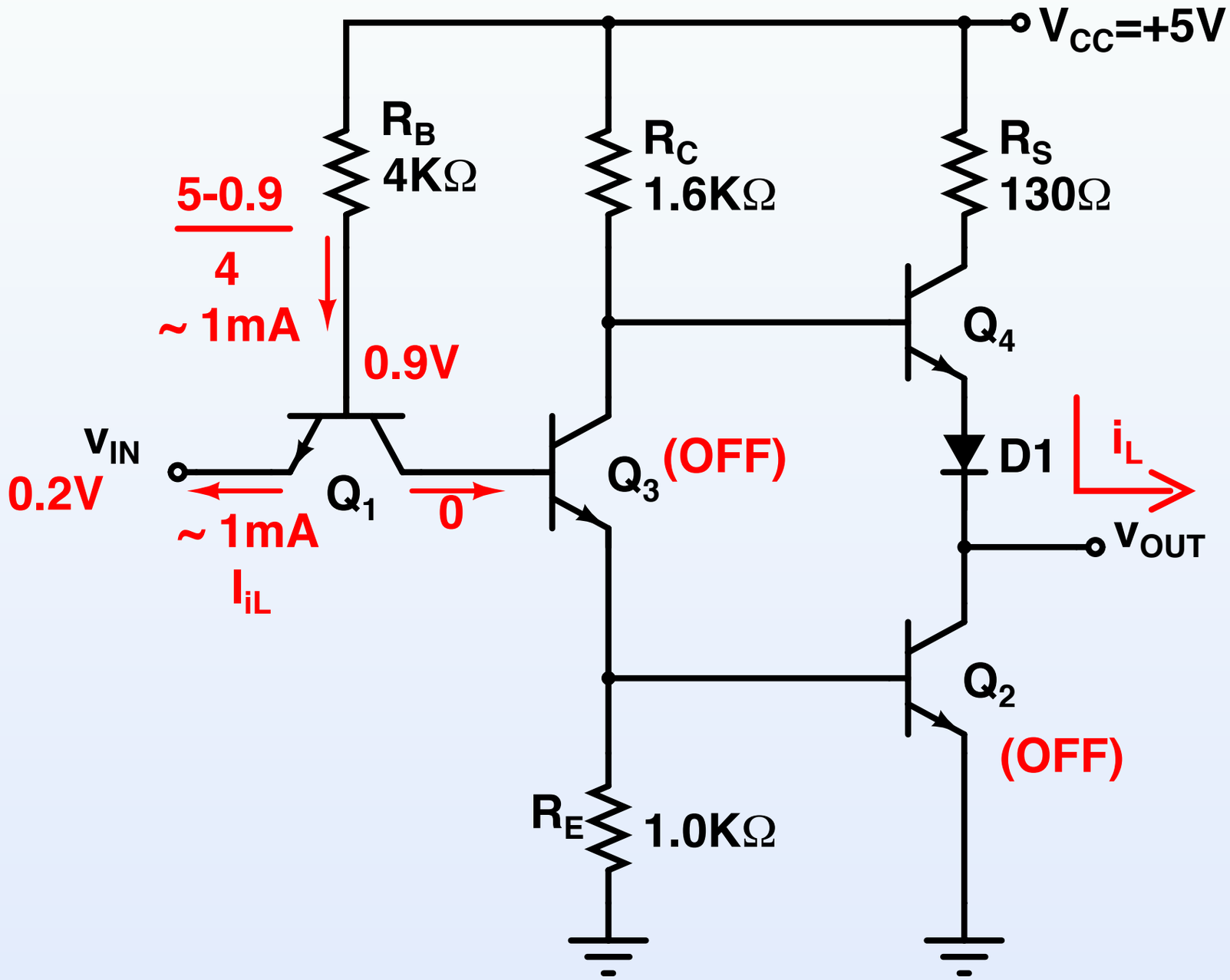


5V

Q1 works in reverse active mode


iB1=(5V-2.1V)/4kΩ=0.73mA
V_{CC}=+5V
R_B 4KΩ
R_C 1.6KΩ
R_S 130Ω
2.1V
+
0.7
-
βRiB1=.02×0.73mA=15μA
Q_4
V_{IN}
Q_1
Q_3
D1
V_{OUT}
+
0.7
-
5V
iC1=iB3≃0.73mA
Q_2
+
0.7
-
R_E 1.0KΩ
Q1 works in reverse active mode
βR = 0.02

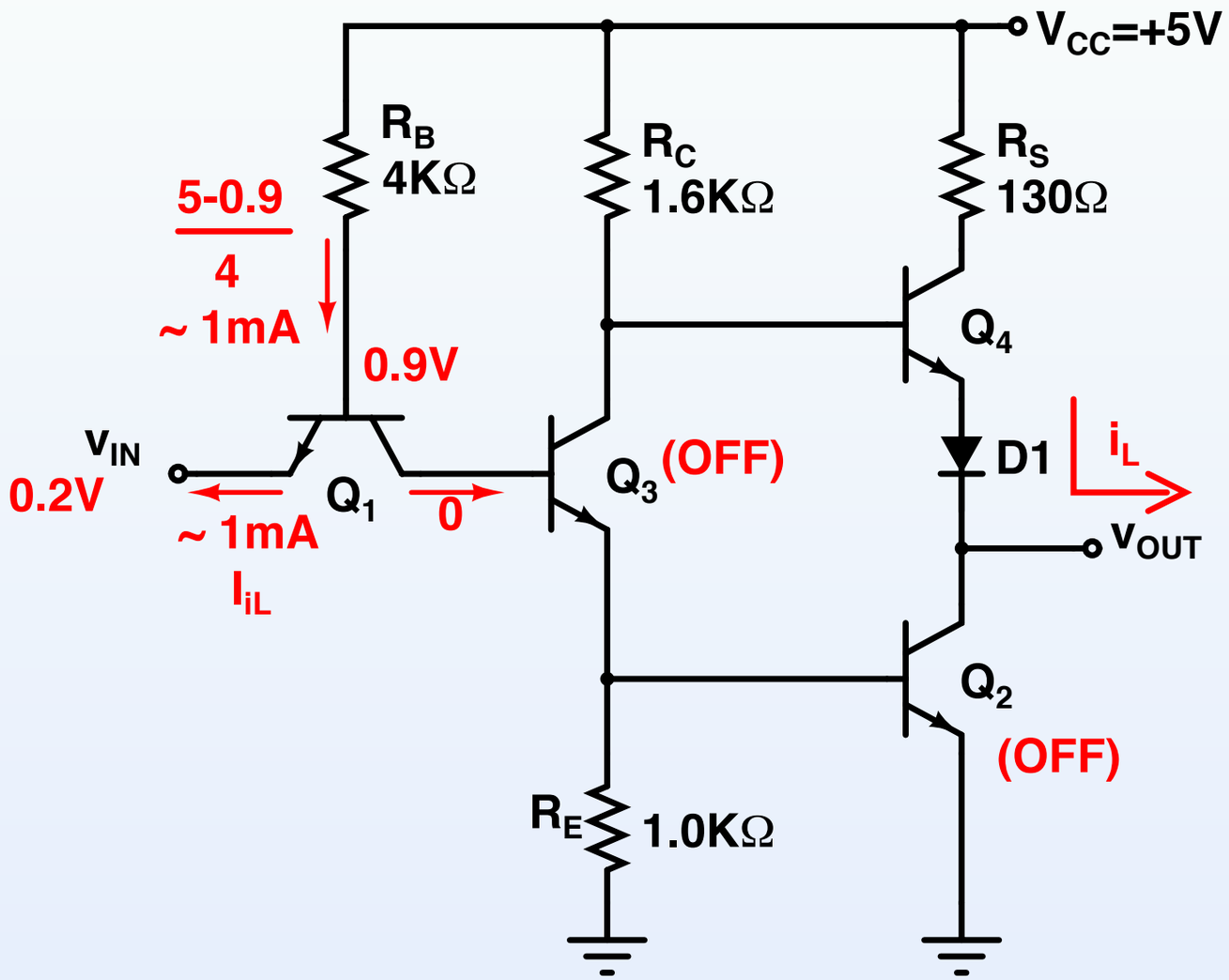

V_{CC}=+5V
R_B 4KΩ
R_C 1.6KΩ
R_S 130Ω
IB = 5-2.1 / 4
0.73mA
5-0.9 / 1.6
0.9V
0
Q_4 (OFF)
2.1V
2.6mA
1.4V
Q_2 (sat)
D1 (OFF)
V_{IN}
5V
Q_1
0.73mA
βRIB
I_{iH}=15uA
3.3mA
V_{OUT}
0.2V
0.7V
Q_3 (sat)
β_R=0.02
0.7mA
2.6mA
R_E 1.0KΩ


V_{CC}=+5V
R_B
4KΩ
R_C
1.6KΩ
R_S
130Ω
5-0.9
4
~ 1mA
0.9V
Q_4
V_{IN}
0.2V
Q_1
~ 1mA
I_{iL}
0
Q_3 (OFF)
D1
i_L
V_{OUT}
Q_2
(OFF)
R_E
1.0KΩ

1. Assuming Q4 has $\beta=50$ and that $V_{CE,Sat}=0.3V$, find value of i_L at which Q4 saturates.

2. Assuming $v_{BE,4}=v_D=0.7V$ when $i=1mA$, find v_O when $i_L=1mA$ and $10mA$.

3. Find the max i_L that can be sourced by a TTL gate while $V_{OH} > 2.4V$ (guaranteed value).



Assuming Q4 has β=50 and that VCE,Sat=0.3V, find value of iL at which Q4 saturates

KVL por el colector de Q4:

$$vE4 = 5V - 130\Omega \times iC4 - 0.3V \quad (1)$$

KVL por base de Q4, con $iB4 = iC4/\beta$

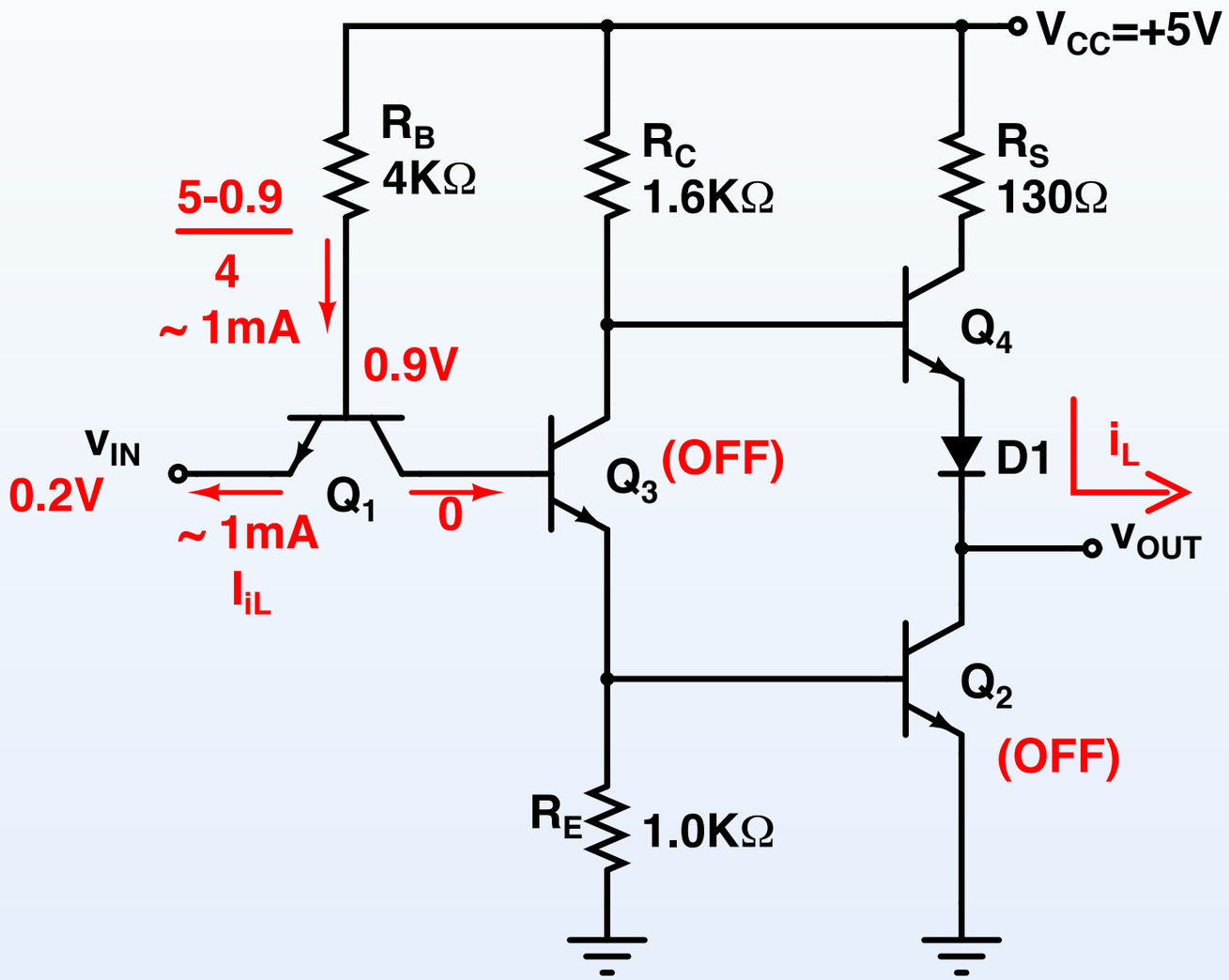
$$vE4 = 5V - 1.6k\Omega \times iC4/50 - 0.7V \quad (2)$$

Igualando (1) y (2)

$$5V - 130\Omega \times iC4 - 0.3V = 5V - 1.6k\Omega \times iC4/50 - 0.7V$$

$$(130\Omega - 1.6k\Omega/50) \times iC4 = 0.7V - 0.3V = 0.4V$$
$$iC4 = 0.4V \div (130\Omega - 32\Omega) = 4.08mA$$

$$iL = 51 \times iC4/50 = 4.16mA$$



Assuming vBE,4 = vD= 0.7V when i = 1mA, find vO when iL = 1mA and 10mA

a) when iL = 1mA

$$vO = 5V - iL \times 1.6k\Omega \div 51 - 0.7V - 0.7V$$

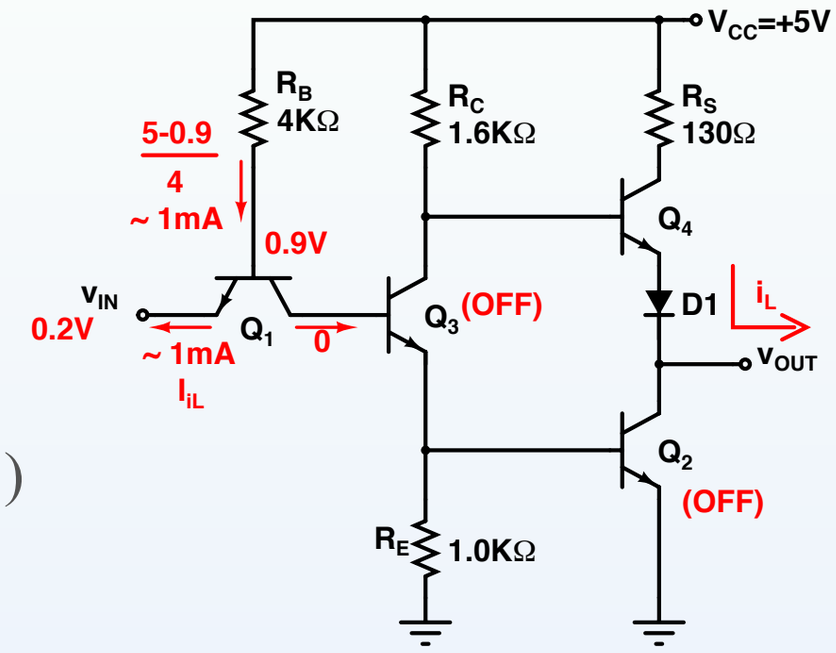
$$= 3.6V - 1mA \times 1.6k\Omega \div 51 \simeq 3.6V$$

b) when iL = 10mA

$$iC \simeq iL = IS \exp(vBE / VT) \qquad (1)$$

$$1mA = IS \exp(0.7V / VT) \qquad (2)$$

(1) ÷ (2)



$$iC / 1mA = \exp((vBE - 0.7V)/ VT)$$

$$vBE = vD = 0.7 + (0.025V) \ln (10) = 0.76V$$

Assuming active region operation,

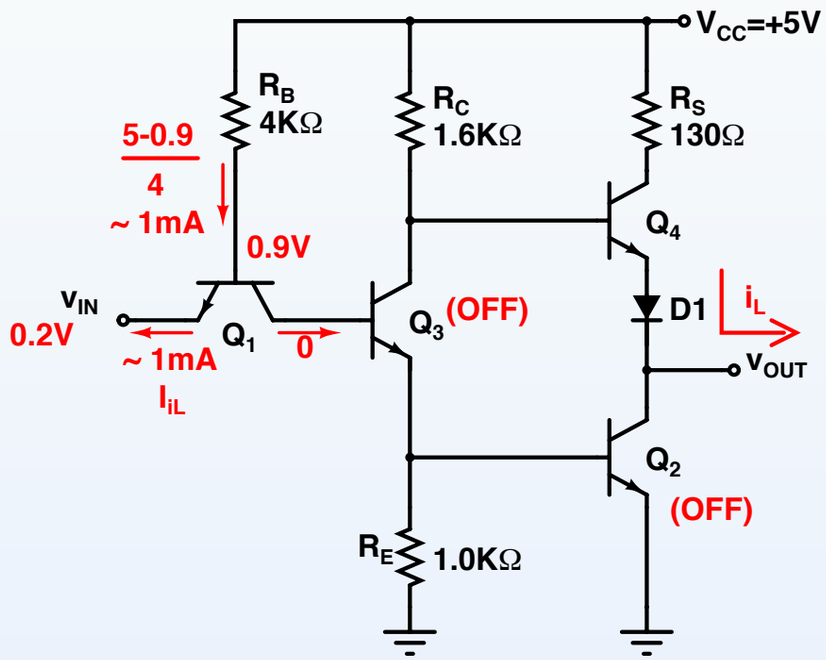
$$vE4 = 5V - iL \times 1.6k\Omega \div 51 - 0.76V = 4.24V - 10mA \times 1.6k\Omega \div 51 \simeq 3.9V$$

$$vC4 \simeq 5V - 130\Omega \times 10mA = 3.7V$$

$\therefore$ Q4 is saturated, and

$$vO = vC4 - 0.3V - 0.76V = 2.64V$$

Find the max iL that can be sourced by a TTL gate while VOH > 2.4V (guaranteed value).



From the previous problem, we expect Q4 to be saturated, and

$$vO = 5V - 130\Omega \times iL - 0.3V - vD = 2.4V$$

$$iL = (2.3V - vD)/130\Omega$$

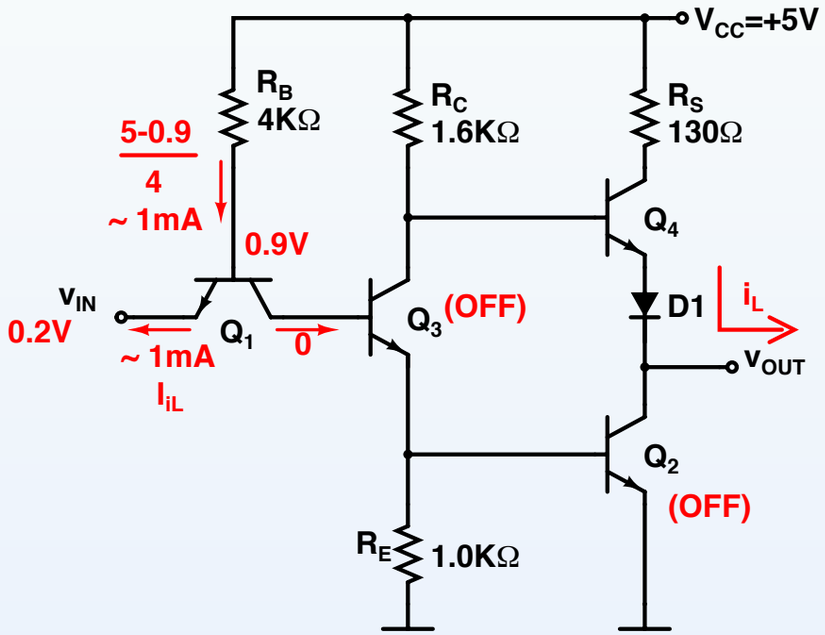
Another equation is needed. Use

$$iL / 1mA = \exp((vD - 0.7V)/ VT)$$

$$vD = 0.7V + VT \ln (iL / 1mA)$$

and solve the two equations by recursive approximation.

vD	iL
0.7V	12.3 mA
0.76V	11.8 mA
0.76V	11.8 mA



vD	iL
0.7V	13 mA
0.76V	12.5 mA
0.76V	12.5 mA

A better approx. not assuming iC = iL:

$$vO = 5V - 130\Omega \times iC - 0.3V - vD = 2.4V$$

$$iC = (2.3V - vD)/130\Omega = iL - iB$$

$$iB = (5V - 2.4V - vBE - vD)/1.6k\Omega$$

Let vBE = vD

$$iL = iC + iB = (2.3V - vD)/130\Omega + (2.6V - 2vD)/1.6k\Omega$$

$$iL = 19.3mA - vD/111.8\Omega$$

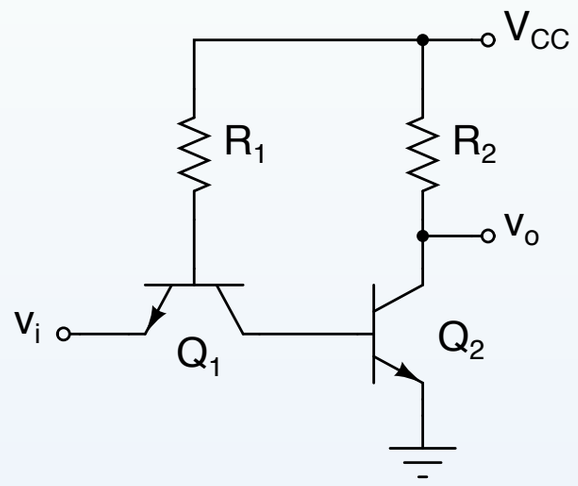
Another equation is needed. Use

$$iL / 1mA = \exp((vD - 0.7V)/ VT)$$

$$vD = 0.7V + VT \ln (iL / 1mA)$$

and solve the two equations by recursive approximation.

El siguiente diagrama muestra un invertidor de lógica TTL simplificada como los que discute el libro de texto.



Use los siguientes datos: $V_{CE_{SAT}} = 0{,}15V$, $v_{BE} = 0{,}7V$ para una junta PN polarizada hacia adelante (*forward bias*), $\beta_F = 20$, $\beta_R = 0{,}1$, $R_1 = R_2 = 20k\Omega$ y $V_{CC} = 2{,}5V$. Determine:

a) el voltaje v_H en la salida cuando el nivel es alto (5 puntos);

b) el voltaje v_L en la salida cuando el nivel es bajo (5 puntos);

c) la corriente en la base del transistor Q_2 cuando $v_i = v_H$ (5 puntos);

d) la corriente en la base del transistor Q_2 cuando $v_i = v_L$ (5 puntos);

e) si el transistor Q_2 esta saturado (explique su respuesta en detalle) (5 puntos);

f) la potencia disipada cuando $v_i = v_H$ (5 puntos);

g) la potencia disipada cuando $v_i = v_L$ (5 puntos);

a) el voltaje V_H en la salida cuando el nivel es alto (5 puntos);
RESPUESTA: $\boxed{V_H = 2{,}5V}$

b) el voltaje V_L en la salida cuando el nivel es bajo (5 puntos);
RESPUESTA: $\boxed{V_L = V_{CE_{SAT}} = 0{,}15V}$

c) la corriente en la base del transistor Q_2 cuando $v_i = V_H$ (5 puntos);
RESPUESTA: El voltaje en la base de Q_1 será más bajo que el del emisor, pero será suficientemente alto para hacer conducir la junta BC de Q_1 y la de BE de Q_2. Por lo tanto,

$$i_{B1} \approx \frac{V_{CC} - v_{BC_1} - v_{BE_2}}{R_1} = \frac{2{,}5V - 1{,}4V}{20k\Omega} = 55\mu A$$

La corriente del emisor de Q_1 será $-\beta_R \times i_{B_1} = -0{,}1 \times 55\mu A = -5{,}5\mu A$, donde el signo negativo indica que la corriente entra al emisor.

$$i_{B_2} = -i_{C_1} = -i_{E_1} + i_{B_1} = \boxed{60{,}5\mu A}$$

d) la corriente en la base del transistor Q_2 cuando $v_i = V_L$ (5 puntos);
RESPUESTA: Si $v_i = V_L = 0{,}15V$, Q_1 estará saturado y el voltaje en la base de Q_2 será de aproximadamente $0{,}3V$. Por lo tanto, Q_2 estar en la región de corte y la corriente será $\boxed{0}$.

e) si el transistor Q_2 esta saturado cuando $v_i = V_H$ (explique su respuesta en detalle) (5 puntos);
RESPUESTA: Si Q_2 estuviera operando en la región activa,

$$i_{C_2} = \beta_F \times i_{B_2} = 20 \times 60{,}5\mu A = 1{,}21mA$$

El voltaje en el colector de Q_2 seria

$$v_{C_2} = V_{CC} - i_{C_2} \times R_2 = 2{,}5V - 20k\Omega \times 1{,}21mA = -21{,}7V$$

lo cual no es posible. Esto demuestra que Q_2 estará saturado.

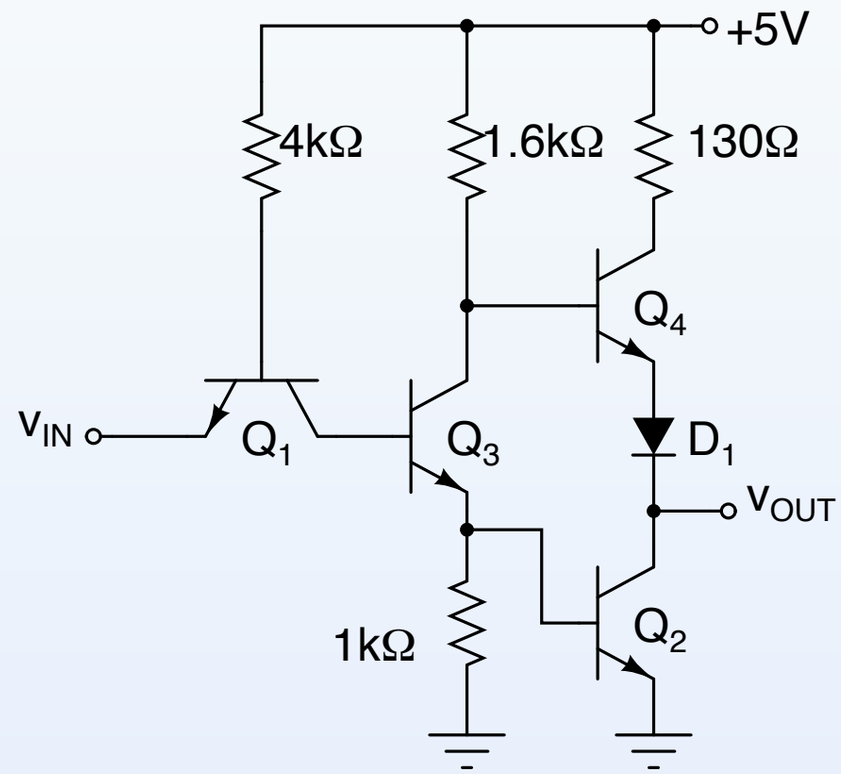
f) la potencia disipada cuando $v_i = V_H$ (5 puntos);
RESPUESTA:

$$P = 2{,}5V \times \frac{2{,}5V - 0{,}15V}{20k\Omega} + 2{,}5V \times 55\mu A + 2{,}5V \times 5{,}5\mu A = \boxed{445\mu W}$$

g) la potencia disipada cuando $v_i = V_L$ (5 puntos);

$$P = (2{,}5V - 0{,}15V) \times \frac{2{,}5V - 0{,}7V - 0{,}15V}{20k\Omega} = \boxed{194\mu W}$$

For the following circuit shown, $\beta_R = 0.2V$, $\beta_F = 10$, $V_{CE,SAT} = 0.2V$ and $V_{BE,ON} = 0.7V$. Find the output voltage if $v_i = 0.2V$ for an inverter driving a load of 20 inverters like the one shown, connected to the output node. (20 points)



ASWER:

For the driver inverter, the input is 0.2V, Q_1 will be saturated, Q_3 and Q_2 will be OFF and Q_4 will be ON.

For the load inverters, the input will be V_H and transistor Q_1 will be operating in reverse-saturation mode, Q_2 and Q_3 will be ON. The input current on each load inverter will thus be

$$\beta_R \times \frac{5V - 2.1V}{4k\Omega} = 0.2 \times .725mA = 145\mu A$$

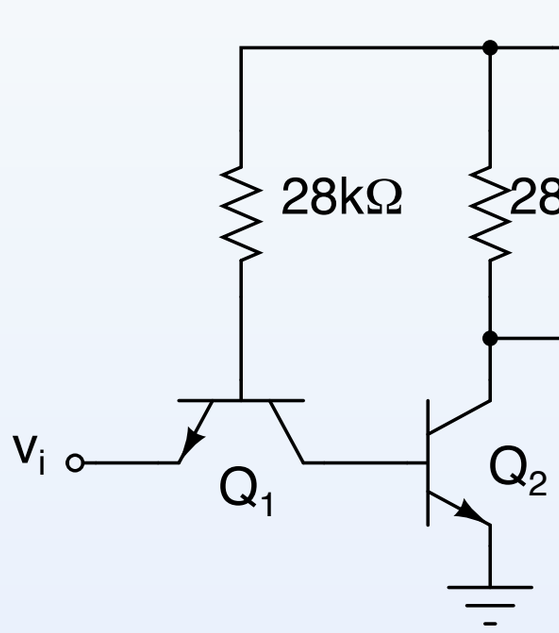
The total current in the emitter of Q_4 is then

$$i_{e4} = 20 \times .145mA = 2.9mA$$

The voltage at Q_4's collector will be $5V - 2.9mA \times 130\Omega = 4.623V$ and the transistor will operate in active mode with a base current $i_{b4} = \frac{2.9mA}{11} = 264\mu A$. Thus the voltage at Q_4's base is $5V - .264mA \times 1.6k\Omega \approx 4.6V$ and the output voltage is

$$\boxed{v_O = 4.6V - 1.4V = 3.2V}$$

Find the power dissipated by the following circuit if $v_i = 2V$. Use the parameters values given in previous problem



ANSWER:

Q_1 must be operating in reverse-active mode, with it's base pinned-down at 1.4V by the two forward-biased PN junctions (Q_1's base-collector and Q_2's base-emitter). Q_1's base current is thus

$$i_{b1} = \frac{5V - 1.4V}{28k\Omega} = 129\mu A$$

A current of $0.2 \times 129\mu A = 25.8\mu A$ flows into the emitter of Q_1. The current flowing into the base of Q_2 is

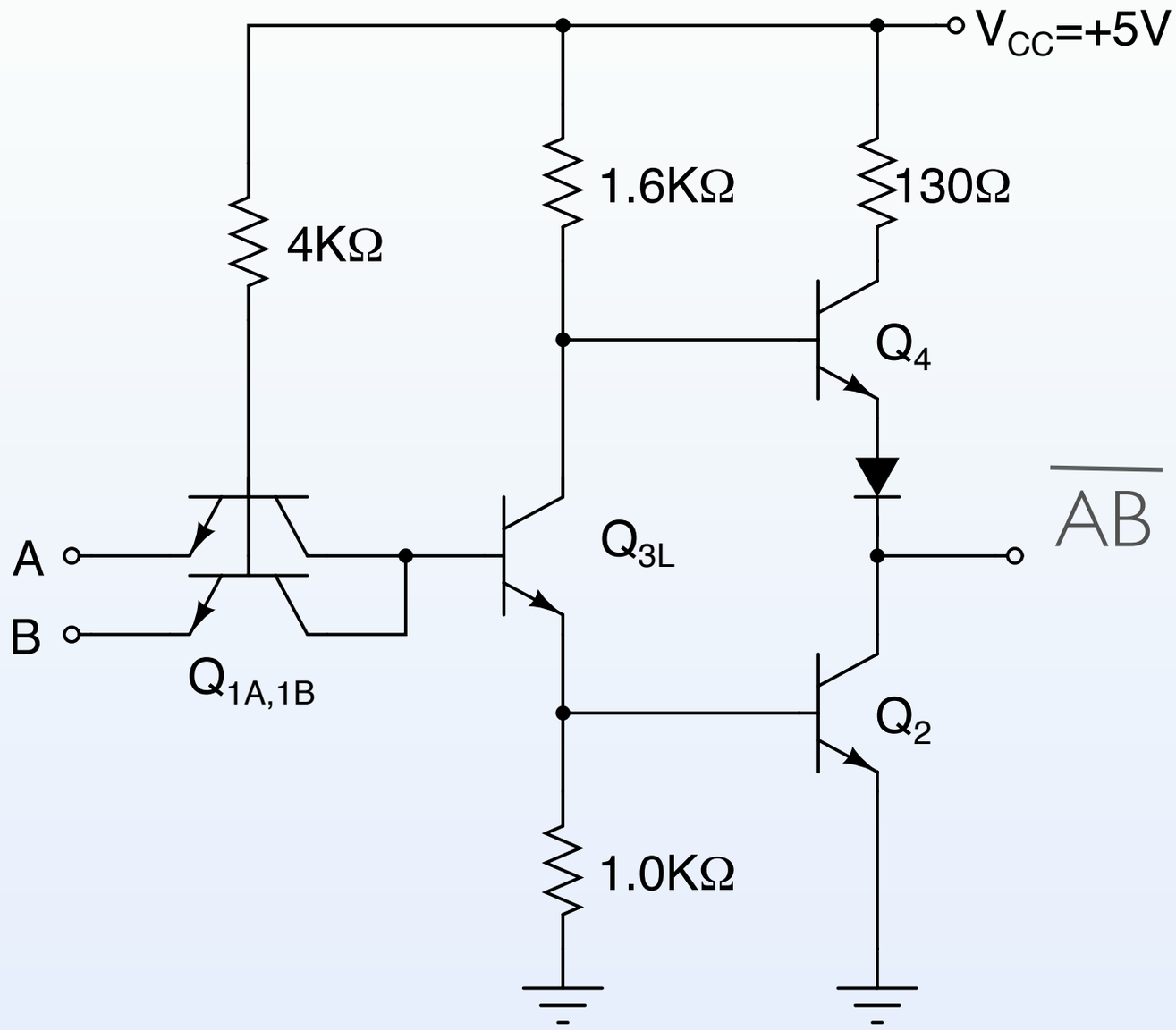
$$i_{b2} = 1.2 \times 129\mu A = 154.3\mu A$$

This current is large enough to saturate transistor Q_2 - otherwise, the drop across the collector resistor would be larger than the supply voltage. Thus the output voltage equals $V_{CE,SAT} = 0.2V$ and the current in Q_2's collector is

$$i_{c2} = \frac{5V - 0.2V}{28k\Omega} = 171.4\mu A$$

Finally, the dissipated power can be found to be

$$\boxed{P = 5V \times 129\mu A + 5V \times 171.4\mu A + 2V \times 25.8\mu A = 1.55mW}$$



TTL NAND Gate

AND-OR-INVERT Gate