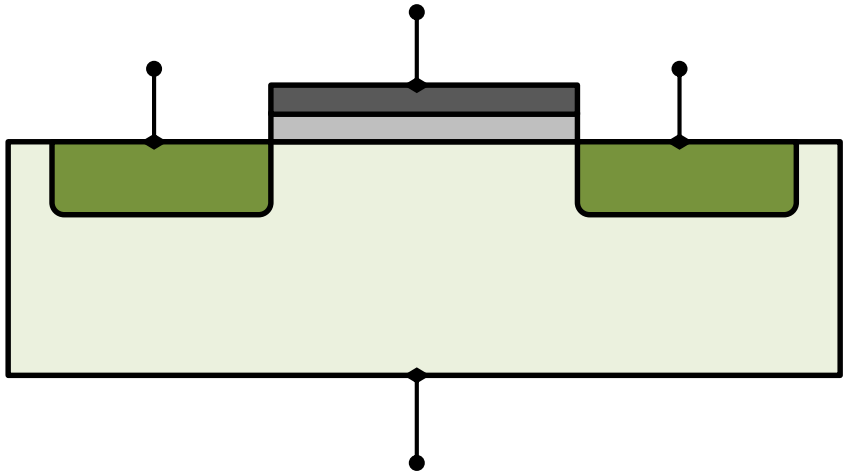
# MOSFET → Chapter 5

10/28/2019

- **MOS – Metal Oxide Semiconductor**
- **FET – Field-Effect Transistor**
- **4 terminal device**

**Advantages:**

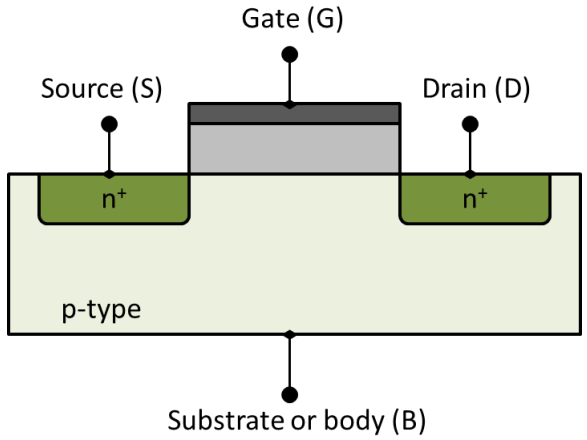
- **Small area; comparatively**
- **Less power**
- **Relatively simple manufacturing process**

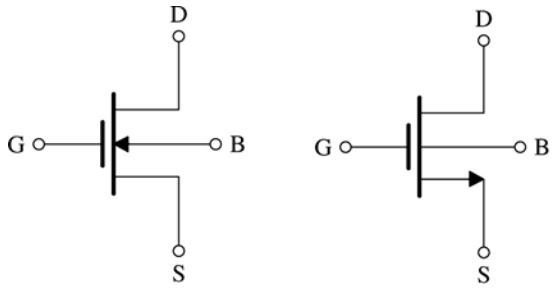


Cross Section Diagram

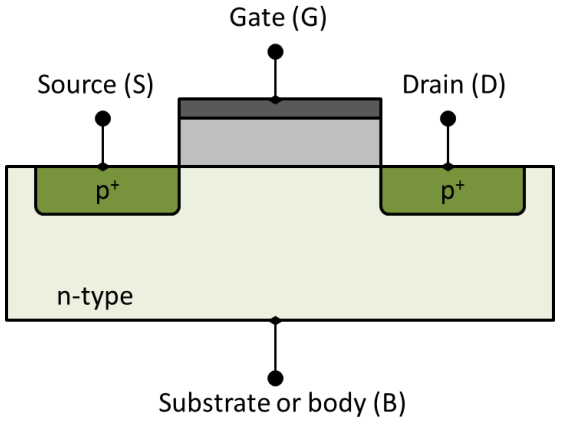
** If the bulk terminal is omitted, it is presumed is connected to the source*

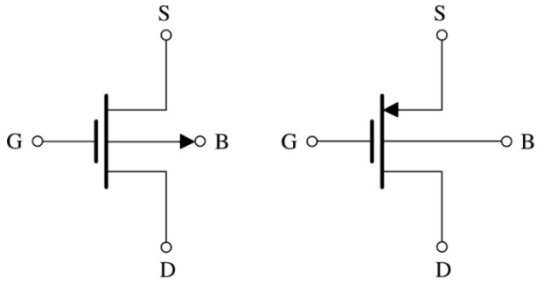
- ***nMOS Transistor***




- ***pMOS Transistor***



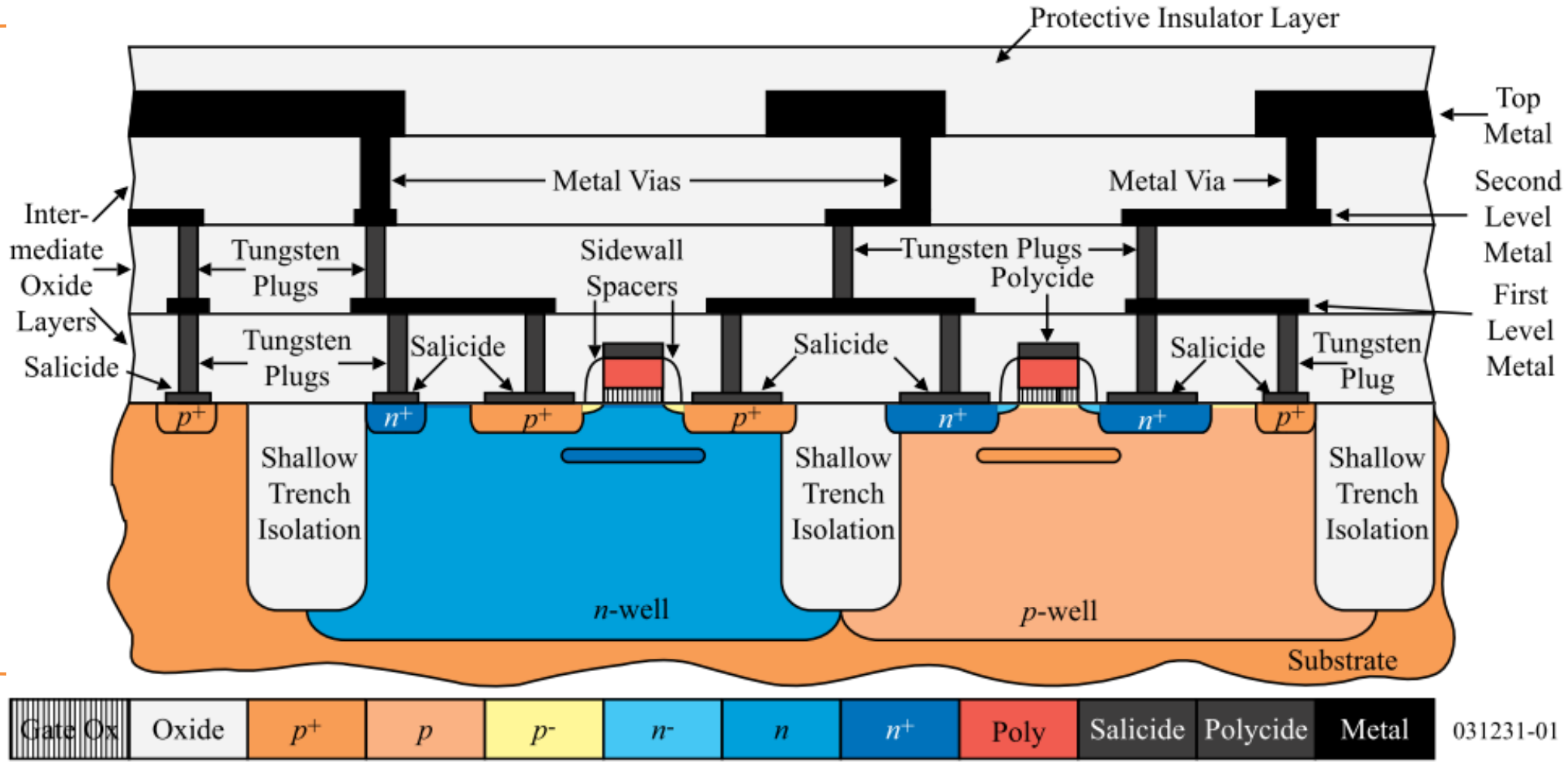

Symbol

# Modern CMOS Technology

## *Twin-Well Process*



*IC – Cross-Section*

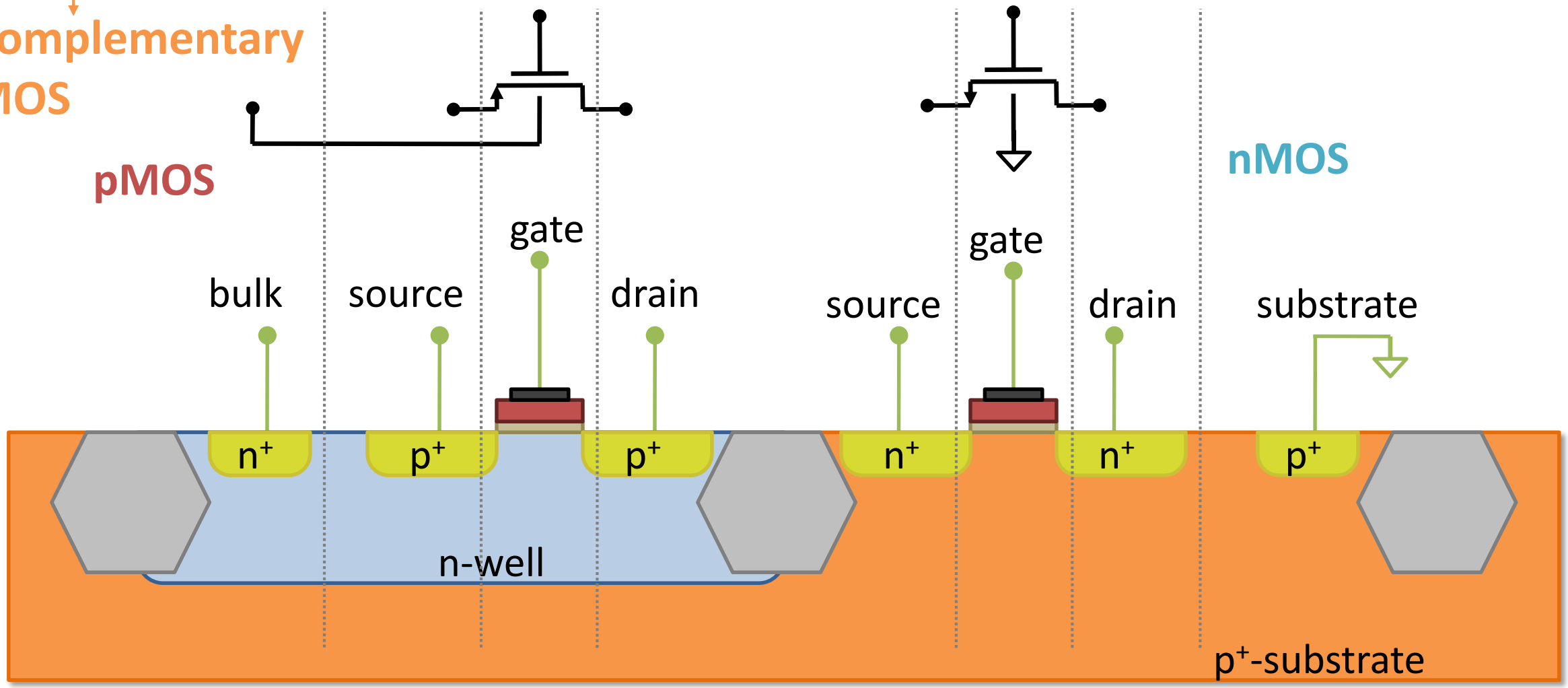


# CMOS Transistors

*Single-Well Process*



**Complementary MOS**



# Operation Regions

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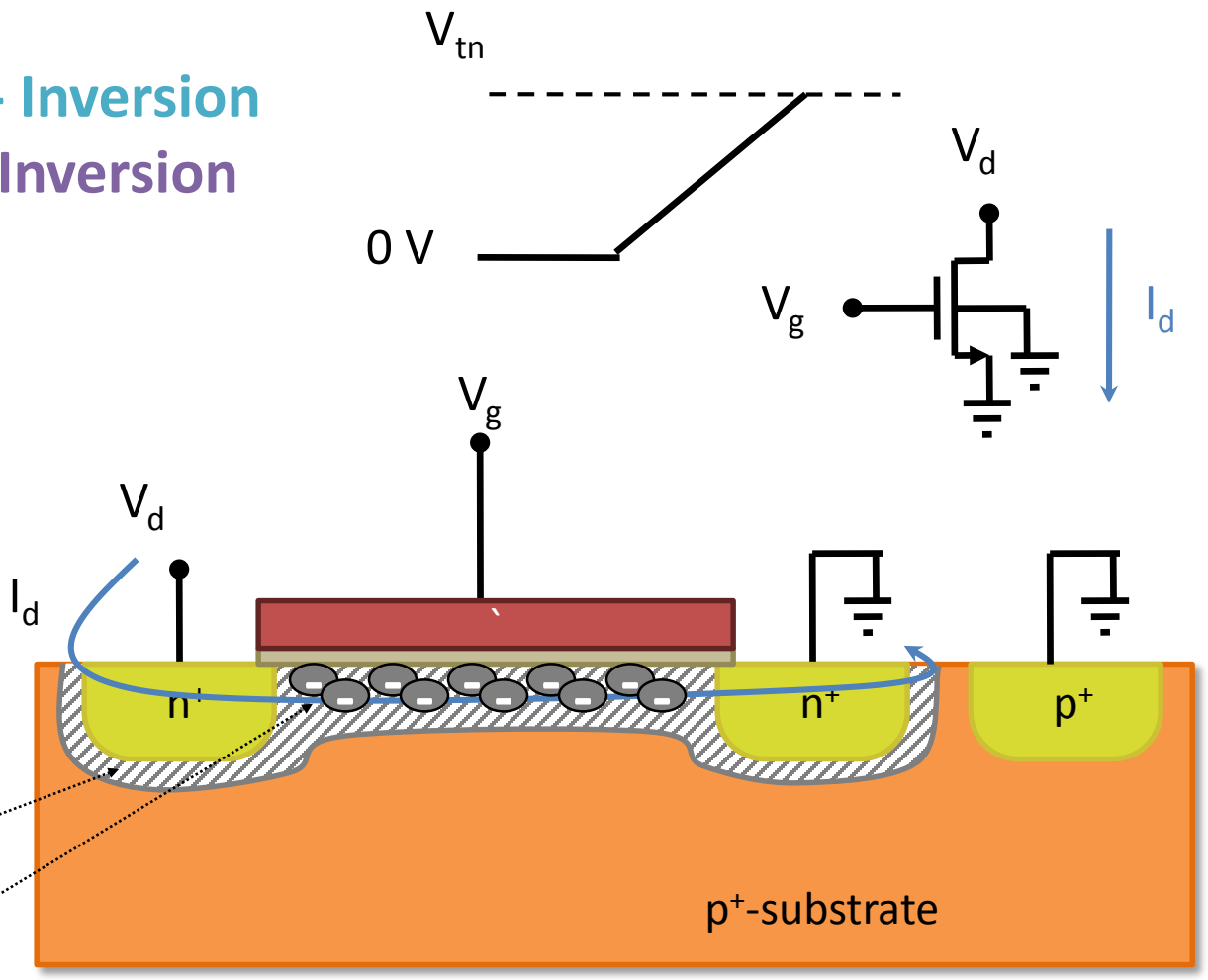
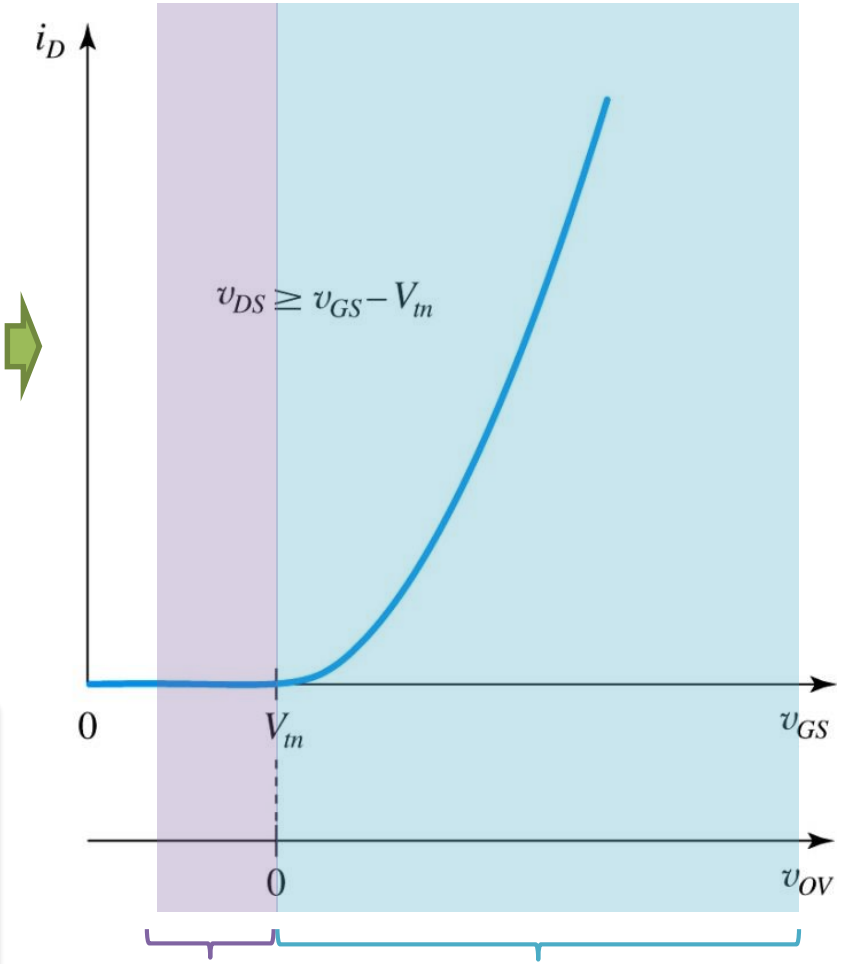
1) **Cut-Off**
2) **Strong - Inversion**
3) **Weak - Inversion**




$I_D = f(e^{V_{GS}})$ $I_D = f(v_{GS}^2)$

# nMOS Strong Inversion → Saturation

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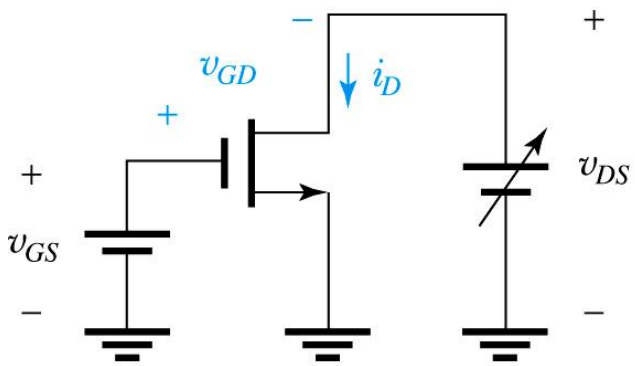
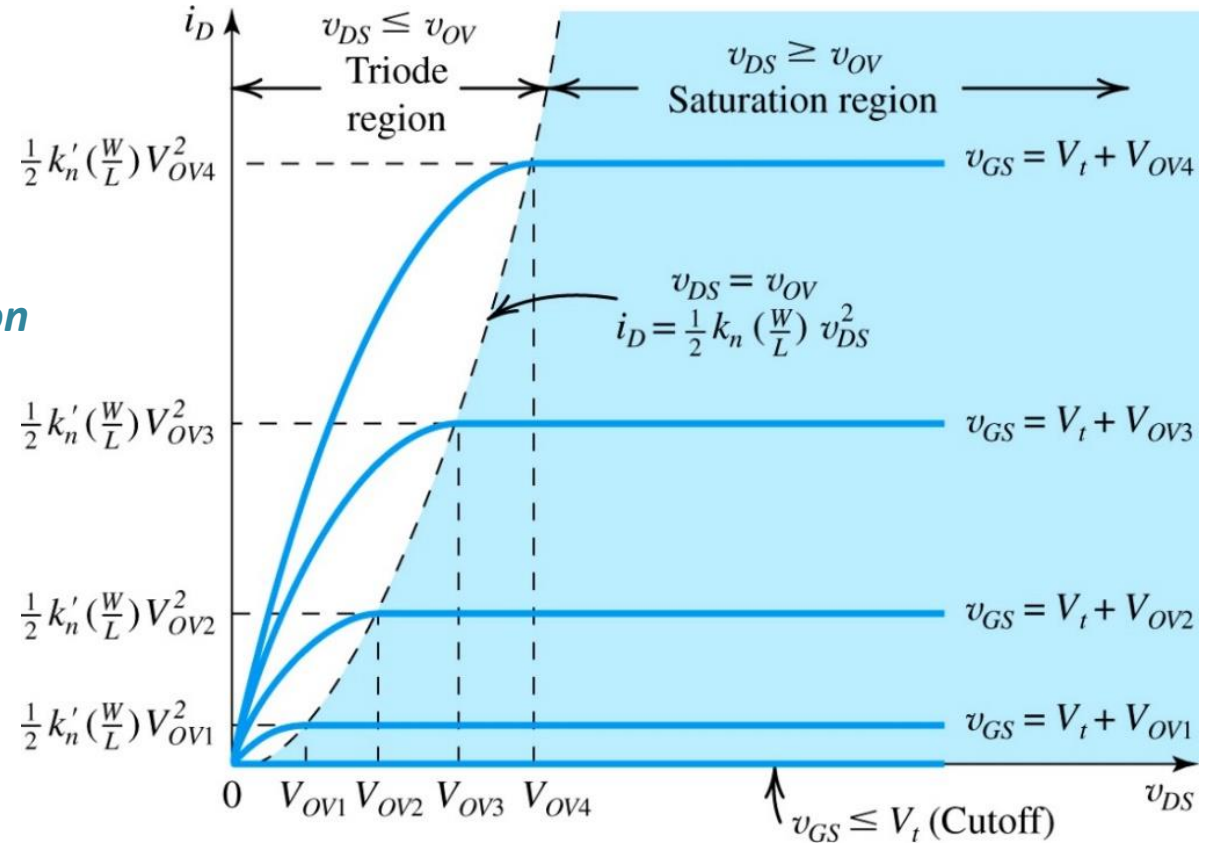



- $v_{GS} > v_{tn}$
- $v_{DS} > v_{GS} - v_{tn}$
- $i_G = 0$

**Over-drive Voltage** $V_{ov} = V_{GS} - V_{tn}$

$i_D \approx f(v_{GS}^2)$




$K_n$

*Channel Length Modulation Parameter [1/V]*

$$I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_{tn})^2(1 + \lambda V_{DS})$$

$$\approx \frac{1}{2}k_n'\frac{W}{L}(V_{GS} - V_{tn})^2$$

*nMOS Transconductance Parameter [A/V²]*

$$k_n' = \mu_n C_{ox}$$

# nMOS Strong Inversion → Ohmic

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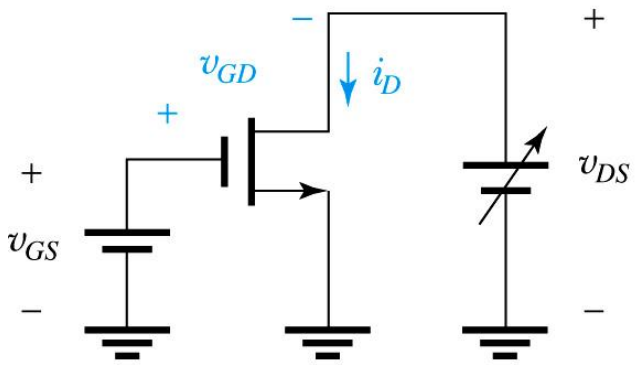



- $v_{GS} > v_{tn}$
- $v_{DS} < v_{GS} - v_{tn}$
- $i_G = 0$

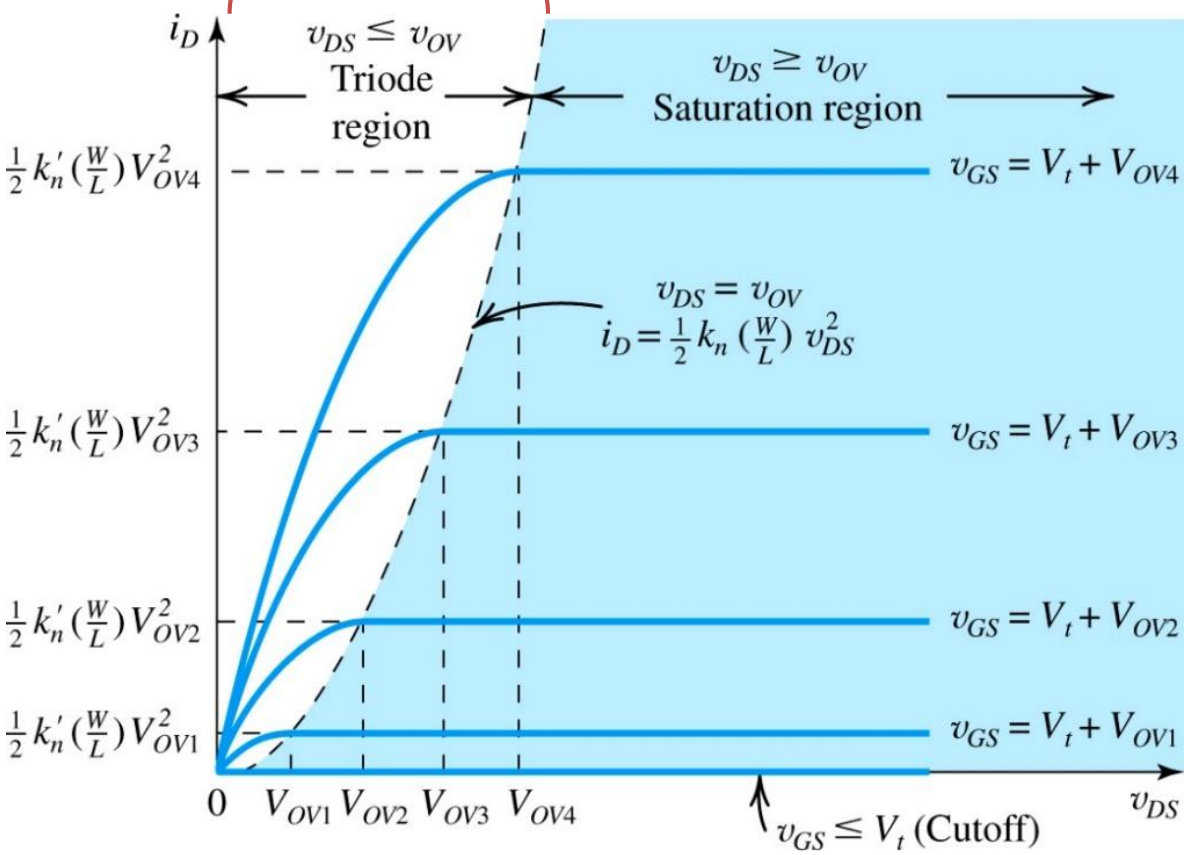
$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_{tn})(V_{DS}) - \frac{1}{2}V_{DS}^{\ 2}\right]$$

$$\approx k_n' \frac{W}{L}(V_{GS} - V_{tn}) \cdot V_{DS}$$

$$r_{ds} = \frac{1}{k_n' \frac{W}{L}(V_{GS} - V_{tn})}$$

$V_{ov} = V_{GS} - V_{tn}$

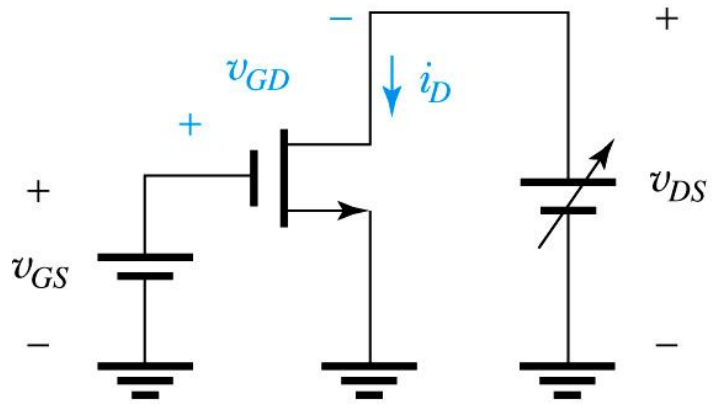
$i_D = f(v_{GS}, v_{DS})$



# Overdrive Voltage

***Additional voltage required at $V_{GS}$ to be able to conduct a given current $I_D$***

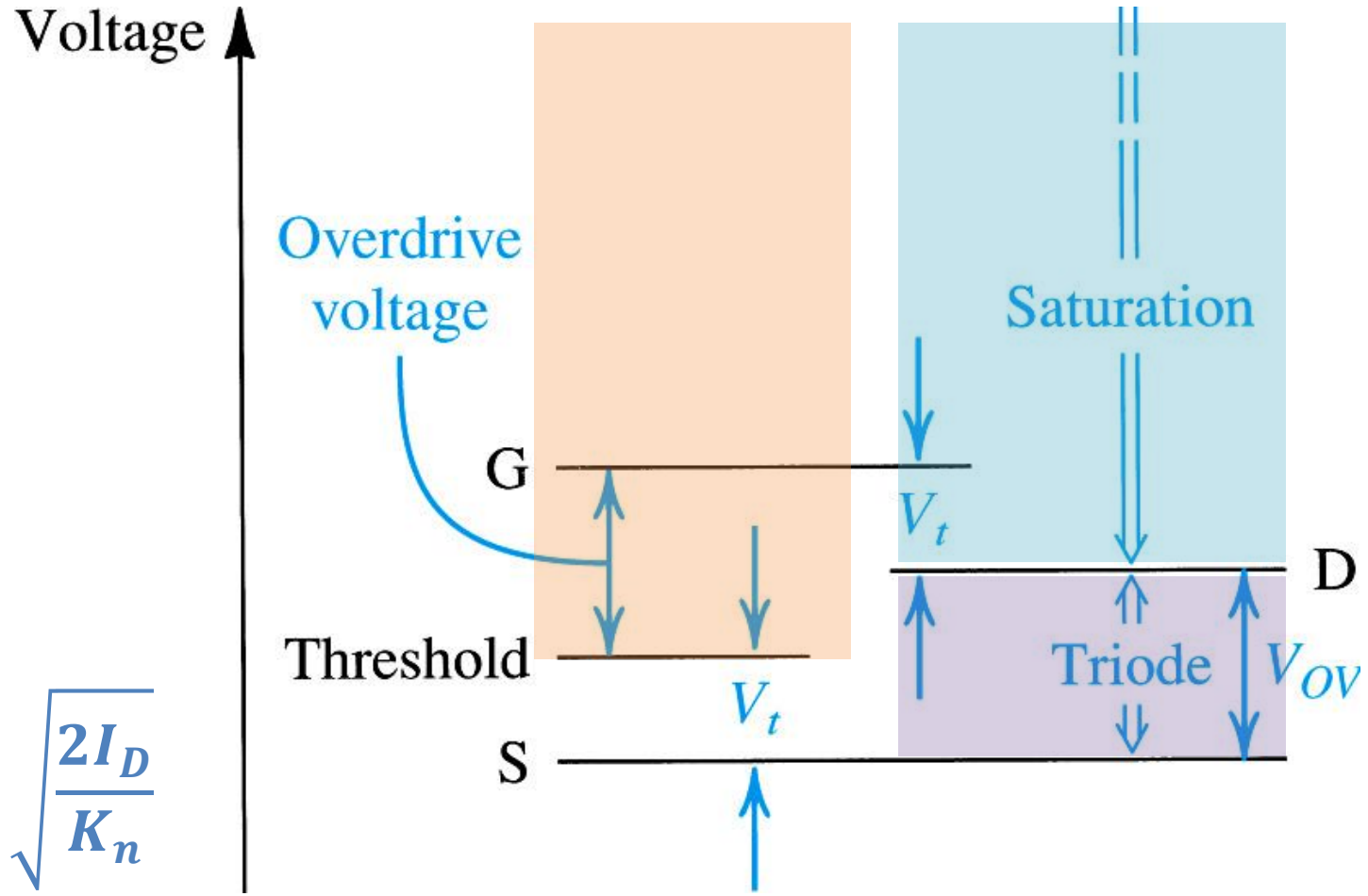





$\mathbf{V_{GS} > V_{tn} \rightarrow}$ **Strong Inversion**

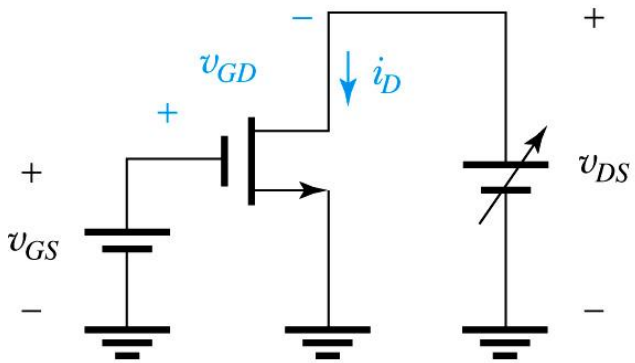
- $\mathbf{V_{DS} > V_{ov} \rightarrow}$ **Saturation**
- $\mathbf{V_{DS} < V_{ov} \rightarrow}$ **Ohmic**

$$\mathbf{V_{ov} = V_{GS} - V_{tn} = \sqrt{\frac{2I_D}{K_n}}}$$



# nMOS Weak Inversion → Saturation






- $V_{GS} < V_{tn}$
- $V_{DS} > 0.1\ V$

$$I_D = I_0 e^{\frac{V_{GS} - V_{tn}}{n \cdot U_t}}$$

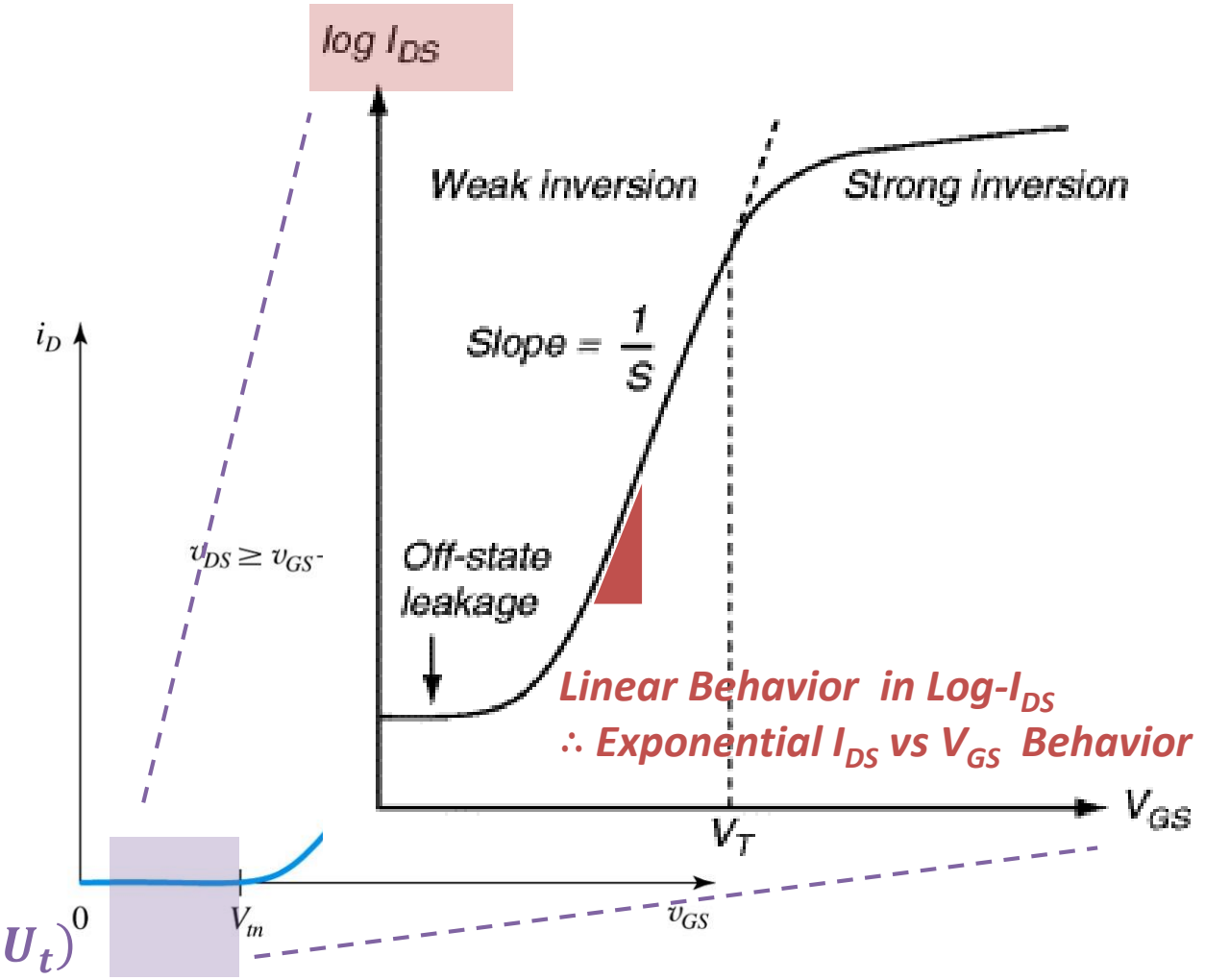
*Slope Factor*

$n = [1 : 2]$

*Thermal Voltage [V]*

$U_t \propto T$

$U_t \approx 25mV\ @\ 25^oC$




$$(V_{tn} - 5 \cdot U_t) < V_{GS} < (V_{tn} - 2 \cdot U_t)$$

# nMOS Large Signal Model



***Condition***

- **Strong Inversion – Ohmic**

$$I_D = \mu C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{{V_{DS}}^2}{2}\right]$$

$V_{GS} > V_{th}$
$V_{DS} < V_{OV}$

- **Strong Inversion - Saturation**

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$

$V_{GS} > V_{th}$
$V_{DS} > V_{OV}$

- **Weak Inversion - Saturation**

$$I_D = I_0 . e^{\frac{V_{GS} - V_{th}}{nU_T}}$$

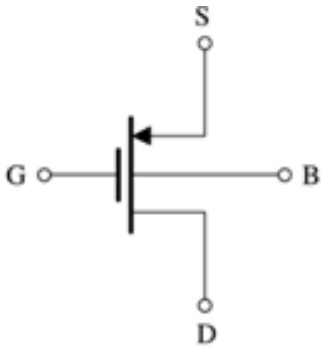
$V_{th} - 5 \cdot U_T < V_{GS} < V_{th} - 2 \cdot U_T$

# Weak Inversion vs Strong Inversion?

| Weak Inversion | Strong Inversion |
|---|---|
| Saturation current is exponential in $V_{GS}$ | Saturation current is square law in $V_{GS}$ |
| $V_{DSAT}$ is constant at approximately 100mV | $V_{DSAT}$ varies linearly with gate voltage |
| Current flows by diffusion | Current flows mainly by drift |
| Charge concentrations are small | Charge concentrations are large |
| Currents are small | Current are large |
| Good for ultra-low-power operation | Good for high-power operation |
| Power efficiency is constant with current | Power efficiency is lower |
| High noise and offset | Low noise and offset |
| Can work on low power supply voltage | Needs higher power supply voltages |
| Linearity is hard to achieve | Linearity is easy to achieve |
| Suited for slow-and-parallel architectures | Suited for fast-and-serial architectures |

# pMOS Large Signal Model

10/28/2019




## Saturation Mode

- $v_{SG} > |v_{tp}|$
- $v_{SD} > v_{SG} - |v_{tp}|$
- $i_G = 0$

$$I_D = \frac{1}{2} k_p{}' \frac{W}{L} (V_{SG} - |V_{tp}|)^2 (1 + \lambda V_{SD})$$

$$\approx \frac{1}{2} k_p{}' \frac{W}{L} (V_{SG} - |V_{tp}|)^2$$

$$V_{ov} = V_{SG} - |V_{tp}|$$

## Ohmic Mode

- $v_{SG} > |v_{tp}|$
- $v_{SD} < v_{SG} - |v_{tp}|$
- $i_G = 0$

$$I_D = k_p{}' \frac{W}{L} \left[ (V_{SG} - |V_{tp}|)(V_{SD}) - \frac{1}{2} V_{SD}{}^2 \right]$$

$$\approx k_P{}' \frac{W}{L} (V_{SG} - |V_{tp}|) \cdot V_{SD}$$

*pMOS Transconductance Parameter [A/V²]*

$$k_p{}' = \mu_p C_{ox}$$

# MOSFET Model Parameters

$U_t = kT/q$ → thermal voltage (~25mV @ room temp.)

$\mu$ → electron/hole mobility
$\kappa_s = 1/n$ → subthreshold slope coefficient (unit-less)
$C_{ox} = \varepsilon_{ox}/t_{ox}$ → gate oxide capacitance per unit area ($F/cm^2$)
$\varepsilon_{ox}$ → dielectric permittivity of $SiO_2$
$t_{ox}$ → oxide thickness

$K_n = k_n' \cdot W/L$ → transconductance parameter($A/V^2$)
$k_n' = \mu C_{ox}$
$\gamma$ → body effect coefficient ($V^{1/2}$)
$\lambda$ → channel-length modulation parameter ($V^{-1}$)

$V_{T0}$ → threshold voltage at $V_{SB}$=0 (V)
$V_T$ → threshold voltage (V)
$\phi_0$ → ≈ surface potential (V)

# Threshold Voltage

**The required voltage to produce and inversion layer.**

$$V_T = V_{T0} + \gamma\left(\sqrt{\phi_0 + V_{SB}} - \sqrt{\phi_0}\right)$$

**surface potential**

**body effect coefficient**

$$V_{T0} = \phi_{ms} + 2\phi_F + \frac{Q_{dep}}{C_{ox}}$$

**The threshold voltage is a function of $V_{SB}$!!!**

**work-function difference between the gate metal and the silicon**

Fermi level

**voltage required to sustain the depletion layer**

# Example 5.2



**Consider an nMOS transistor fabricated in a 0.18µm process with L=0.18µm and W=2um. The process technology is specified to have $C_{ox}$=8.6fF/µm$^2$, $\mu_n$=450cm$^2$/V·s, and $V_{th}$=0.5V.**

a) **Find $V_{GS}$ and $V_{DS}$ that result in the MOSFET operating at the edge of saturation with $I_D$=100 µ A.**
b) **If $V_{GS}$ is kept constant, find $V_{DS}$ that results in $I_D$=50µA.**
c) **To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with $V_{DS}$=0.3V. Find the change in $i_D$ resulting from $v_{GS}$ changing from 0.7V by +0.01V and by -0.01V.**

# Example 5.5



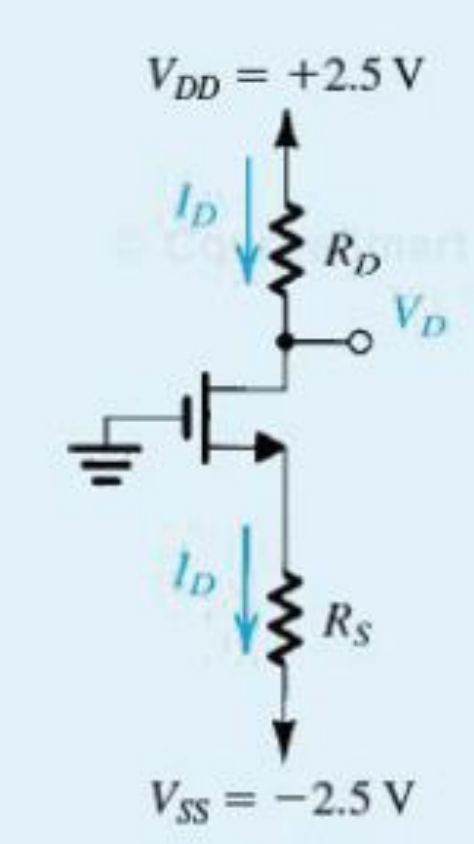
**An n-channel MOSFET operating with $V_{ov}$=0.5V exhibits a linear resistance $r_{DS}$=1kΩ when $v_{DS}$ is very small.**

a) **What is the value of the device trans-conductance parameter $K_n$?**
b) **Assuming λ = 0, what is the value of the current $I_D$ obtained when $v_{DS}$ is increased to 0.5V? And to 1V?**
c) **Assuming an λ = 0.1$V^{-1}$, what is the value of the current $I_D$ obtained when $v_{DS}$ is increased to 0.5V? And to 1V?**

# Example 5.3



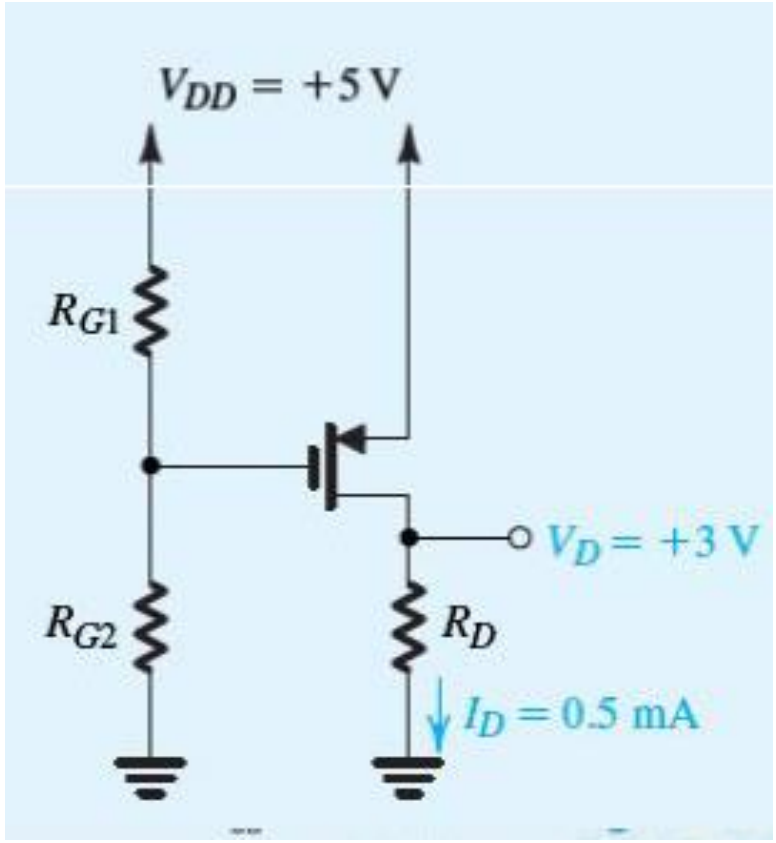
**Assuming λ=0, design the circuit below, that is, determine the values of $R_D$ and $R_S$, so that the transistor operates at $I_D$=0.4mA and $V_D$=0.5V. The NMOS transistor has $V_{th}$=0.7V, $\mu_n C_{ox}$=100μA/V², and W/L=32.**



# Example 5.7



**Assuming λ=0, design the circuit below, so that the transistor operates in saturation with $I_D$=0.5mA and $V_D$=3V. The PMOS transistor has $V_{th}$=-1V, $K_p$=1mA/V$^2$. What is the largest value that $R_D$ can have while maintaining saturation-region operation?**

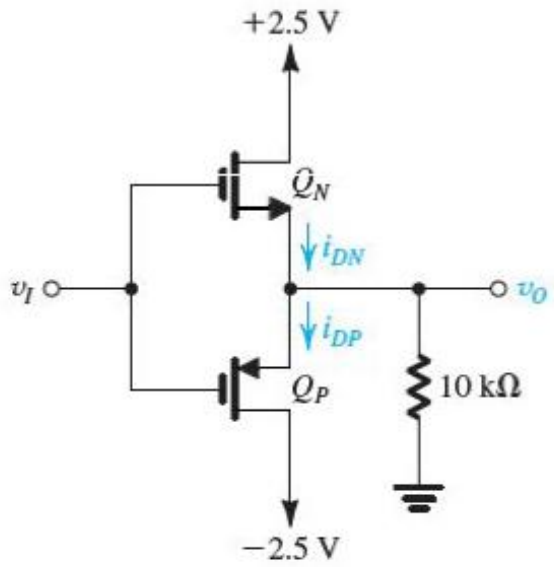


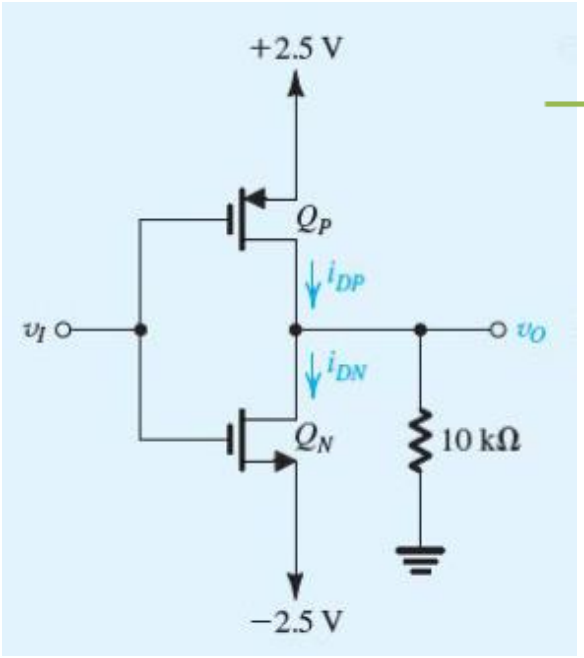
# MOS Behavior → Intuitively



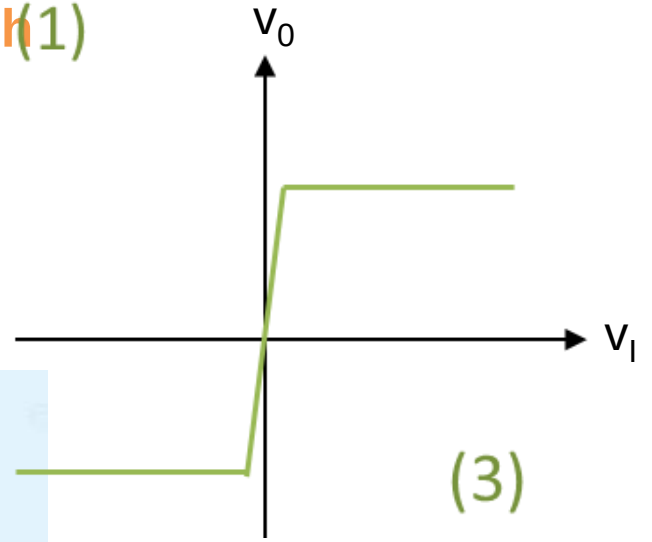
**Choose the plot that best represents each circuit behavior!**

**Circuit (a)** _____ **Circuit (b)** _____




(1)

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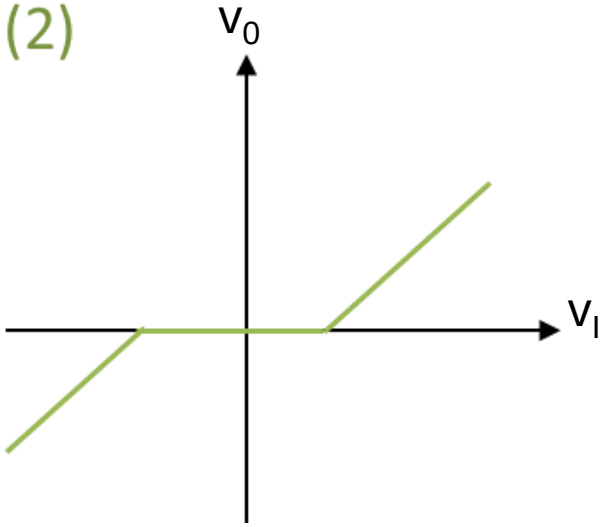


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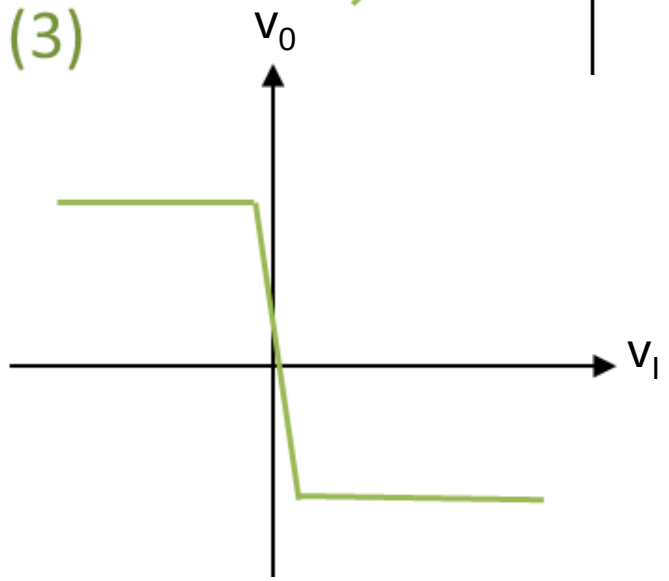
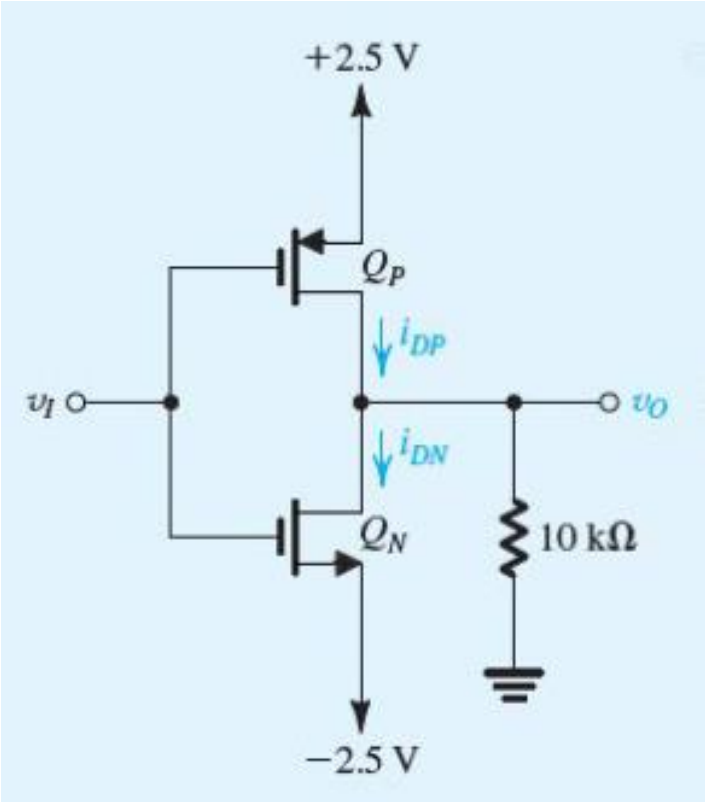


# Example 5.8



**Assuming matched NMOS and PMOS transistors with $V_{thn}=-V_{thp}=1V$, $K_n=K_p=1mA/V^2$ and $\lambda=0$, find the drain currents $I_{Dn}$ and $I_{Dp}$, as well as the voltage $v_o$, for $v_I=0V$, +2.5V, and -2.5V.**

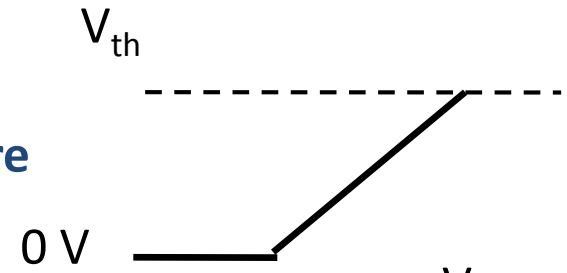


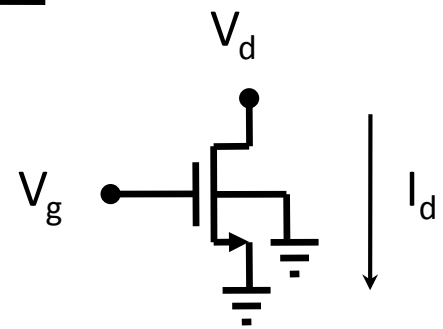
# Last Lecture → MOS

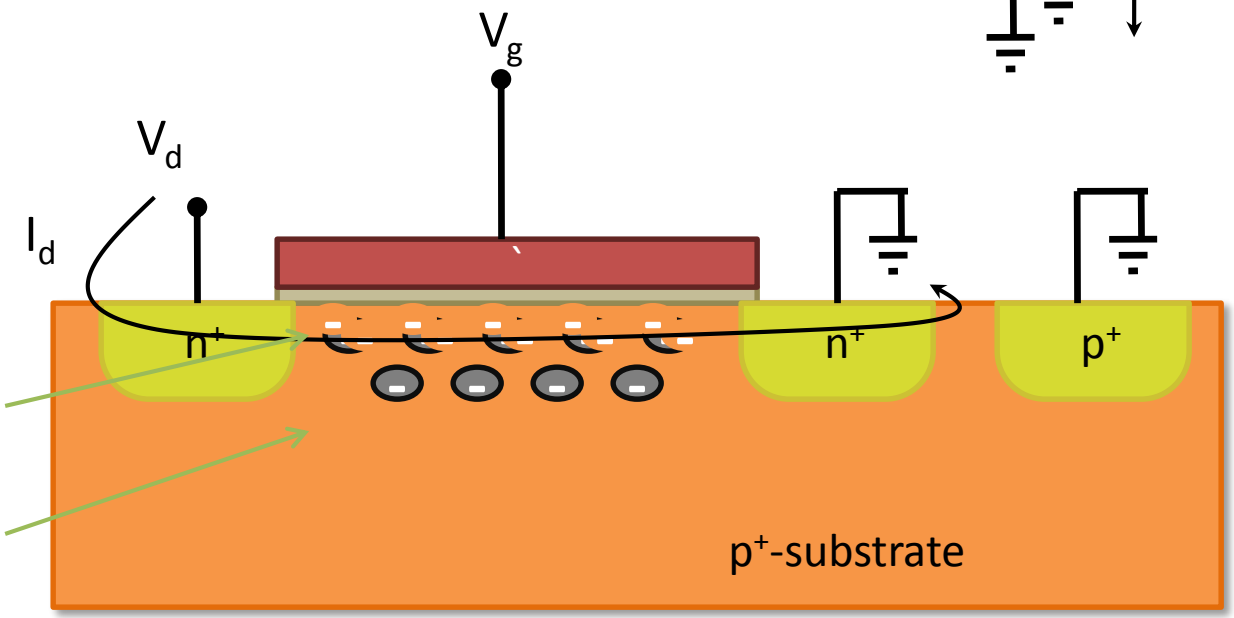
- **Two external voltage sources are required for biasing**
- **Three operation modes:**
  1) **Cut-Off**
  2) **Ohmic**
  3) **Saturation**

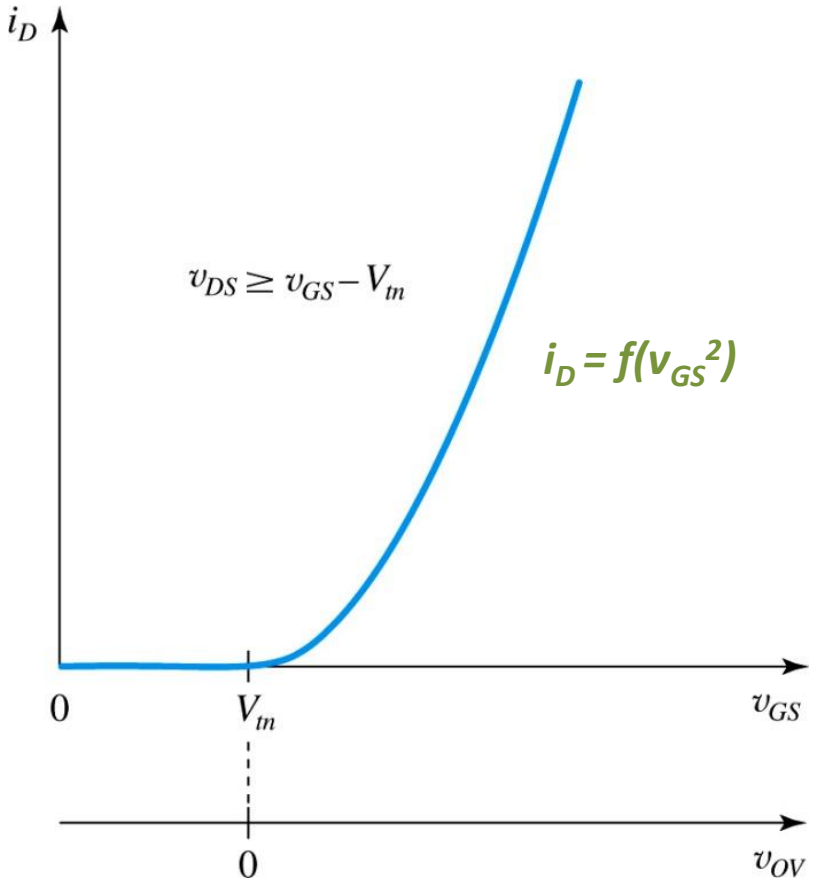
*used for switching!*

*used for amplification!*



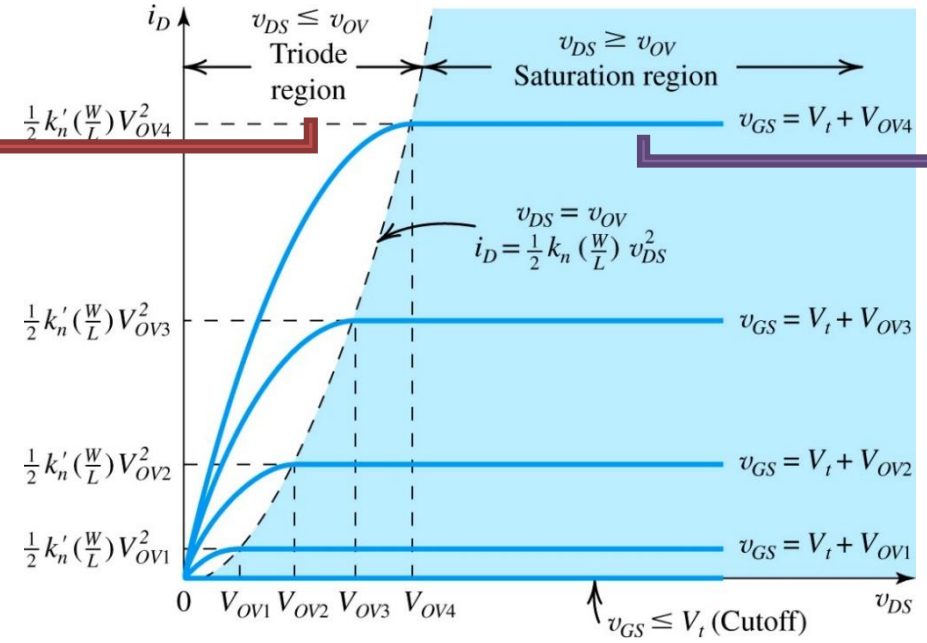



# Last Lecture → MOS DC Analysis

## Triode

- $v_{GS} > v_{th}$
- $v_{DS} < v_{GS} - v_{th} = v_{ov}$
- $i_G = 0$




## Saturation

- $v_{GS} > v_{th}$
- $v_{DS} > v_{GS} - v_{th} = v_{ov}$
- $i_G = 0$

*Transconductance Parameter [A/V²]*

$$k_n' = \mu_n C_{ox}$$

$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_{th})(V_{DS}) - \frac{1}{2}V_{DS}^{\ 2}\right]$$

$$\approx k_n' \frac{W}{L}(V_{GS} - V_{th}) \cdot V_{DS}$$

*Channel Length Modulation Parameter [1/V]*

$$K_n$$

$$I_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$

$$\approx \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_{th})^2$$

# Exercise 5.5

**An n-channel MOSFET operating with $V_{ov}$=0.5V exhibits a linear resistance $r_{DS}$=1kΩ when $v_{DS}$ is very small.**

~~**a) What is the value of the device trans-conductance parameter $K_n$?**~~

~~**b) Assuming λ = 0, what is the value of the current $I_D$ obtained when $v_{DS}$ is increased to 0.5V? And to 1V?**~~

**c) Assuming an λ = 0.1$V^{-1}$, what is the value of the current $I_D$ obtained when $v_{DS}$ is increased to 0.5V? And to 1V?**