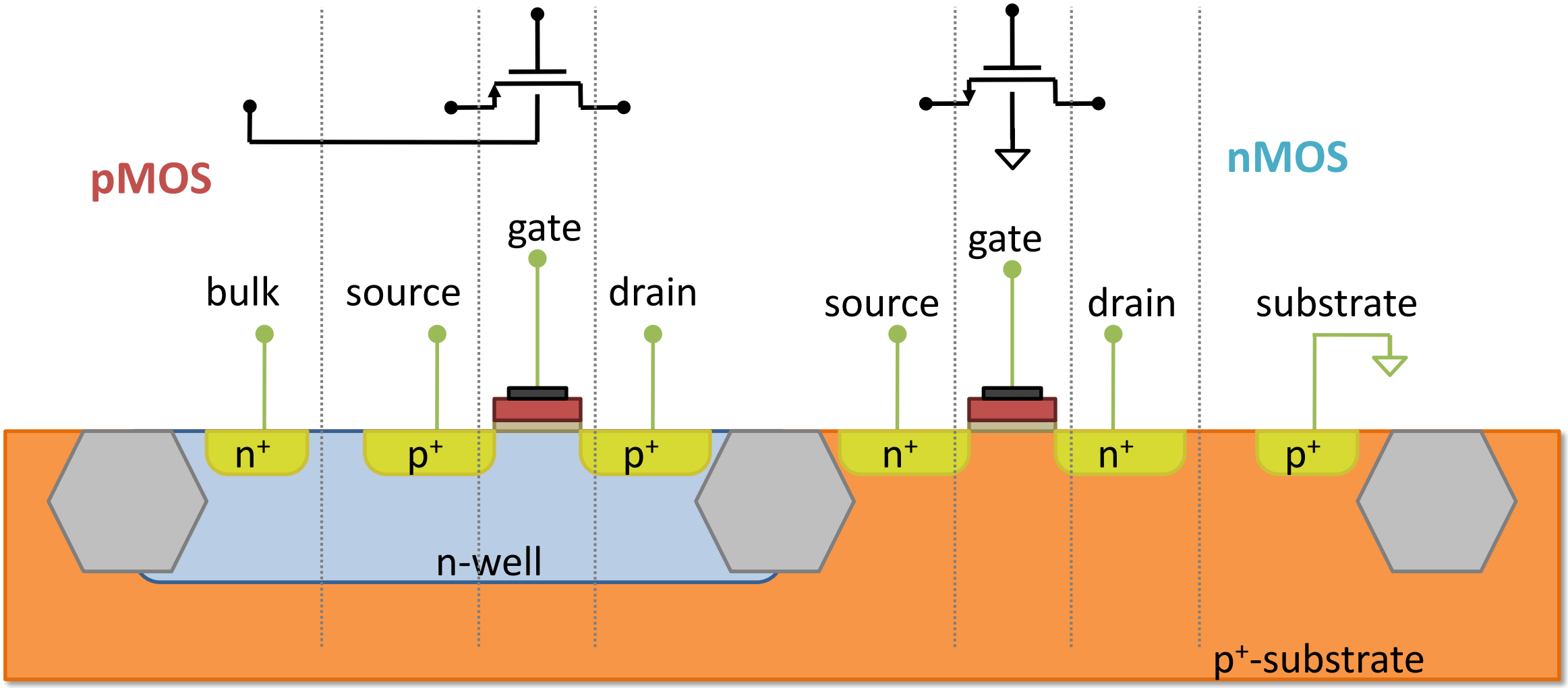
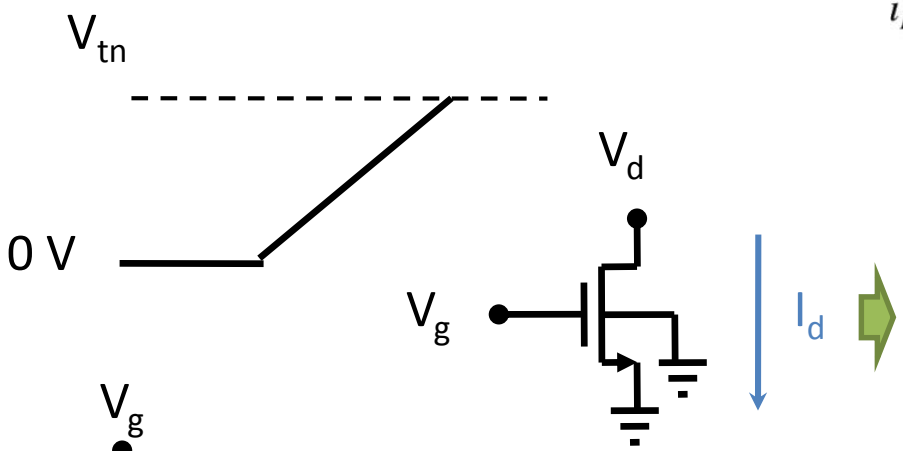
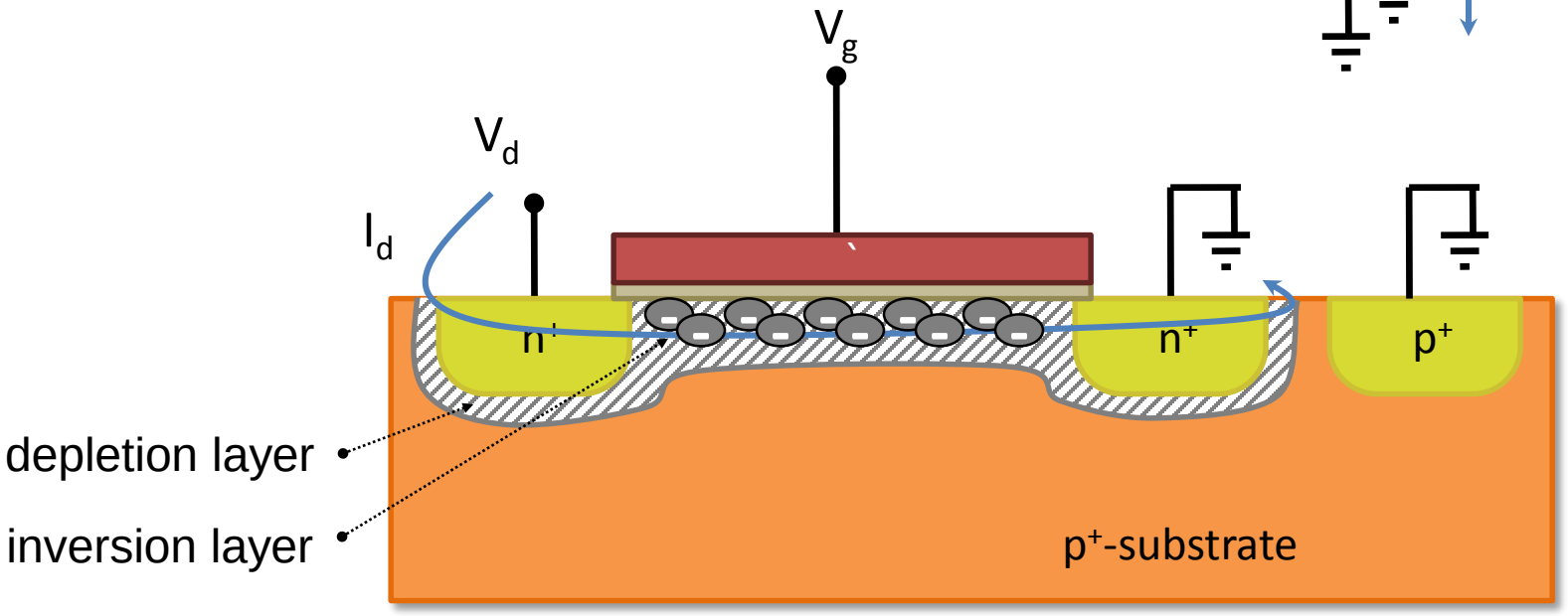
Last Lecture → CMOS Transistor

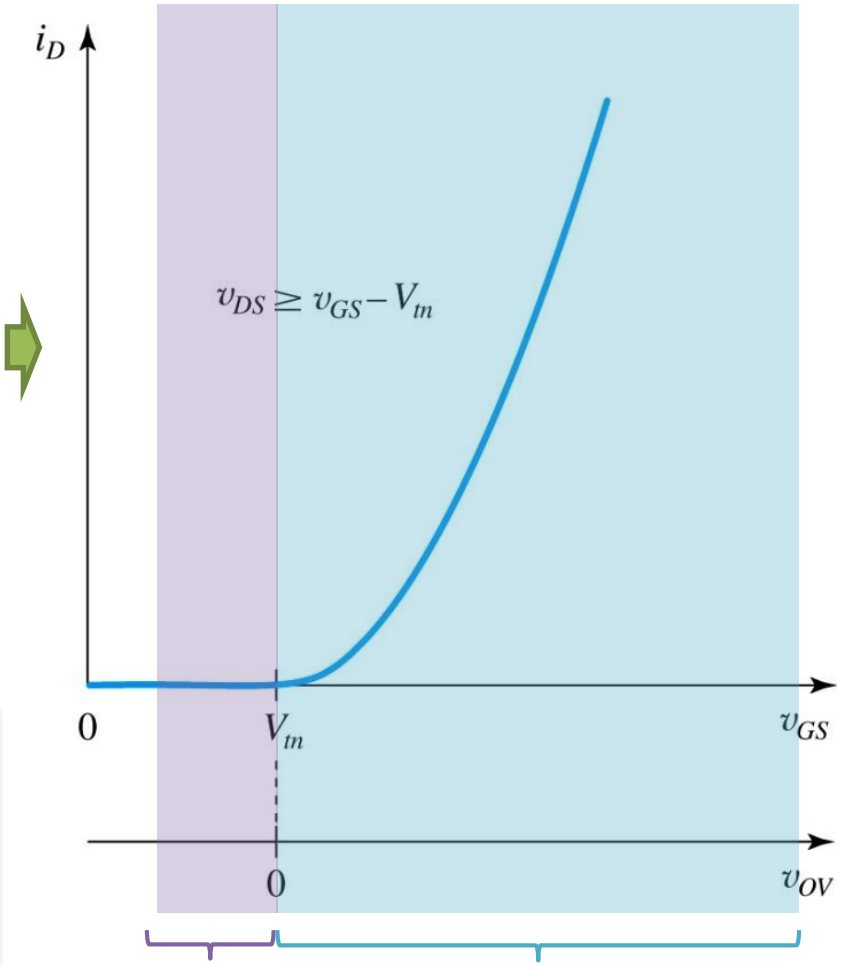


Last Lecture → Operating Region

1) **Cut-Off**
2) **Strong - Inversion**
3) **Weak - Inversion**







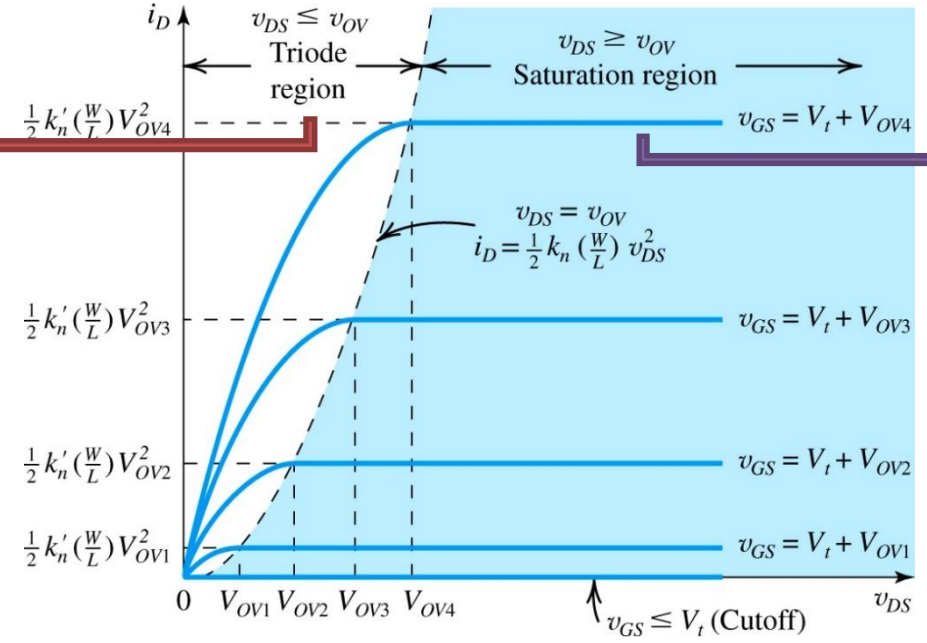
$I_D = f(e^{V_{GS}})$ $I_D = f(v_{GS}^2)$

Last Lecture → Strong Inversion

10/28/2019

Triode

- $v_{GS} > v_{th}$
- $v_{DS} < v_{GS} - v_{th} = v_{ov}$
- $i_G = 0$



Saturation

- $v_{GS} > v_{th}$
- $v_{DS} > v_{GS} - v_{th} = v_{ov}$
- $i_G = 0$

Transconductance Parameter [A/V²]

$$k_n' = \mu_n C_{ox}$$

$$I_D = k_n' \frac{W}{L}\left[(V_{GS} - V_{th})(V_{DS}) - \frac{1}{2}V_{DS}^{\ 2}\right]$$

$$\approx k_n' \frac{W}{L}(V_{GS} - V_{th}) \cdot V_{DS}$$

Channel Length Modulation Parameter [1/V]

$$I_D = \frac{1}{2}\underbrace{k_n' \frac{W}{L}}_{K_n}(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$

$$\approx \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_{th})^2$$

nMOS Large Signal Model

Condition

- **Strong Inversion – Ohmic**

$$I_D = \mu C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{{V_{DS}}^2}{2}\right]$$

$V_{GS} > V_{th}$
$V_{DS} < V_{OV}$

- **Strong Inversion - Saturation**

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$

$V_{GS} > V_{th}$
$V_{DS} > V_{OV}$

- **Weak Inversion - Saturation**

$$I_D = I_0 . e^{\frac{V_{GS} - V_{th}}{nU_T}}$$

$V_{th} - 5 \cdot U_T < V_{GS} < V_{th} - 2 \cdot U_T$

MOSFET Model Parameters

$U_t = kT/q$ → thermal voltage (~25mV @ room temp.)

μ → electron/hole mobility
$\kappa_s = 1/n$ → subthreshold slope coefficient (unit-less)
$C_{ox} = \varepsilon_{ox}/t_{ox}$ → gate oxide capacitance per unit area (F/cm^2)
ε_{ox} → dielectric permittivity of SiO_2
t_{ox} → oxide thickness

$K_n = k_n' \cdot W/L$ → transconductance parameter(A/V^2)
$k_n' = \mu C_{ox}$
γ → body effect coefficient ($V^{1/2}$)
λ → channel-length modulation parameter (V^{-1})

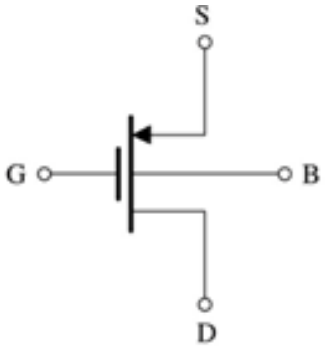
V_{T0} → threshold voltage at V_{SB}=0 (V)
V_T → threshold voltage (V)
ϕ_0 → ≈ surface potential (V)

Weak Inversion vs Strong Inversion?

Weak Inversion	Strong Inversion
Saturation current is exponential in V_{GS}	Saturation current is square law in V_{GS}
V_{DSAT} is constant at approximately 100mV	V_{DSAT} varies linearly with gate voltage
Current flows by diffusion	Current flows mainly by drift
Charge concentrations are small	Charge concentrations are large
Currents are small	Current are large
Good for ultra-low-power operation	Good for high-power operation
Power efficiency is constant with current	Power efficiency is lower
High noise and offset	Low noise and offset
Can work on low power supply voltage	Needs higher power supply voltages
Linearity is hard to achieve	Linearity is easy to achieve
Suited for slow-and-parallel architectures	Suited for fast-and-serial architectures

pMOS Large Signal Model

10/28/2019



Saturation Mode

- $v_{SG} > |v_{tp}|$
- $v_{SD} > v_{SG} - |v_{tp}|$
- $i_G = 0$

$$I_D = \frac{1}{2} k_p{}' \frac{W}{L} (V_{SG} - |V_{tp}|)^2 (1 + \lambda V_{SD})$$

$$\approx \frac{1}{2} k_p{}' \frac{W}{L} (V_{SG} - |V_{tp}|)^2$$

$$V_{ov} = V_{SG} - |V_{tp}|$$

Ohmic Mode

- $v_{SG} > |v_{tp}|$
- $v_{SD} < v_{SG} - |v_{tp}|$
- $i_G = 0$

$$I_D = k_p{}' \frac{W}{L} \left[(V_{SG} - |V_{tp}|)(V_{SD}) - \frac{1}{2} V_{SD}^2 \right]$$

$$\approx k_P{}' \frac{W}{L} (V_{SG} - |V_{tp}|) \cdot V_{SD}$$

pMOS Transconductance Parameter [A/V²]

$$k_p{}' = \mu_p C_{ox}$$

Threshold Voltage

The required voltage to produce and inversion layer.

$$V_T = V_{T0} + \gamma\left(\sqrt{\phi_0 + V_{SB}} - \sqrt{\phi_0}\right)$$

surface potential

body effect coefficient

$$V_{T0} = \phi_{ms} + 2\phi_F + \frac{Q_{dep}}{C_{ox}}$$

The threshold voltage is a function of V_{SB}!!!

work-function difference between the gate metal and the silicon

Fermi level

voltage required to sustain the depletion layer

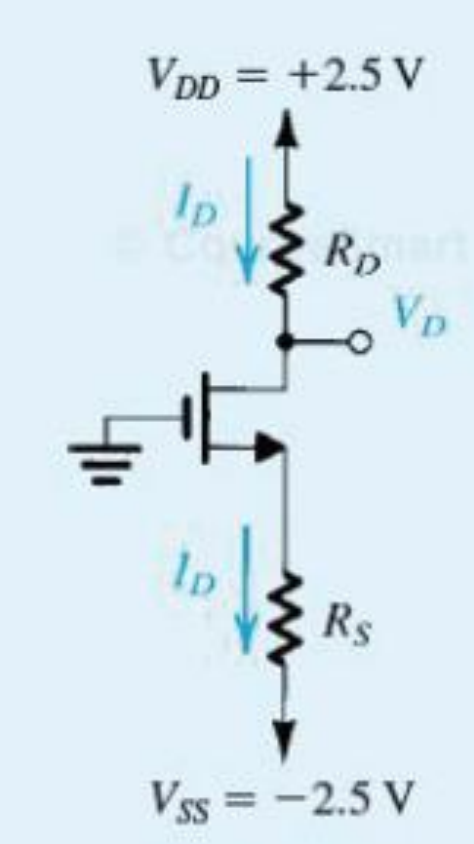
Example 5.2

Consider an nMOS transistor fabricated in a 0.18µm process with L=0.18µm and W=2um. The process technology is specified to have C_{ox}=8.6fF/µm^2, μ_n=450cm^2/V·s, and V_{th}=0.5V.

a) **Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with I_D=100 µ A.**
b) **If V_{GS} is kept constant, find V_{DS} that results in I_D=50µA.**
c) **To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with V_{DS}=0.3V. Find the change in i_D resulting from v_{GS} changing from 0.7V by +0.01V and by -0.01V.**

Example 5.3

Assuming λ=0, design the circuit below, that is, determine the values of R_D and R_S, so that the transistor operates at I_D=0.4mA and V_D=0.5V. The NMOS transistor has V_{th}=0.7V, $\mu_n C_{ox}$=100μA/V², and W/L=32.



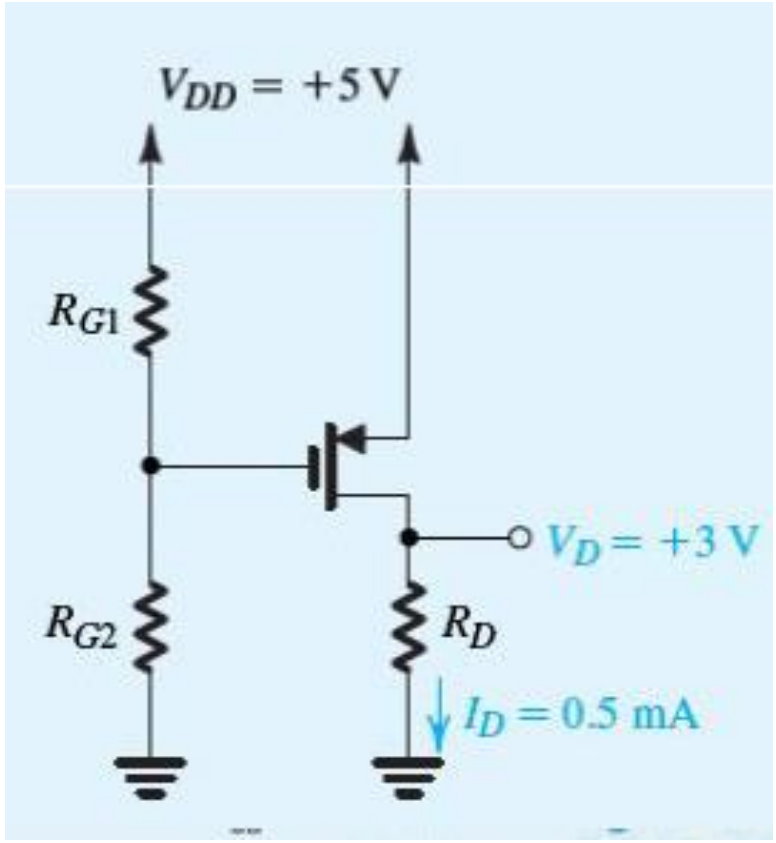
Example 5.5

An n-channel MOSFET operating with V_{ov}=0.5V exhibits a linear resistance r_{DS}=1kΩ when v_{DS} is very small.

a) **What is the value of the device trans-conductance parameter K_n?**
b) **Assuming λ = 0, what is the value of the current I_D obtained when v_{DS} is increased to 0.5V? And to 1V?**
c) **Assuming an λ = 0.1V^{-1}, what is the value of the current I_D obtained when v_{DS} is increased to 0.5V? And to 1V?**

Example 5.7

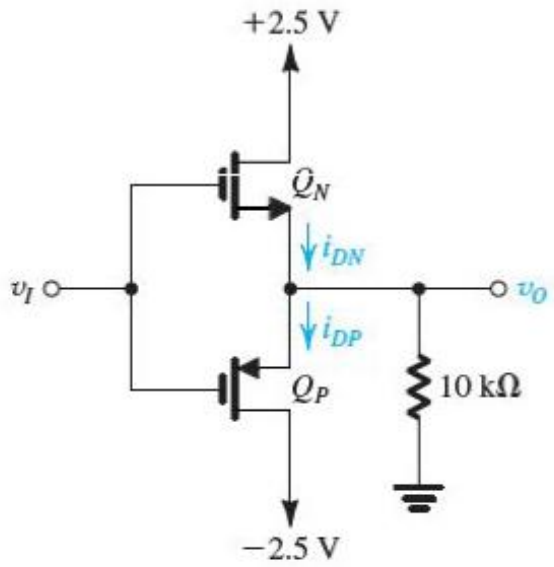
Assuming λ=0, design the circuit below, so that the transistor operates in saturation with I_D=0.5mA and V_D=3V. The PMOS transistor has V_{th}=-1V, K_p=1mA/V^2. What is the largest value that R_D can have while maintaining saturation-region operation?

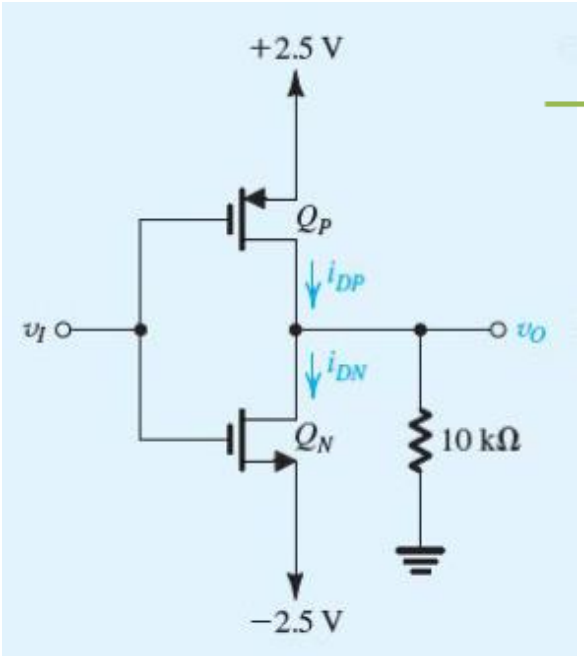


MOS Behavior → Intuitively

Choose the plot that best represents each circuit behavior!

Circuit (a) _____ **Circuit (b)** _____





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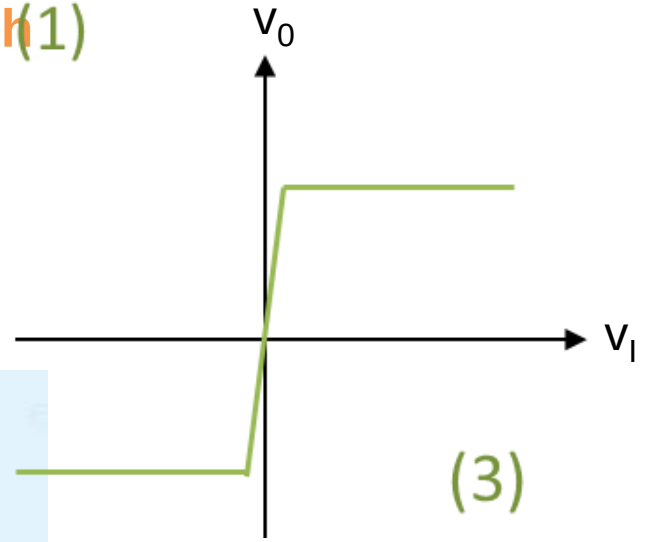
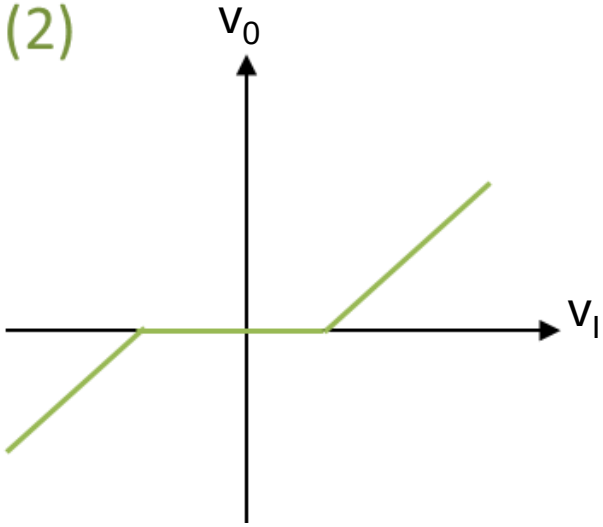
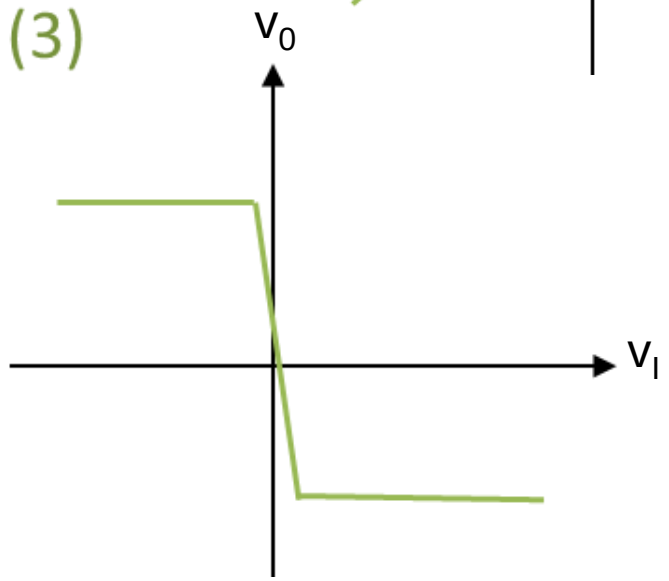


(2)



(3)



Example 5.8

Assuming matched NMOS and PMOS transistors with $V_{thn}=-V_{thp}=1V$, $K_n=K_p=1mA/V^2$ and $\lambda=0$, find the drain currents I_{Dn} and I_{Dp}, as well as the voltage v_o, for $v_I=0V$, +2.5V, and -2.5V.