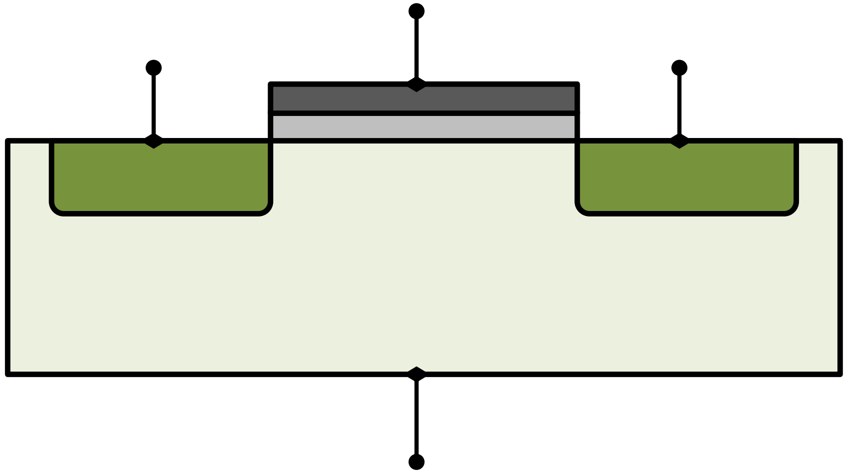
MOSFET → Chapter 5

- **MOS – Metal Oxide Semiconductor**
- **FET – Field-Effect Transistor**
- **4 terminal device**

Advantages:

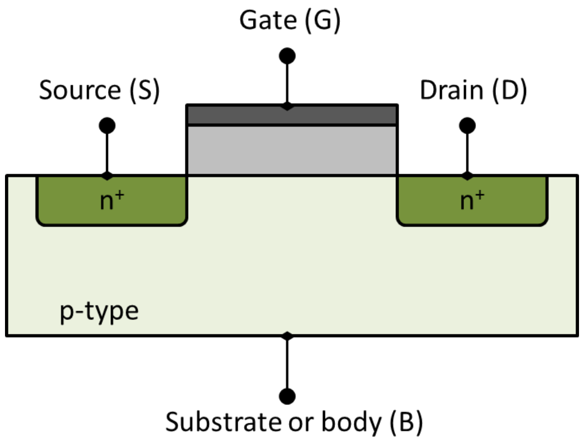
- **Small area; comparatively**
- **Less power**
- **Relatively simple manufacturing process**



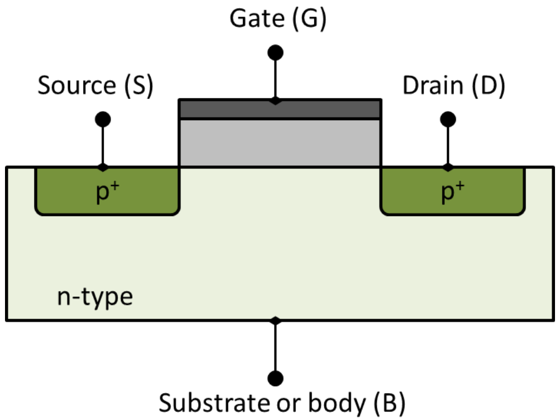
Cross Section Diagram

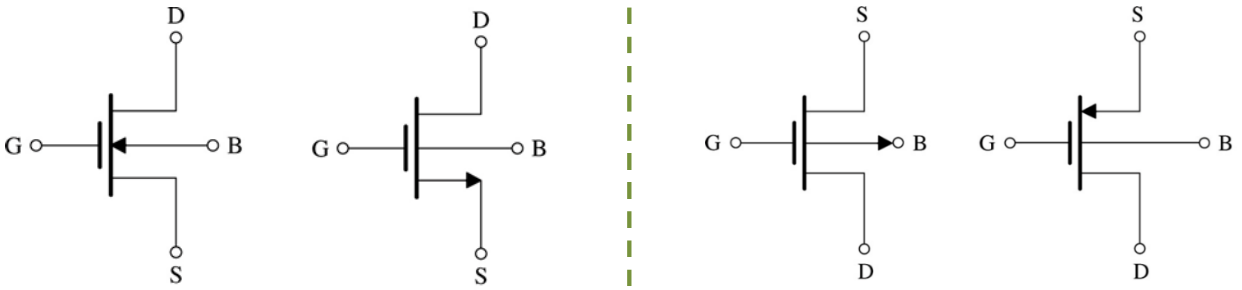
** If the bulk terminal is omitted, it is presumed is connected to the source*

- ***nMOS Transistor***



- ***pMOS Transistor***

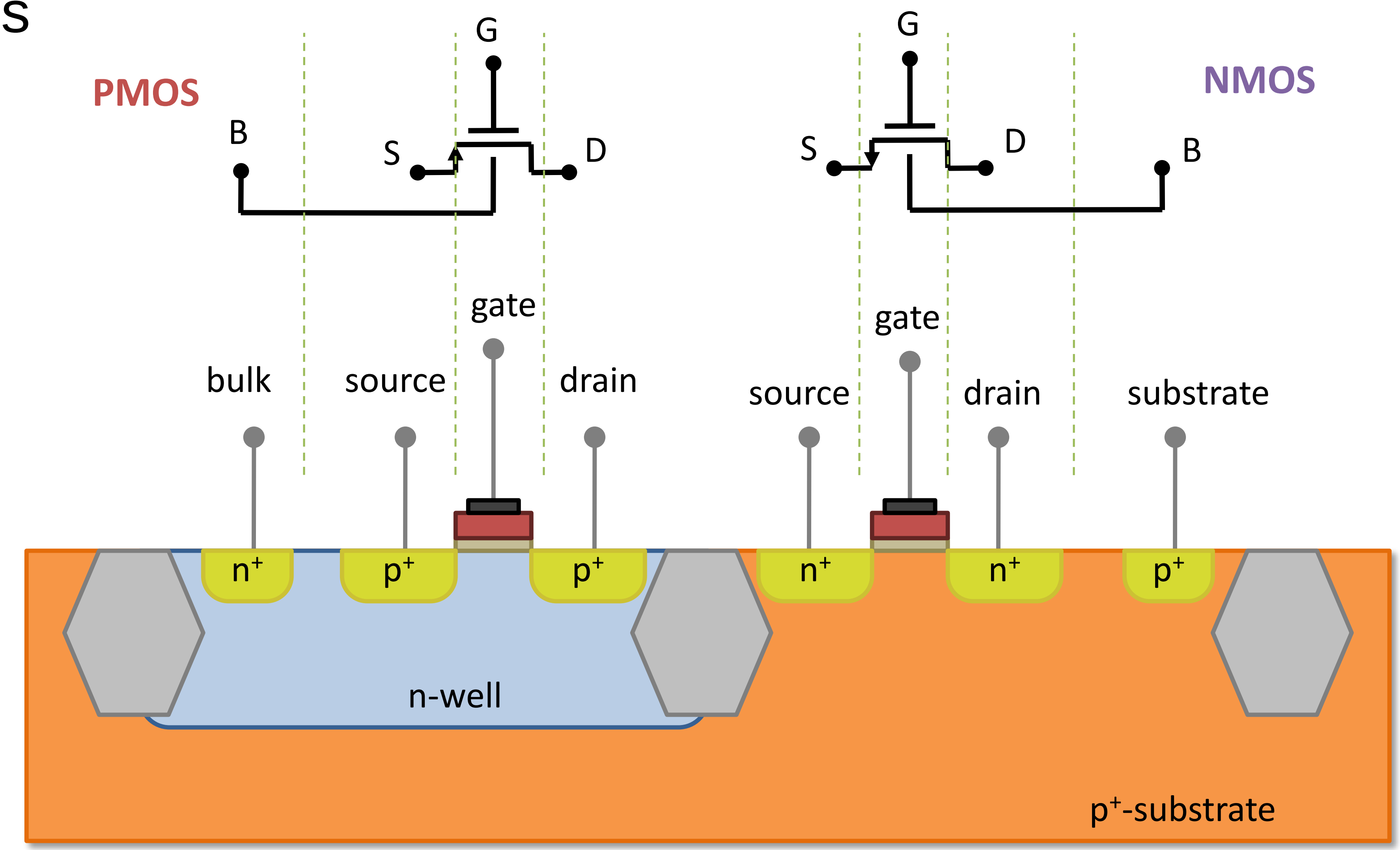




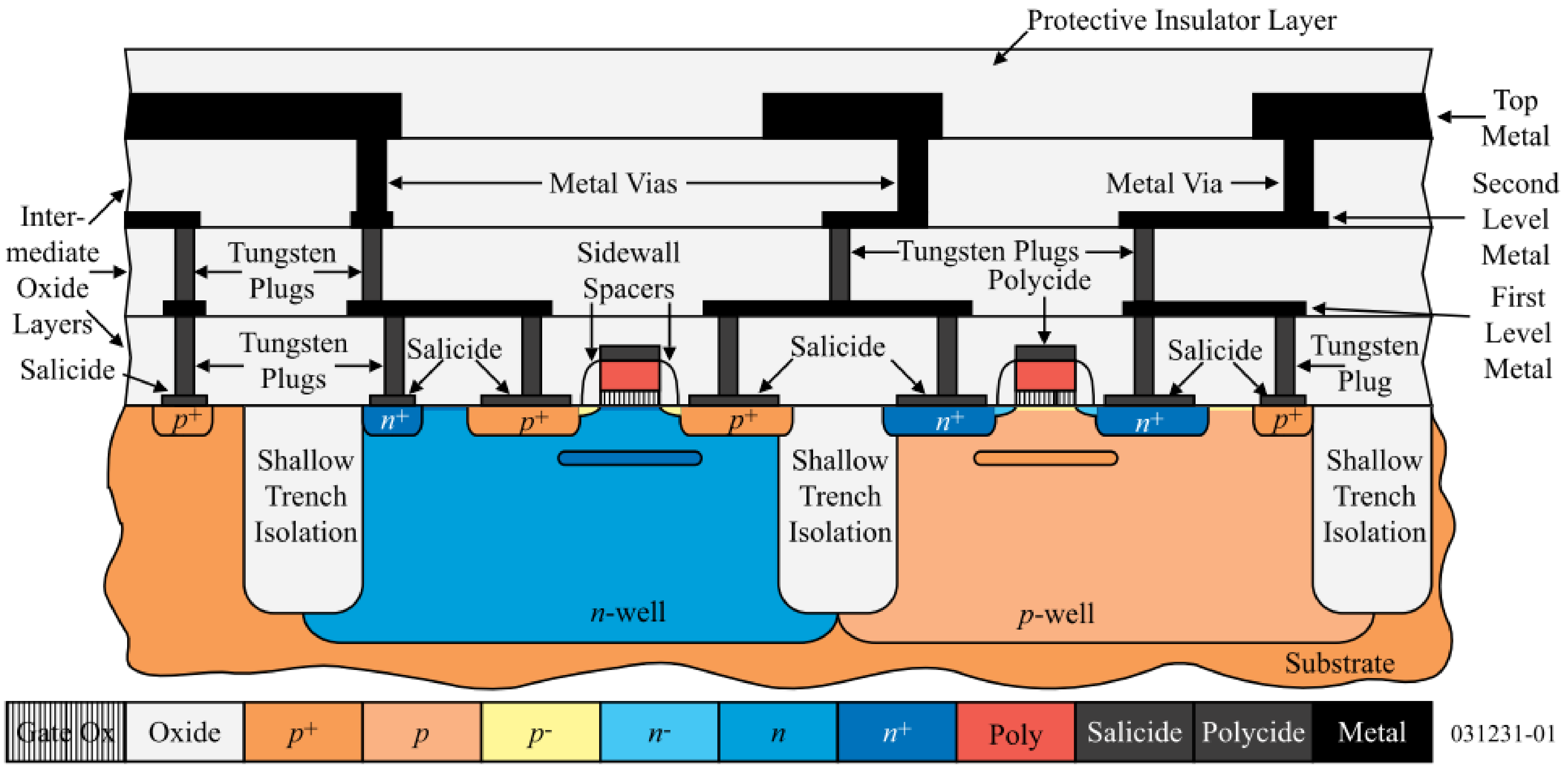
Symbol

CMOS Transistors

Complementary MOS



Modern CMOS Technology

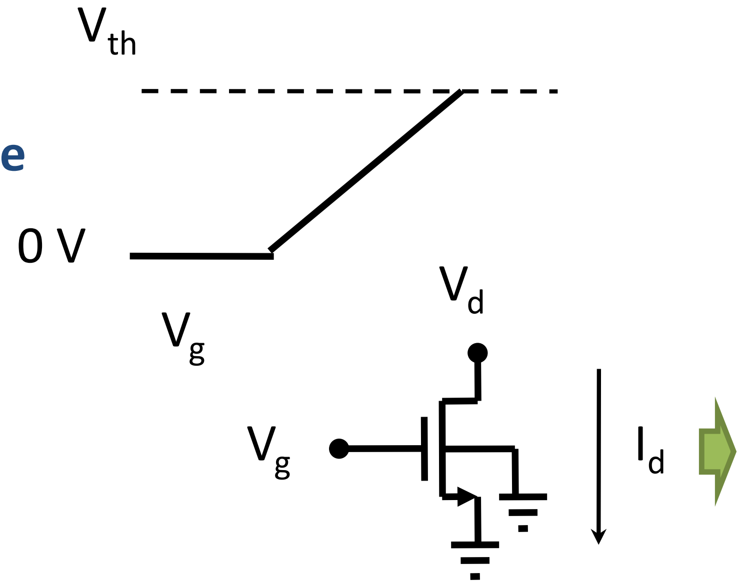


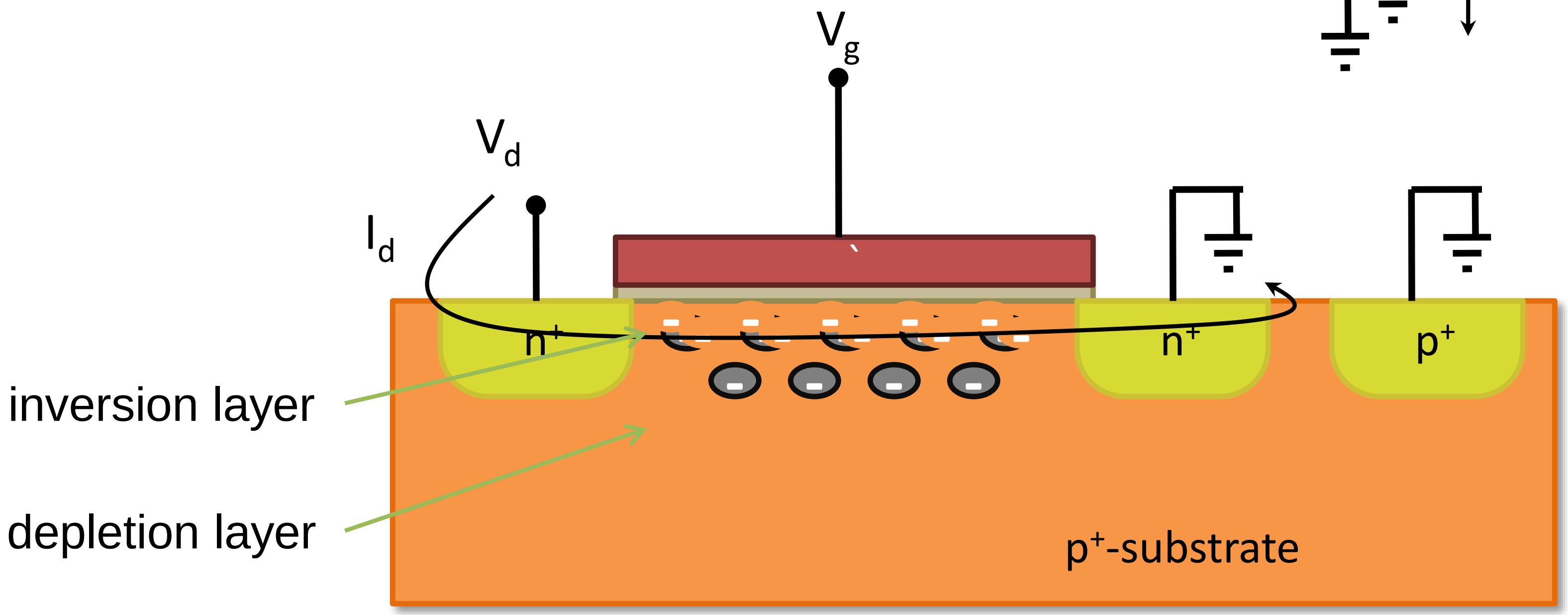
nMOS Operation

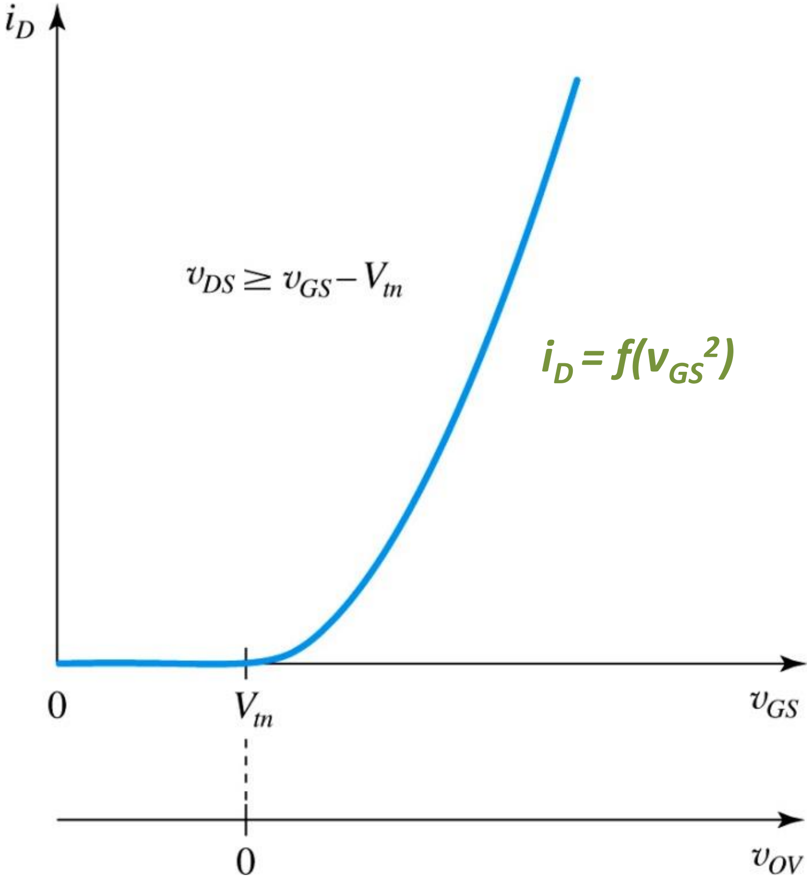
- **Two external voltage sources are required for biasing**
- **Three operation modes:**
  1) **Cut-Off**
  2) **Ohmic**
  3) **Saturation**

used for switching!

used for amplification!







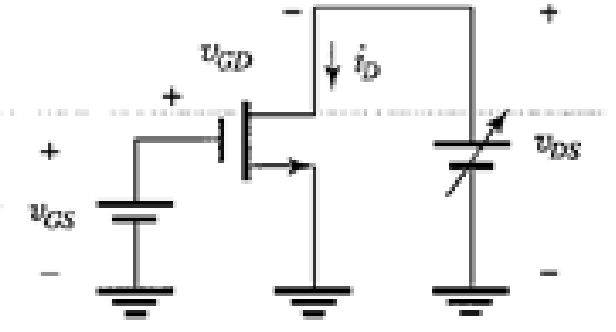
nMOS Operation → Saturation

- $v_{GS} > v_{th}$
- $v_{DS} > v_{GS} - v_{th} = v_{ov}$
- $i_G = 0$

Over-drive Voltage

$$V_{ov} = V_{GS} - V_{th}$$

$i_D = f(v_{GS}, v_{DS})$



K_n

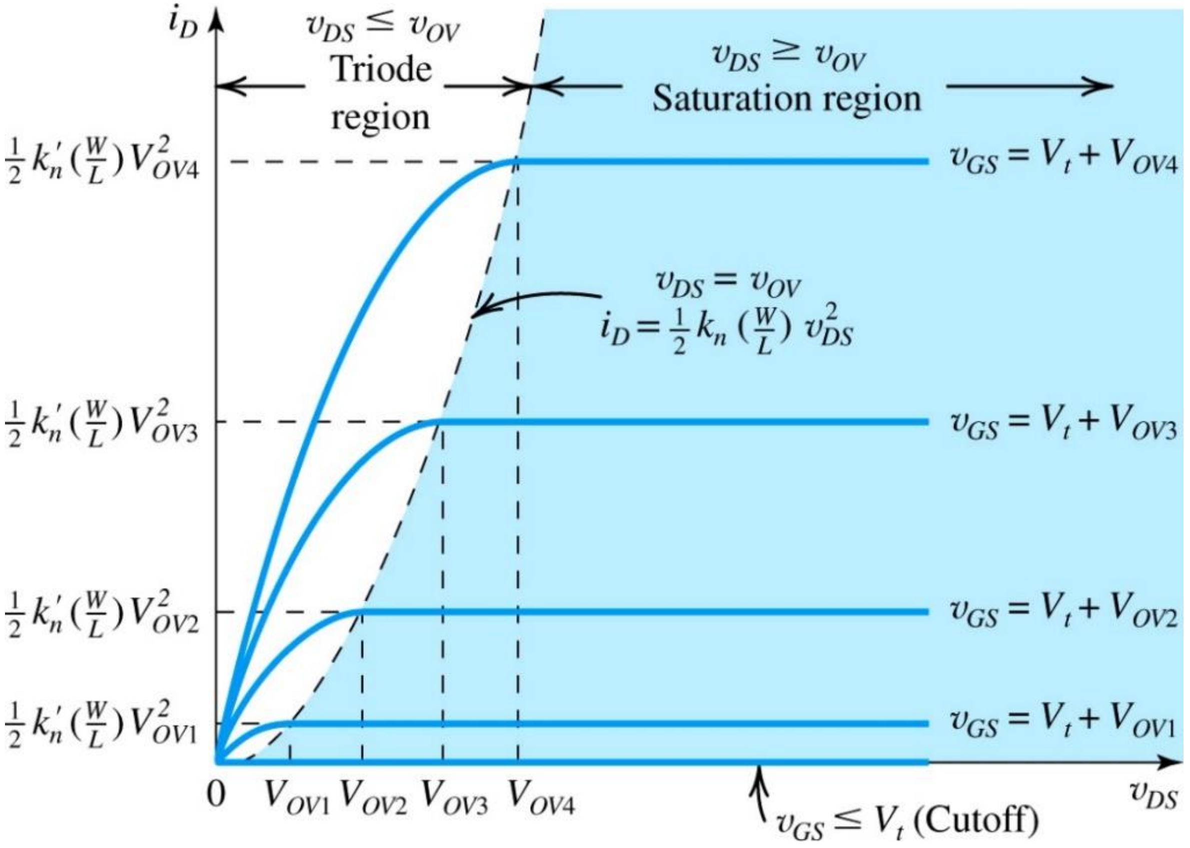
Channel Length Modulation Parameter [1/V]

$$I_D = \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_{th})^2(1+\lambda V_{DS})$$

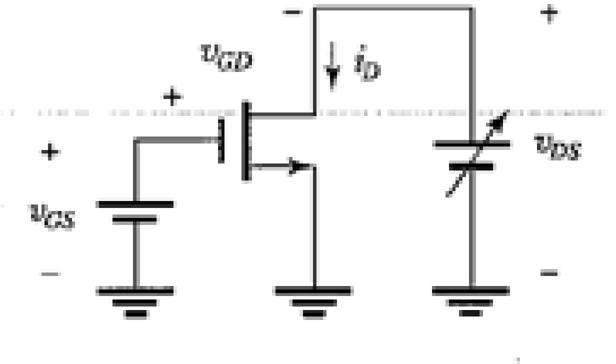
$$\approx \frac{1}{2}k_n'\frac{W}{L}(V_{GS}-V_{th})^2$$

Transconductance Parameter $[A/V^2]$

$$k_n' = \mu_n C_{ox}$$



nMOS Operation → Ohmic



- $v_{GS} > v_{th}$
- $v_{DS} < v_{GS} - v_{th} = v_{ov}$
- $i_G = 0$

$$I_D = k_n'\frac{W}{L}\left[(V_{GS}-V_{th})(V_{DS}) - \frac{1}{2}V_{DS}^{2}\right]$$

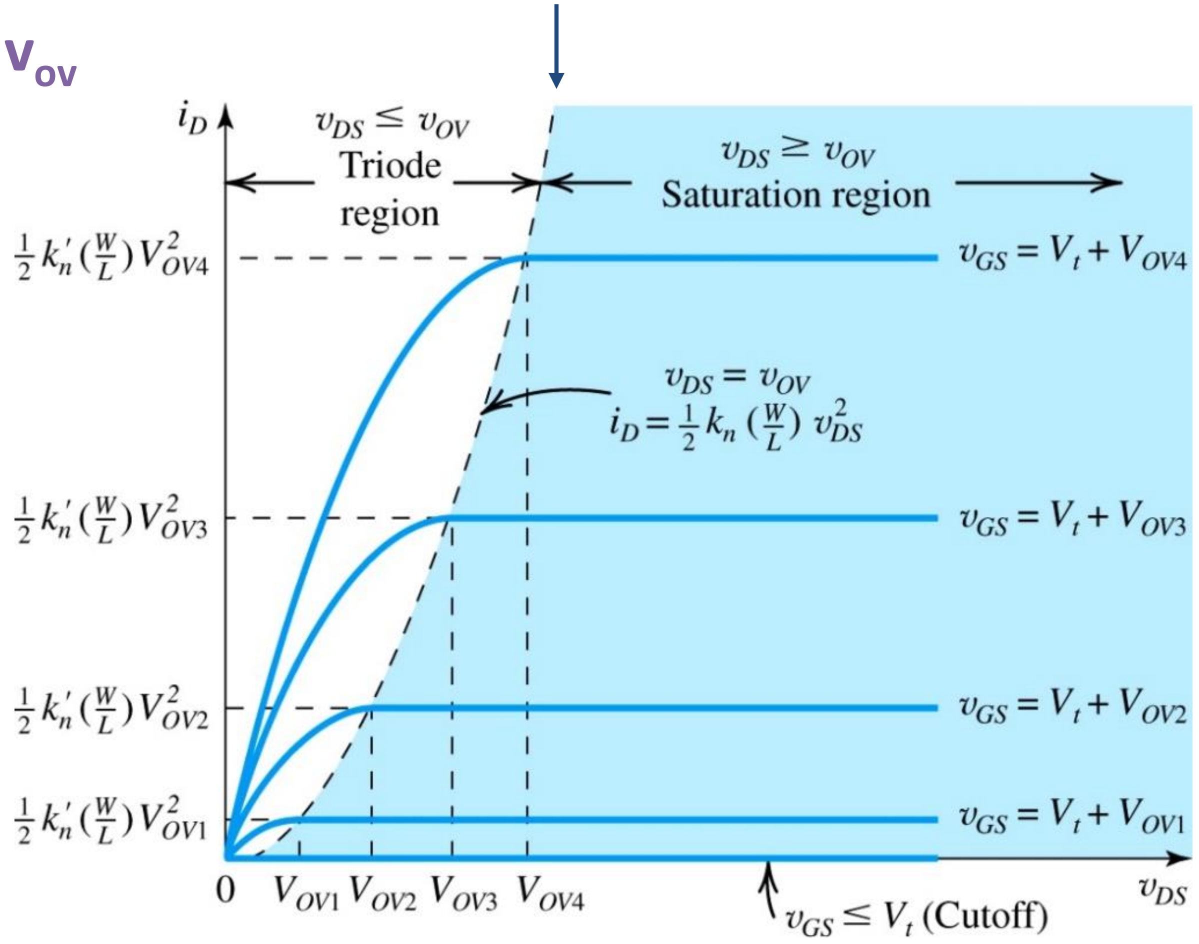
$$\approx k_n'\frac{W}{L}(V_{GS}-V_{th})\cdot V_{DS}$$

$$r_{ds} = \frac{1}{k_n'\frac{W}{L}(V_{GS}-V_{th})}$$

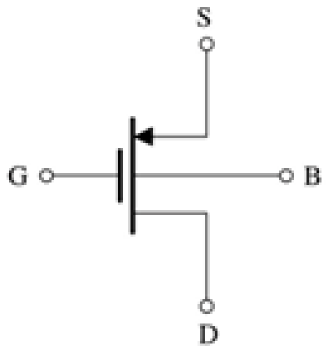
Over-drive Voltage

$$V_{ov} = V_{GS} - V_{th}$$

$i_D = f(v_{GS}, v_{DS})$



Large Signal Model (pMOS)



→ **Saturation Mode**

- **$v_{SG} > |v_{th}|$**
- **$v_{SD} > v_{SG} - |v_{th}| = v_{ov}$**
- ***$i_G = 0$***

$$I_D = \frac{1}{2} k_n{}' \frac{W}{L} (V_{SG} - |V_{th}|)^2 (1 + \lambda V_{SD})$$

$$\approx \frac{1}{2} k_n{}' \frac{W}{L} (V_{SG} - |V_{th}|)^2$$

→ **Ohmic Mode**

- **$v_{SG} > |v_{th}|$**
- **$v_{SD} < v_{SG} - |v_{th}| = v_{ov}$**
- ***$i_G = 0$***

$$I_D = k_n{}' \frac{W}{L} \left[(V_{SG} - |V_{th}|)(V_{SD}) - \frac{1}{2} V_{SD}{}^2 \right]$$

$$\approx k_n{}' \frac{W}{L} (V_{SG} - |V_{th}|) \cdot V_{SD}$$

Example 5.2

Consider an nMOS transistor fabricated in a 0.18µm process with L=0.18µm and W=2um. The process technology is specified to have C_{ox}=8.6fF/µm^2, μ_n=450cm^2/V·s, and V_{th}=0.5V.

a) Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with I_D=100 µ A.
b) If V_{GS} is kept constant, find V_{DS} that results in I_D=50µA.
c) To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with V_{DS}=0.3V. Find the change in i_D resulting from v_{GS} changing from 0.7V by +0.01V and by -0.01V.