- $Z_L \neq Z_0$ creates a potential inconsistency at the termination leading to a $v_B \neq 0$ and $i_B \neq 0$

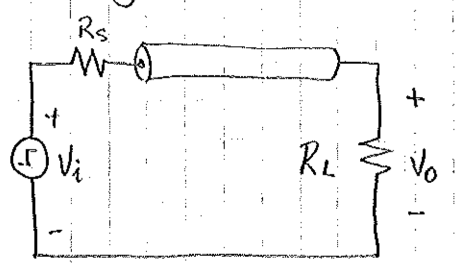
Reflection Coefficient

$$\Gamma = \left.\frac{v_B}{v_F}\right|_{\text{Right End}} = \left.\frac{v_F}{v_B}\right|_{\text{Left End}} = \frac{\frac{Z_L}{Z_0} - 1}{\frac{Z_L}{Z_0} + 1} = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (13)$$

$$|\Gamma| \leq 1$$

Note that for $Z_L = \infty \Rightarrow \Gamma \to 1$ and $Z_L = 0 \Rightarrow \Gamma \to -1$

Case analysis:



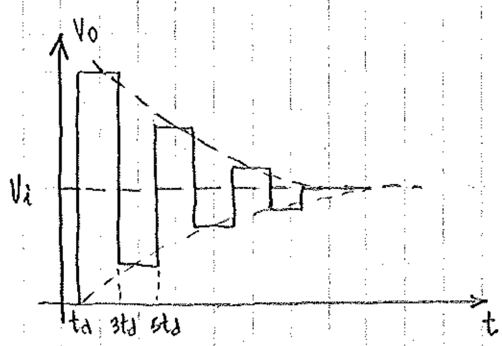
For this circuit
$R_S = 10\,\Omega$
$R_L = 10\,K$
$R_0 = 100\,\Omega$

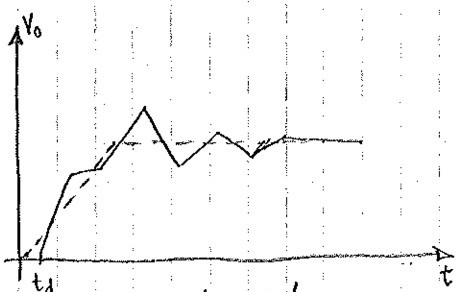
- $R_S \ll R_0 \ll R_L$
- Assuming $t_r \ll t_d$
- V_o will be a damped oscillation
- V_o could be interpreted as multiple oscillations.
- Oscillations are avoided by terminating the line with Z_0
- Propagation delay per unit length of an unloaded transmission line

$$\delta = t_d / l = \sqrt{LC} \qquad \delta = 1/c$$

- In an homogeneous medium

$$\delta = \sqrt{\mu \varepsilon}$$





$t_d \ll t_r$

$\mu = \mu_r \mu_0 \to$ permeability (magnetic response)

$\varepsilon = \varepsilon_r \varepsilon_0 \to$ permittivity (electric field response)

For digital lines $\mu_r \approx 1$, $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, and $\mu_0 = 4\pi \times 10^{-7}$ H/m

Thus $\delta = 33.35 \sqrt{\varepsilon_r}$ ps/cm

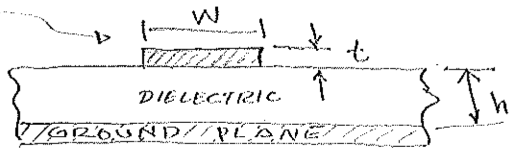
- If neither the source or load impedance match Z_0 then multiple reflections will occur

Let Γ_L and Γ_S be the reflexion indices of load & source, respectively

When Γ_S and Γ_L have opposite signs, reflections alternate causing ringing

Traces on PCBs (strips & microstrips)

- Microstrip



$$Z_0 = \frac{87 \ln\left(\frac{5.98h}{0.8w + t}\right)}{\sqrt{\varepsilon_r + 1.41}}$$

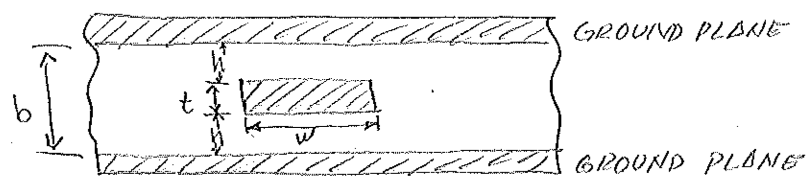
ε_r = relative dielectric constant of insulator

Valid for $0.1 < w/h < 0.3$
$1 < \varepsilon_r < 15$

The propagation delay is dependent only on ε_r

$$\delta = 33.35\sqrt{0.475\varepsilon_r + 0.67} \ \text{ps/cm}$$

- Strip



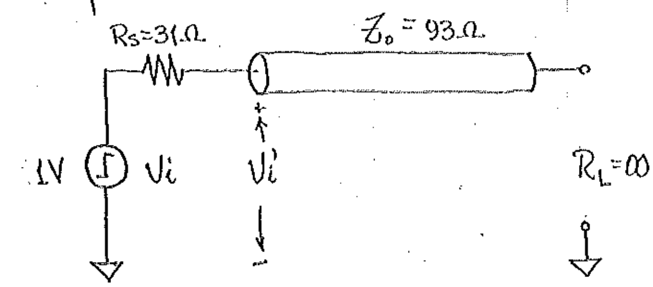
$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4b}{0.67\pi(0.8w + t)}\right]$$

Valid for $\frac{w}{(b-t)} < 0.35$ and $t/b < 0.25$

$$\delta = 33.35\sqrt{0.475\varepsilon_r + 0.67}$$

- On PCBs traces are highly predictable
- Transverse Electromagnetic mode: operation of strip & μstrip

Example:



- Mismatched line at both ends
- Lattice diagram used to keep track of
  - Magnitude
  - Polarity
  - Time

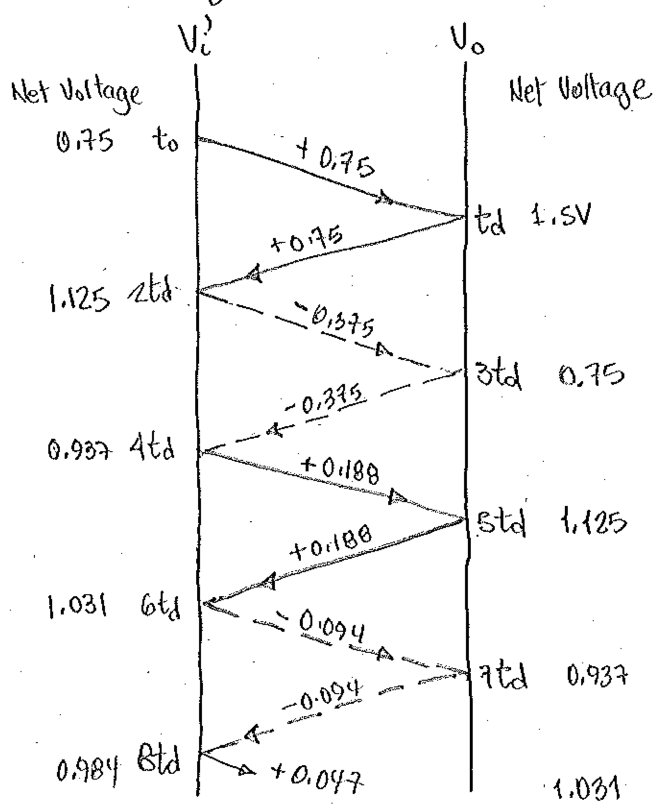
Assuming step is applied at $t = t_0$

$$V_i' = \frac{Z_0}{Z_0 + R_s} V_i = \frac{93}{93+31} \times 1 = 0.75V \quad \leftarrow \text{This is } V_F \text{ for } t_0$$

Since $R_s \neq Z_0 \neq R_L \Rightarrow$ Relections will develop

$$\Gamma_\ell = \frac{\infty - 93}{\infty + 93} = +1 \qquad \Gamma_s = \frac{31-93}{31+93} = -0.5$$

Lattice Diagram:



- Input @ t_0 is 0.75V
- After td, V_0' is $V_i' + \Gamma_\ell (V_i') = 1.5V$
- After 2td the voltage at source

$$V_i + \underbrace{\Gamma_\ell V_i}_{V_r} + \Gamma_s \underbrace{\Gamma_\ell V_i}_{V_r} = 1.125$$

reflexion $\Gamma_s \Gamma_\ell V_i$

- After 3td at the load

$$V_0^2 = V_i^2 + \Gamma_\ell V_r = 1.125 - 0.375 = 0.75$$

⋮

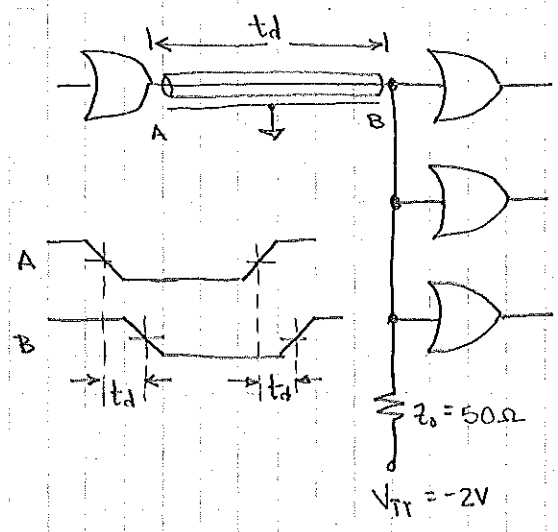
and so-on

Termination Techniques for Fast circuits :

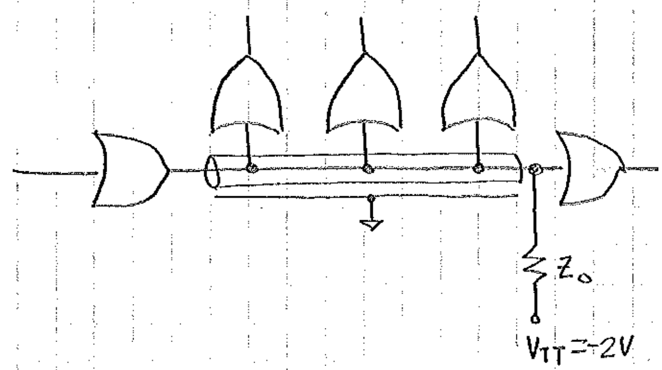
- Parallel Termination
- Serial Termination

Parallel Termination : Eliminates reflections at the end of the transmission line.

loads can be lumped at the end of the line or distributed along the line



PARALLEL TERMINATION
WITH LUMPED LOAD



PARALLEL TERMINATION
WITH DISTRIBUTED LOAD

- ECL output stage designed to drive a 50Ω line terminated with Z_0 with no reflections (lumped load model). Auxiliary supply V_{TT} required
- In distributed load model, the edge propagation decreases with x along the TL due to the distributed load capacitance

In this case the propagation delay and characteristic impedance will be:

$$\delta' = \sqrt{L(C+C_d)} = \sqrt{1+\frac{C_d}{C}}\,\delta$$

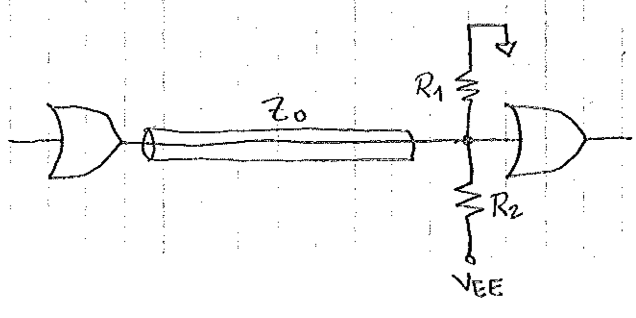
and

$$Z_0' = \sqrt{\frac{L}{C+C_d}} = \left(\frac{1}{\sqrt{1+C_d/C}}\right) Z_0$$

where C_d is the gate input capacitance (distributed load)

*** See example ***

- An alternative using a single supply :



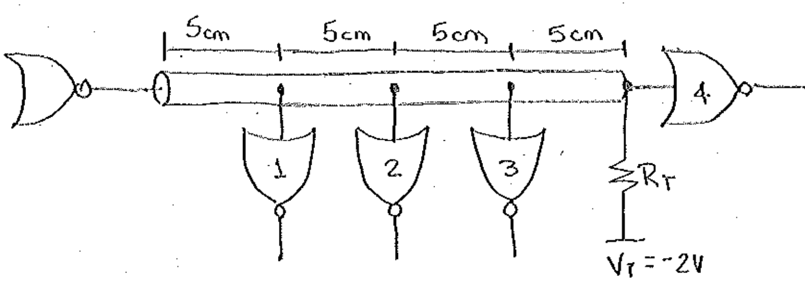
$$R_2 = \frac{V_{EE}}{V_T} Z_0 = 2.6 Z_0$$

R_1 = Selected such that $R_1 \| R_2 = Z_0$

$$R_1 = \frac{R_2}{1.6}$$

Parallel Termination Example:

- Four identical ECL gates
  - Total capacitance 13 pF
  - Spaced at 5cm intervals
  - 20cm-long microstrip
  - $Z_0 = 68\,\Omega$
  - $\varepsilon_r = 5$
- Find the parallel terminating resistor for no reflection @ end



1) Line capacitance $C = \dfrac{\delta}{Z_0}$

$$\delta = 33.35\sqrt{0.475\varepsilon_r + 0.67} = 33.35\sqrt{3.045} = 58.19$$

$$C = \frac{58.19}{68} = 0.86\,\text{pF/cm}$$

$$C_d = \frac{C_{Total}}{L} = \frac{13\,\text{pF}}{20\,\text{cm}} = 0.65\,\text{pF/cm}$$

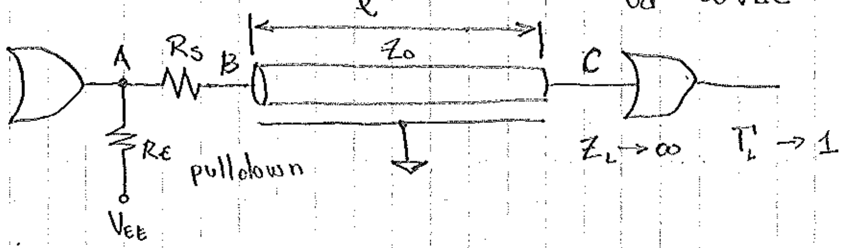
So $$Z_0' = \frac{Z_0}{\sqrt{1 + C_d/C}} = \frac{68}{\sqrt{1 + 0.65/0.86}} = 51.26\,\Omega$$

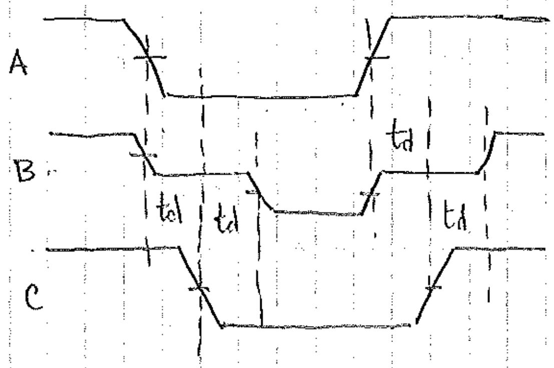
So $\boxed{R_T = 51\,\Omega}$

Series termination: Eliminates reflections at the transmitting end of the line.

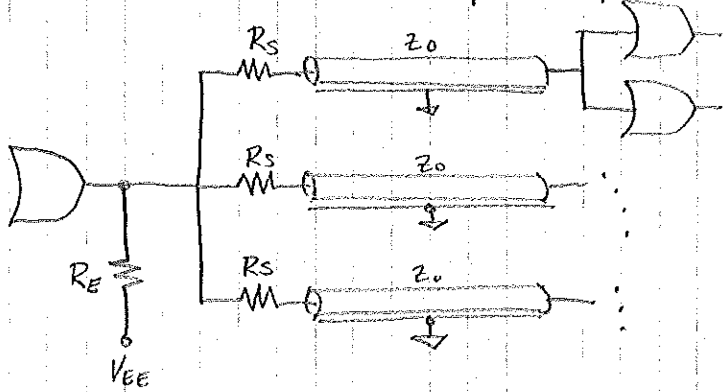
Inserts a SERIES resistor to the driver output

$t_d = l\sqrt{LC}$





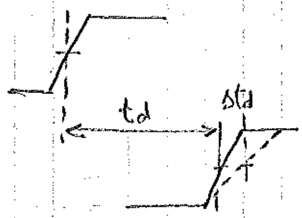
- The series termination is useful for open-ended lines or Load impedances very high
- The sum of R_s plus the driver output impedance are matched to Z_0
- Reduced crosstalk and reduced power dissipation. Single supply
- Cannot be used with distributed load (half logic swing propagating down the line)
- Slower than parallel termination (larger series impedance)
- Parallel lines used to improve speed



- A low-impedance parallel-terminated line has shorter td than a series terminated line with equivalent fan-out. However multiple series terminated operate faster.

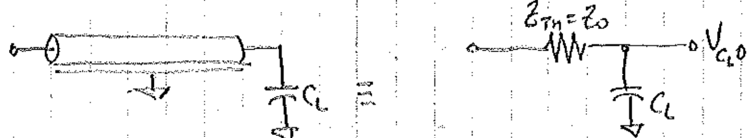
- A capacitive load at the end of a T.L. inserts an additional delay to the signal propagation. (Slows down the rising time)

$$t_d' = t_d + \Delta t_d$$

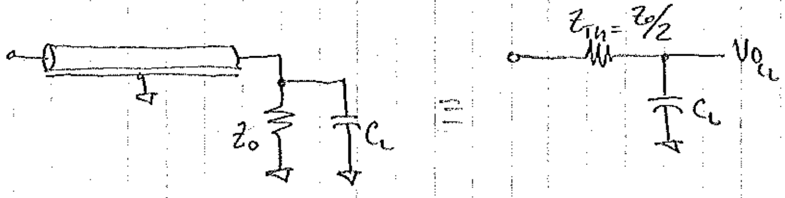


The additional delay can be computed with an RC model in either the series or parallel model.

Series



Parallel



Solution found using Laplace $t_{rise\,input} = 0.8\alpha$; $\alpha \leftarrow$ Ramp time