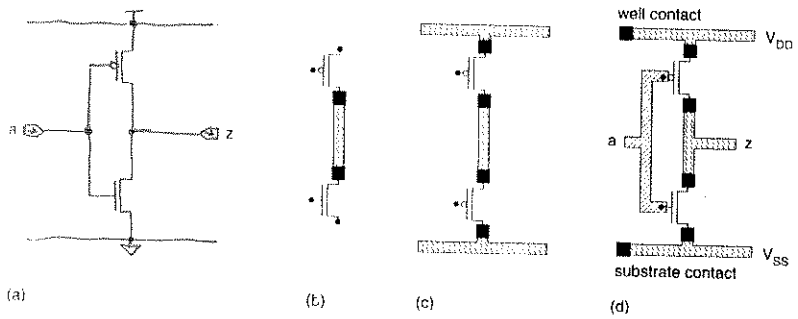
LAYOUT DESIGN OF SIMPLE GATES

- Understanding your book
  - Explanations use unit sized transistors. Actual dimensions are obtained from a detailed layout applying design rules
  - A symbolic layout style is used:
    - No select layers
    - No wells
    - No contact surrounds

- Inverter layout



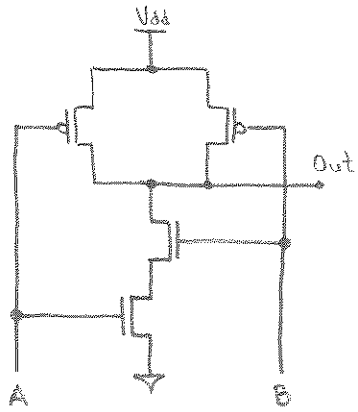
- Begin with a schematic diagram.
- Recall that two physically different interconnect layers might interact

Ex.:

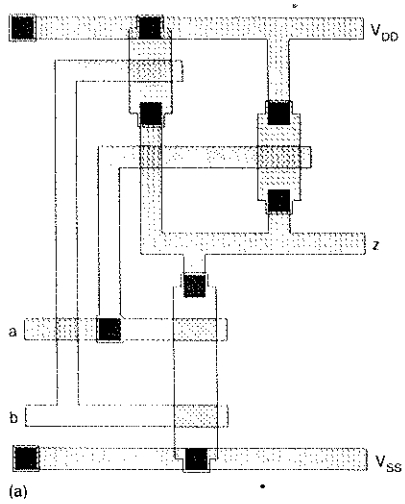
- The connection of the two drains in the inverter.
  N-MOS source & drain are n-diff } cannot be directly connected.
  P-MOS " " " p-diff } Need interdrain connect. & two contacts.
  Use metal.

- The V_{DD} & V_{SS} connection are performed similarly
- The intergate connection can be done in poly
- The substrate (well) connection needs a contact (each)
- The transistors are realized crossing poly and diffusion areas
- Topological transformations might allow nonplanar connection schemas.
  - * Vertical vs. Horizontal diff transistors
  - * Multi-metal layers to allow traversal of cell
  - * Single metal layers crossing the transistor.
- Connection trade-offs might affect performance, area, or both.

Layout of NAND & NOR gates



CMOS NAND gate



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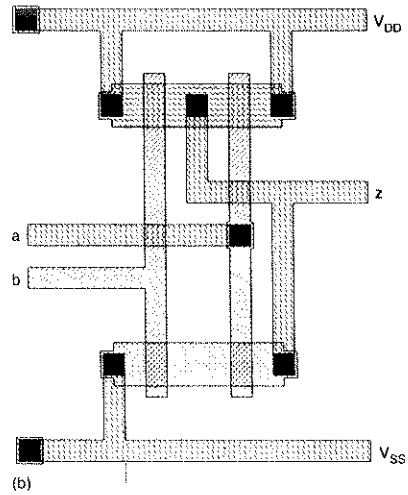

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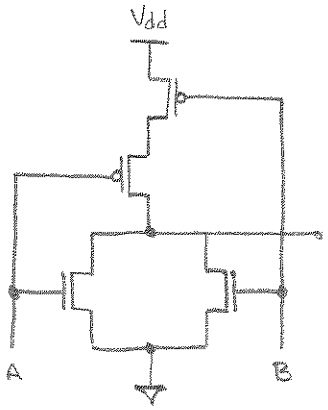
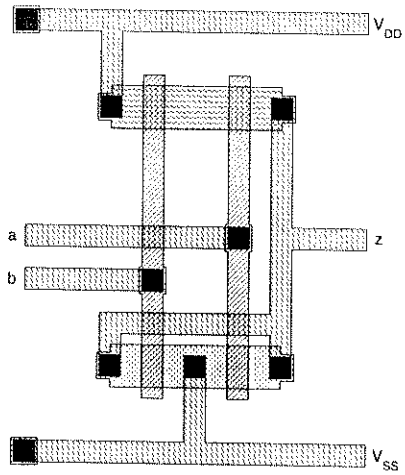


CMOS NOR gate



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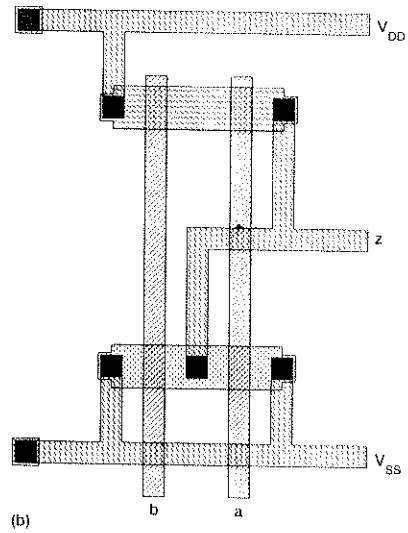

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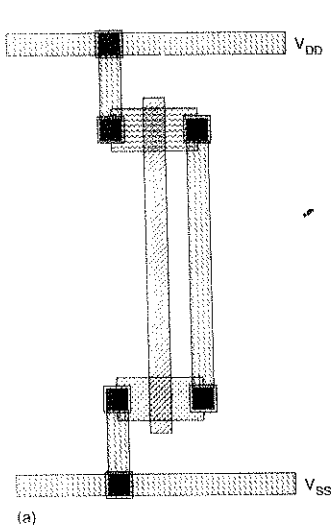

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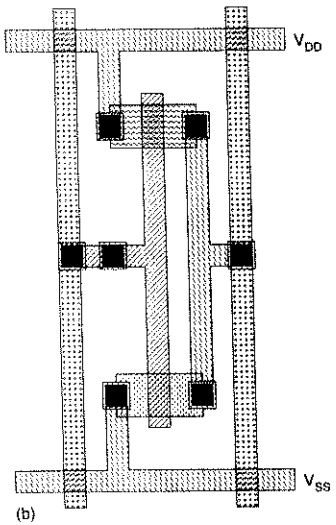

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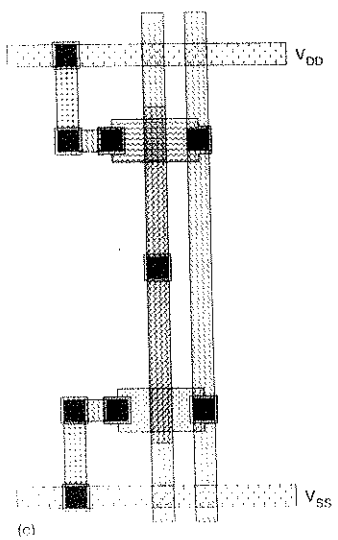

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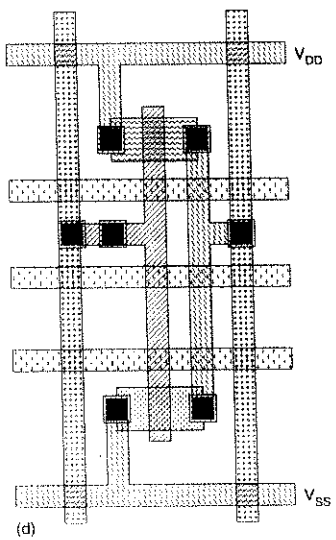

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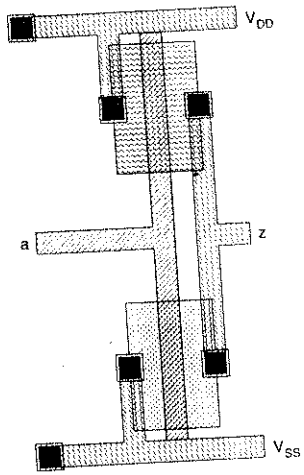

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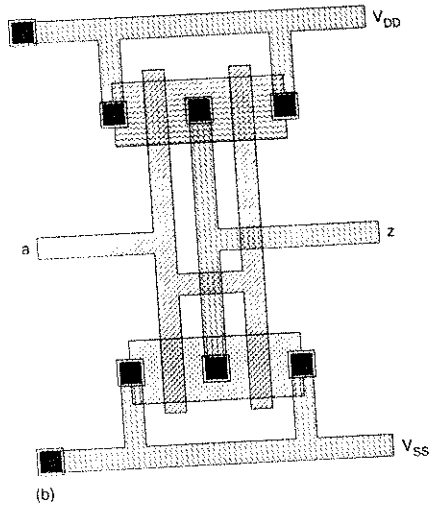

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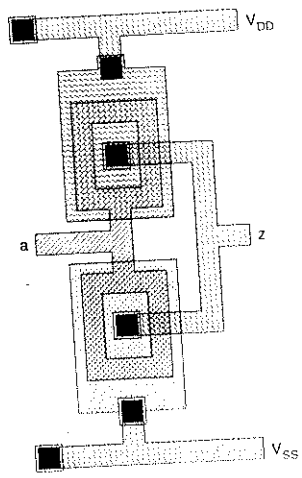

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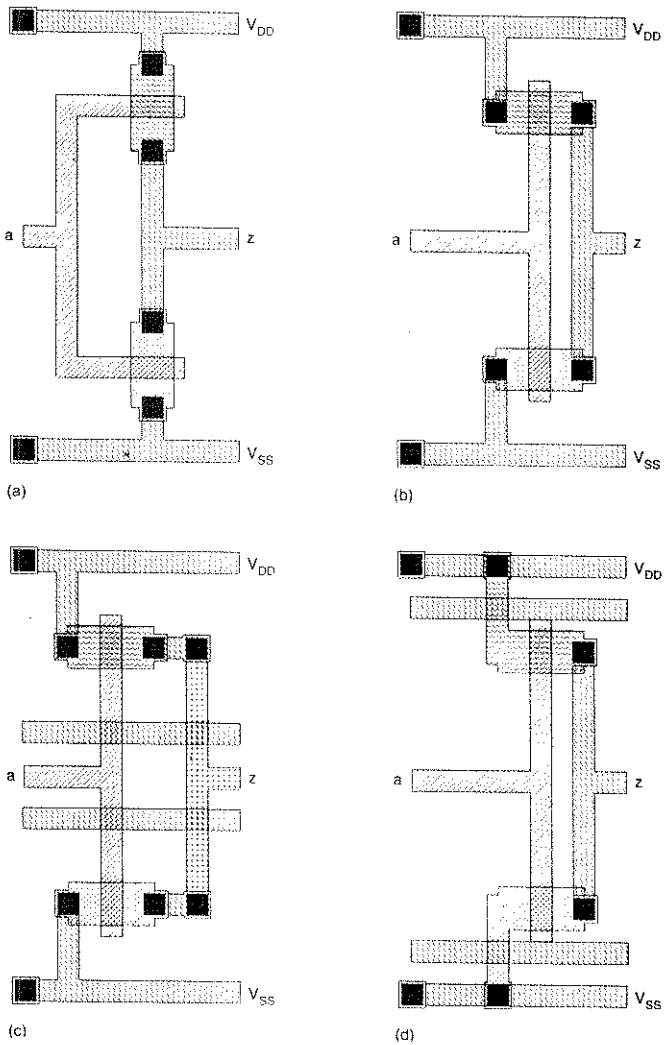


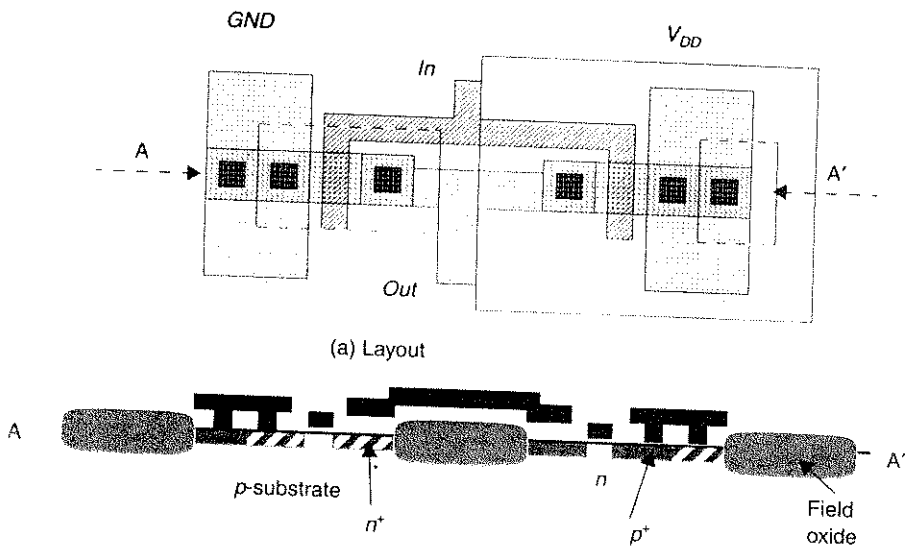


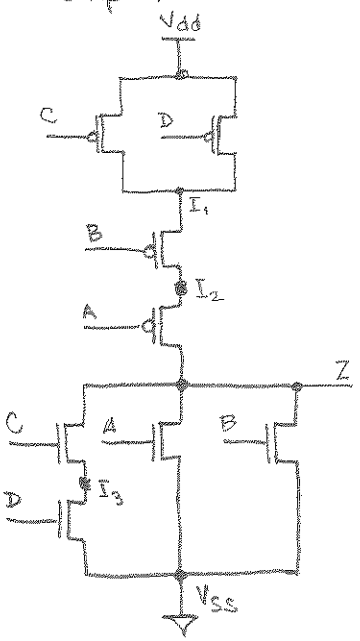
Figure A.6 A detailed layout example, including vertical process cross section and circuit diagram.

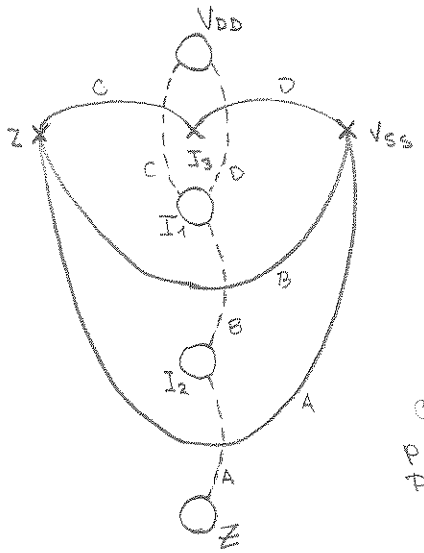
- Layout of complex gates
  - Layout technique "line of diffusion" can be applied to any complementary gate.
  - Can be automatized for static CMOS design.

Procedure

1) Convert the CMOS circuit to a graph
   - Vertices: Source/drain connections
   - Edges: Transistors connecting particular source/drain vertices.
   (Two graphs will be produced: one for each the n-tree and p-tree.

Example:





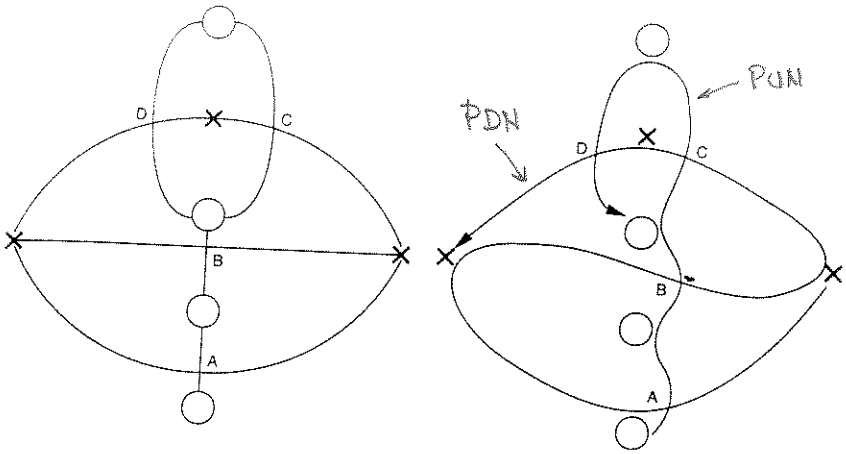
Two graphs are constructed: PUN = pull-up network and PDN = pull down net.

2) Identify equally sequenced Euler paths in PUN & PDN (ABCD-ABCD)
   - Euler path: A path traversing all nodes in a graph such that each edge is visited only once.

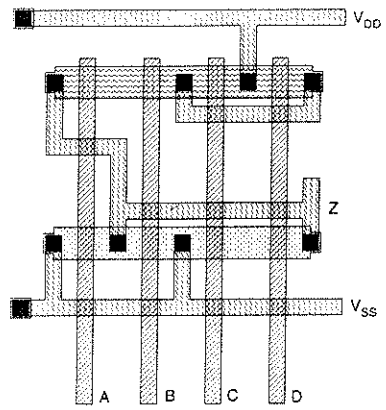
3) An ordering of the inputs leading to an uninterrupted diffusion strip implementation is given by the transistor sequence in the Euler paths in step2.

4) If the requested paths are not found, break the gate into smaller subgates in a minimum number of places.

Euler paths for PUN & PDN : ABCD



Symbolic Layout



NOTES:
- Solutions are not unique
- Dependence on arrangement of input variables
- Easily automatized

- Standard Cell layout : Introduces geometric regularity in the layout.

Typically fix the cell height and allow variable width

- Maximum height N- and P-transistors (W_n & W_p) separated D_{pn}
- V_{DD} and GND on top & bottom of cell respectively

W_p & W_n selected to account for cell properties like Power dissipation, delays, area & noise immunity

- Gate Array layout : Contain a number of predefined structures on the layout, while others are programmed

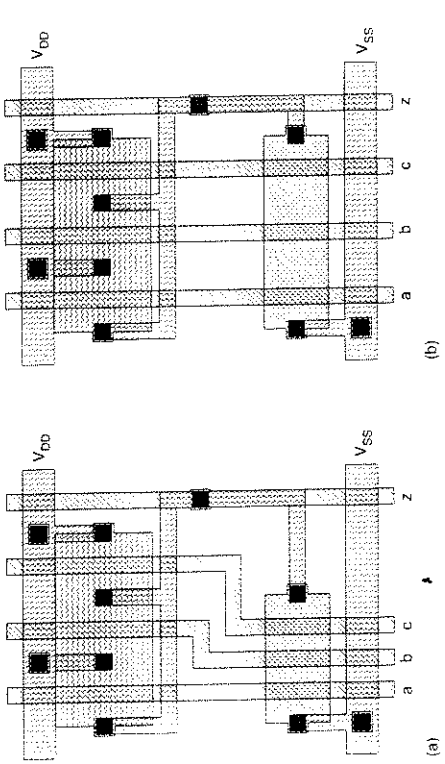
Predefined may include: - Well, diffussion, & poly

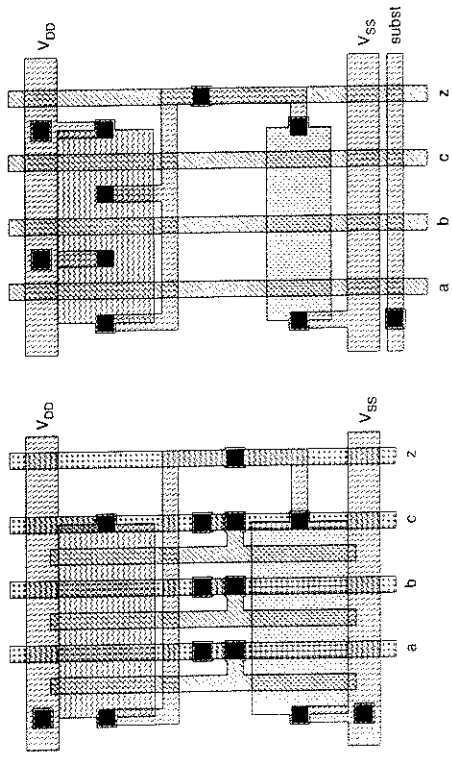
Programmable structures: - Contacts, vias, metal1, metal2

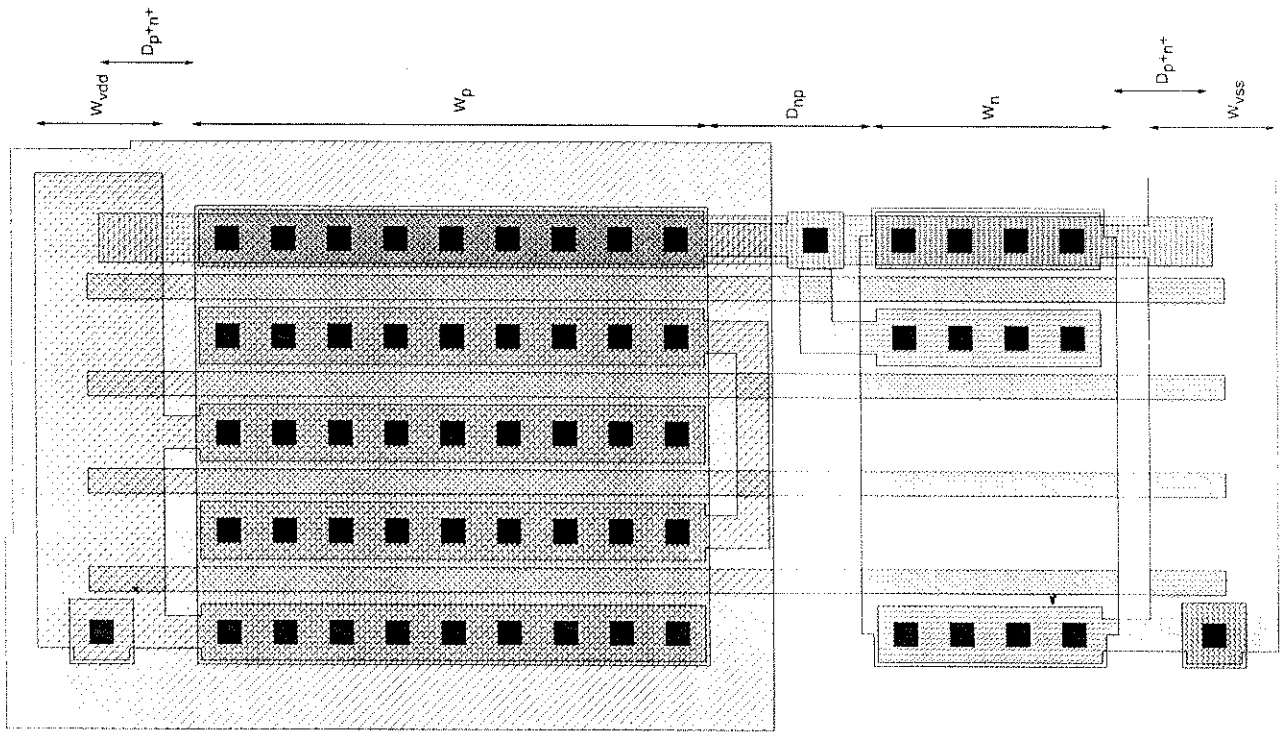
Gates are formed in "islands" with routing channels between them

- Sea-of-gates layout : Diffussion regions are extended accross the chip.

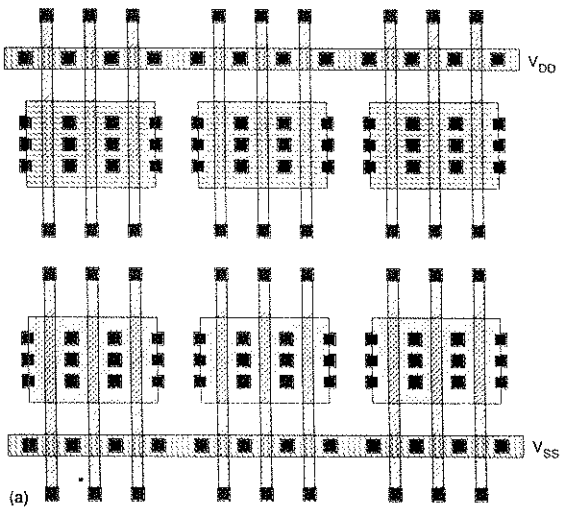
Gate issolation achieved by deactivating end transistors



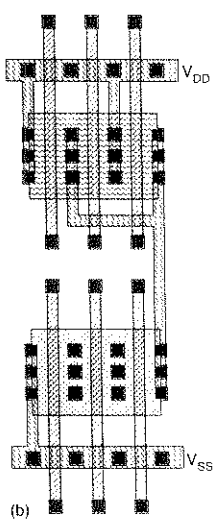




STANDARD-CELL LAYOUTS



UNPROGRAMMED



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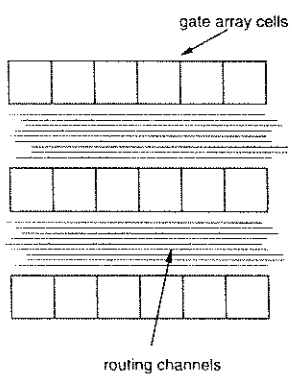
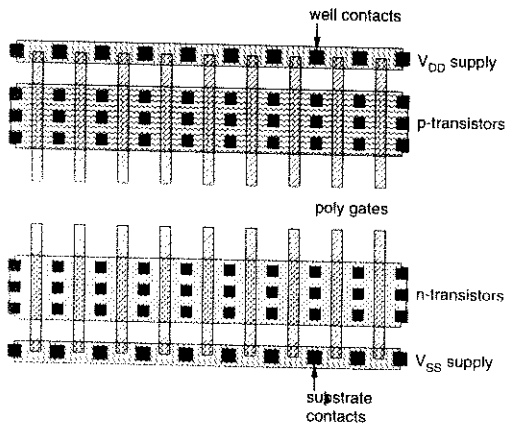
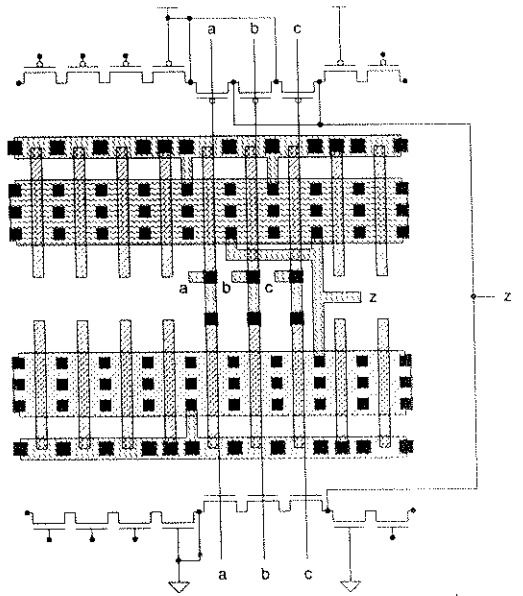


Routing of GA

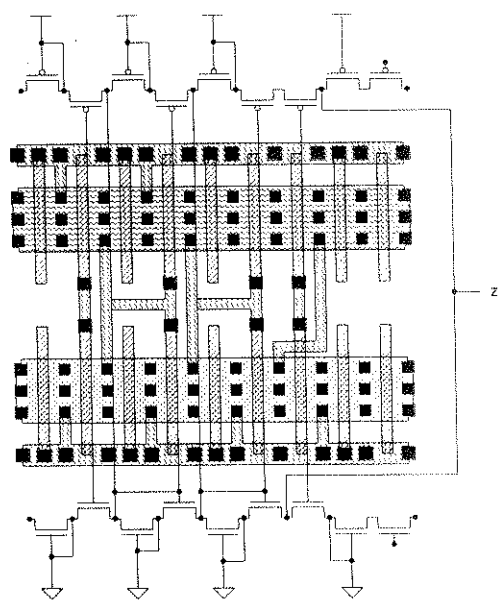
GATE ARRAYS



SEA-OF-GATES



3-input NAND



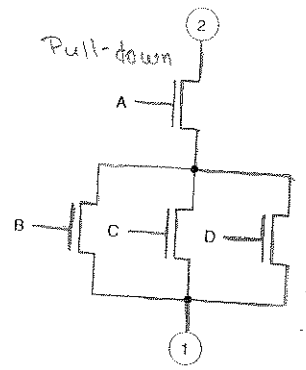
two-input NOR
driven by two inverters

ENGL-4219

CMOS gate layout guidelines

- During the electrical gate design:
  - Use NAND structures where possible, avoiding NOR structures. Critical in high-speed circuits, especially in large fan-in/fan-out situations
  - Use inverters at high fan-out nodes
  - Use minimum-sized gates on high fan-out nodes to minimize loading of driver.
  - Keep sharp rising & falling edges.
- Run V_{DD} & V_{SS} in metal at the top & bottom of the cell.
- Run vertical poly for each gate input. Order poly strips to allow maximal connection between transistors.
- Place N-devices close to Vss rail and P-devices close to Vdd.
- Poly, metal, or diffussion connections to complete gate design.
- Try to optimize blocks of transistors (10-100) rather than individual gates. (not possible when using std. cells).

Gate:



Example: OAI gate

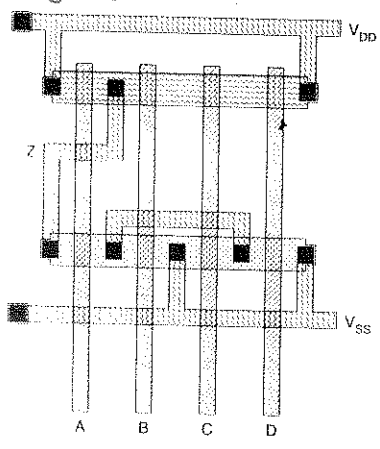
Pull down section could have either ① or ② connected to gnd rail.

a) Connecting ① to gnd, makes ② the output node: 1 transistor capacitance

b) Connecting ② to gnd makes ① the ouput node with at least 2 transistor capacitances.

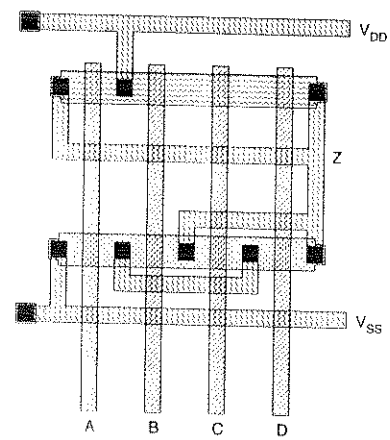
Thus a) is a better choice for speed.

Layouts:



Right

FASTER



Wrong

SLOWER