MOS Inverters

Digital Electronics - INEL 4207

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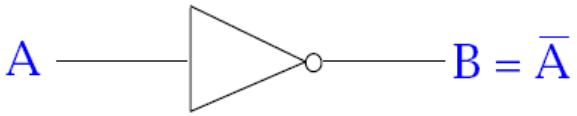
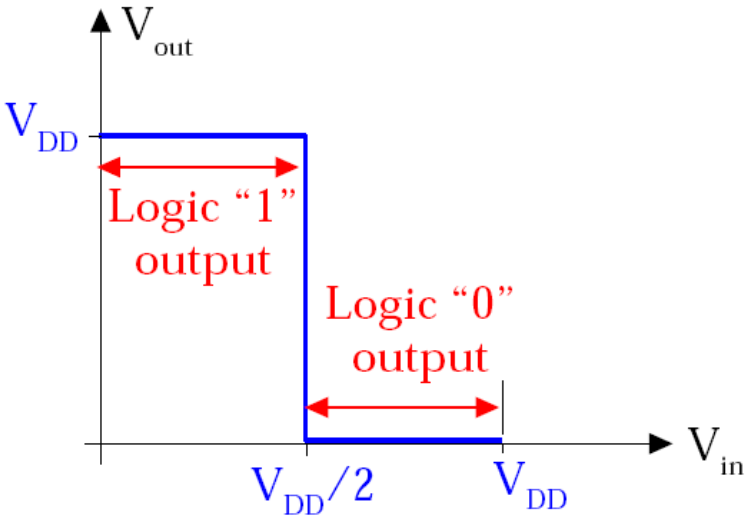
Objectives:

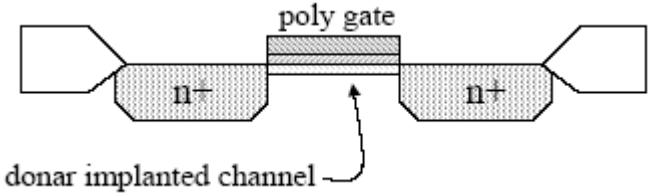
- Introduce MOS Inverter Styles
  - Resistor Load
  - Enhancement Load – Saturated / Linear
  - Depletion
  - Complementary (CMOS)
- Perform DC analysis of the circuits

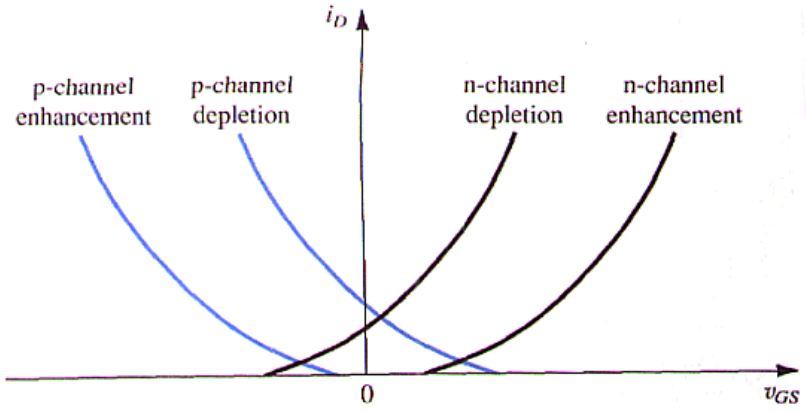
Ideal Inverter





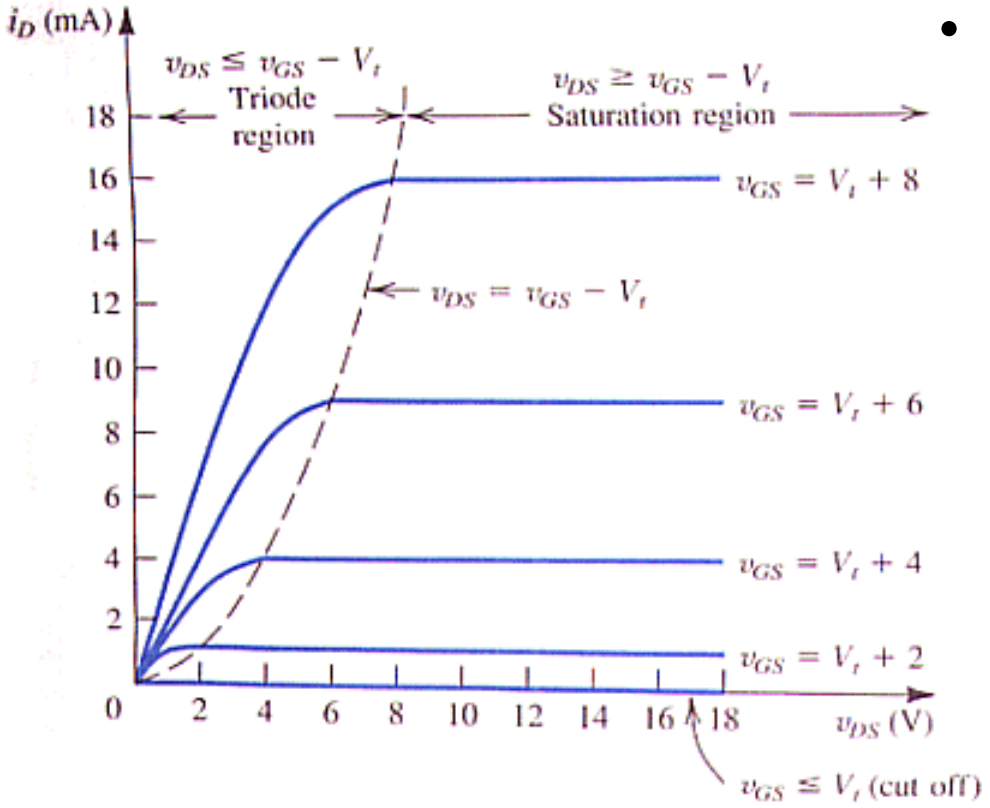
MOS Devices





- Operation regions (Enhancement)
  - $V_{GS}<V_T$:cutoff ,$V_{out}=V_{DD}$
  - $V_{GS}>V_T$,$V_{DS}>V_{GS}-V_T$: saturation
  - $V_{GS}>V_T$,$V_{DS}<V_{GS}-V_T$: linear

MOS Devices



- Operation regions
  - $V_{GS}<V_T$:cutoff , $V_{out}=V_{DD}$

$$I_D \approx 0$$

  - $V_{GS}>V_T$, $V_{DS}<(V_{GS}-V_T)$: linear

$$I_D = \frac{k}{2}\left[2(V_{GS}-V_T)V_{DS} - {V_{DS}}^2\right]$$

  - $V_{GS}>V_T$, $V_{DS}>(V_{GS}-V_T)$: saturation

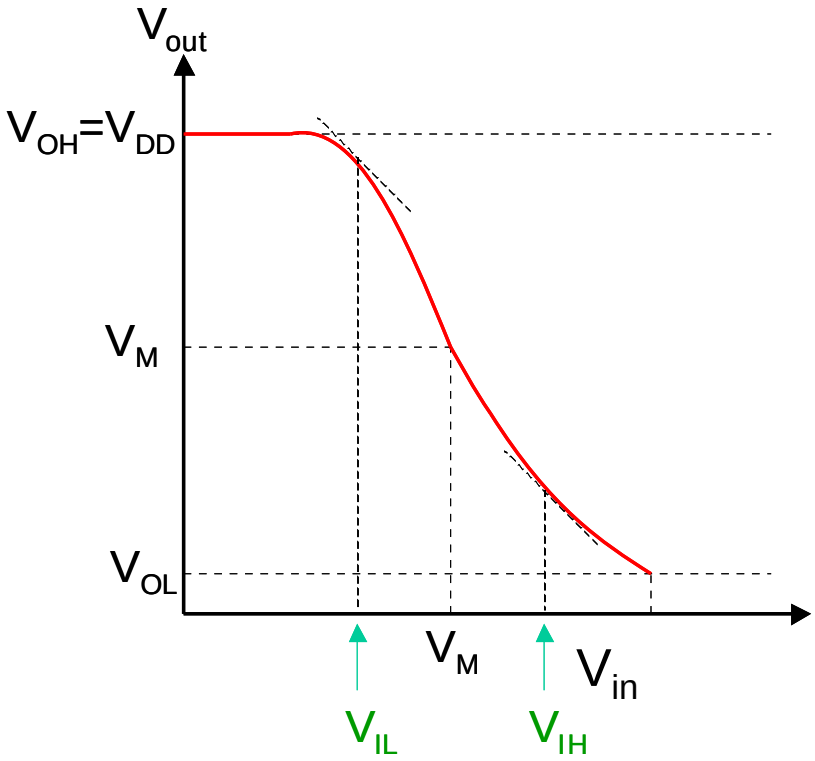
$$I_D = \frac{k}{2}(V_{GS}-V_T)^2$$

$$I_D = \frac{k}{2}(V_{GS}-V_T)^2(1+\lambda V_{DS})$$

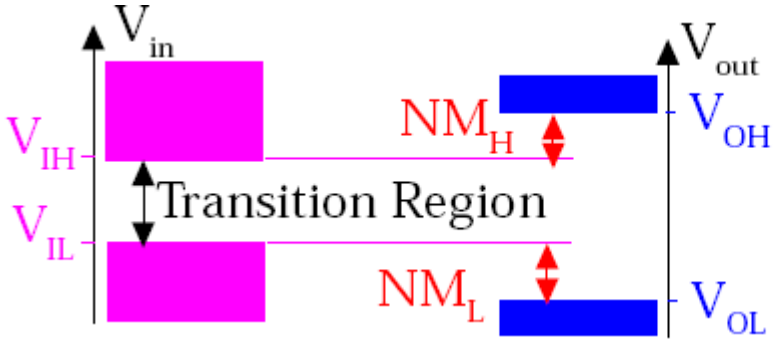
K=device transconductance

λ = channel-length modulation

Static Parameters



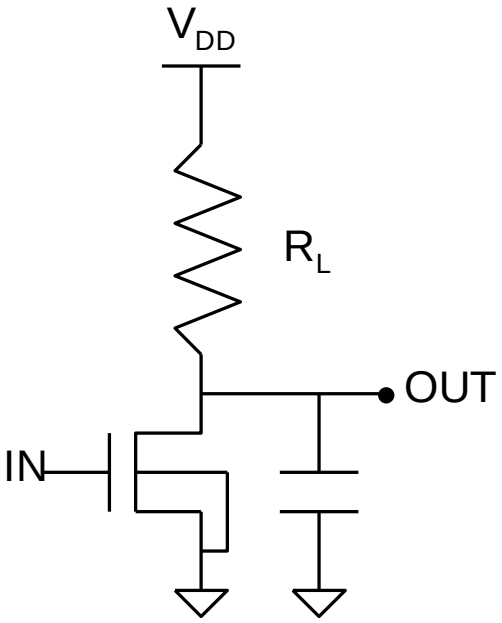
- VOH = max output voltage when output is “1”
- VOL = min output voltage when output is “0”
- VIL = max input voltage which can be interpreted as “0”
- VIH = min input voltage which can be interpreted as “1”

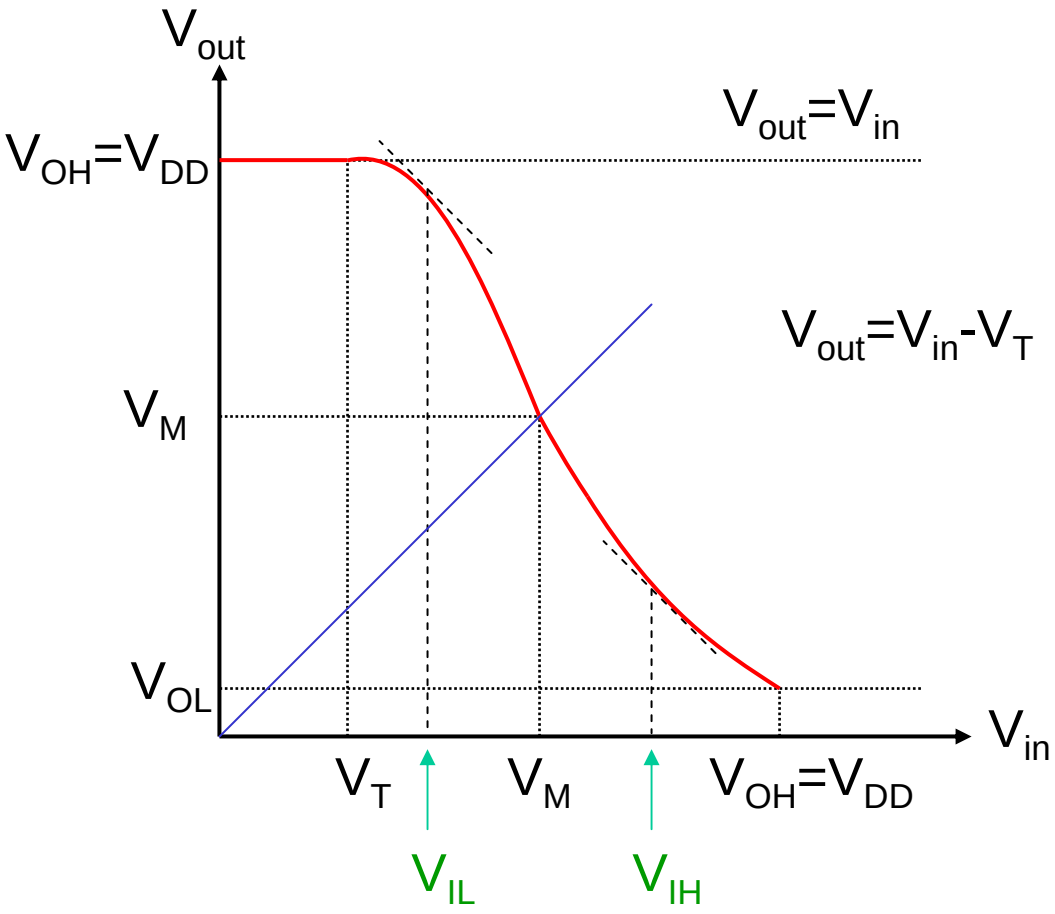


$NM_H = V_{OH} - V_{IH}$

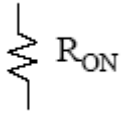
$NM_L = V_{IL} - V_{OL}$

MOS Inverter - Resistor Load





$|V_{GS}| < V_T$ device is open circuit 

$|V_{GS}| > V_T$ device conducts with resistance R_{ON} 

MOS Inverter - Resistor Load : Parameters

V_{OH}

$$V_{OH} = V_{DD}$$

V_{OL}

Assumption: Must verify latter

$$I_{D(lin)} = I_R$$

$$k\left[\left(V_{DD} - V_T\right)V_{OL} - \frac{V_{OL}^2}{2}\right] = \frac{V_{DD} - V_{OL}}{R_L}$$

$$\Rightarrow V_{OL} \cong \frac{V_{DD}}{1 + kR_L\left(V_{DD} - V_T\right)}$$

MOS Inverter - Resistor Load : Parameters - V_{IL}

$$\frac{k}{2}\left(V_{GS}-V_T\right)^2=\frac{V_{DD}-V_{out}}{R_L}$$

$$\frac{dV_{out}}{dV_{in}}=-1$$

$$\frac{dV_{out}}{dV_{in}}=-\frac{dI_D}{dV_{in}}\frac{dV_{out}}{dI_D}=-1$$

$$\frac{dI_D}{dV_{in}}=\frac{d}{dV_{in}}\frac{k}{2}\left(V_{in}-V_T\right)^2=k\left(V_{in}-V_T\right)$$

$$\frac{dV_{out}}{dI_D}=\left(\frac{dI_D}{dV_{out}}\right)^{-1}=\left(\frac{d}{dV_{out}}\left(\frac{V_{DD}-V_{out}}{R_L}\right)\right)^{-1}=-R_L$$

$$\frac{dV_{out}}{dV_{in}}=-\frac{dI_D}{dV_{in}}\frac{dV_{out}}{dI_D}=-k\left(V_{in}-V_T\right)R_L=-1$$

$$V_{IL}=V_T+\frac{1}{kR_L}$$

MOS Inverter - Resistor Load : Parameters - V_{IH}

$$\frac{k}{2}\left[2\left(V_{IH}-V_T\right)V_{out}-V_{out}^{\ 2}\right]=\frac{V_{DD}-V_{out}}{R_L} \qquad (1)$$

$$\frac{dV_{out}}{dV_{in}}=-\frac{dI_D}{dV_{in}}\frac{dV_{out}}{dI_D}=-1.0$$

$$\frac{dV_{out}}{dV_{in}}=-\frac{dI_D}{dV_{GS}}\frac{dV_{DS}}{dI_D}=-\frac{kV_{DS}}{k\left[V_{GS}-V_T-V_{DS}\right]}=-1.0$$

$$V_{out}=\frac{\left(V_{in}-V_T\right)}{2}$$

…substitute in (1)

$$k\left[\left(V_{IH}-V_T\right)\left(\frac{V_{IH}-V_T}{2}\right)-\frac{1}{2}\left(\frac{V_{IH}-V_T}{2}\right)^2\right]=\frac{V_{DD}}{R_L}-\frac{V_{IH}-V_T}{2R_L}$$

…solve quadratic expression by V_{IH}

MOS Inverter - Resistor Load : Parameters - V_M

V_M

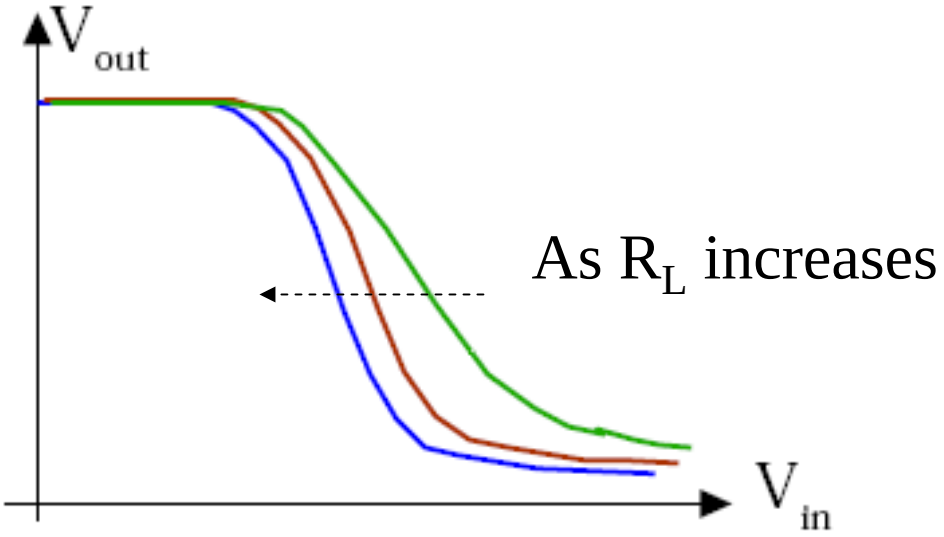
$$I_{DS} = \frac{k}{2}\left(V_{GS} - V_T\right)^2 = I_R = \frac{V_{DD} - V_{DS}}{R}$$

$$\frac{k}{2}\left(V_M - V_T\right)^2 = \frac{V_{DD} - V_M}{R}$$

$$V_M{}^2 - 2V_M\left(V_T - \frac{1}{kR_L}\right) + \left(V_T{}^2 - \frac{2V_{DD}}{kR_L}\right) = 0$$

$$\Rightarrow V_M = V_T + \frac{\sqrt{1 + 2kR_L\left(V_{DD} - V_T\right)} - 1}{kR_L} \cong V_T + \sqrt{\frac{2\left(V_{DD} - V_T\right)}{kR_L}}$$

Effect of R_L on VTC



But putting a larger resistance would also mean:

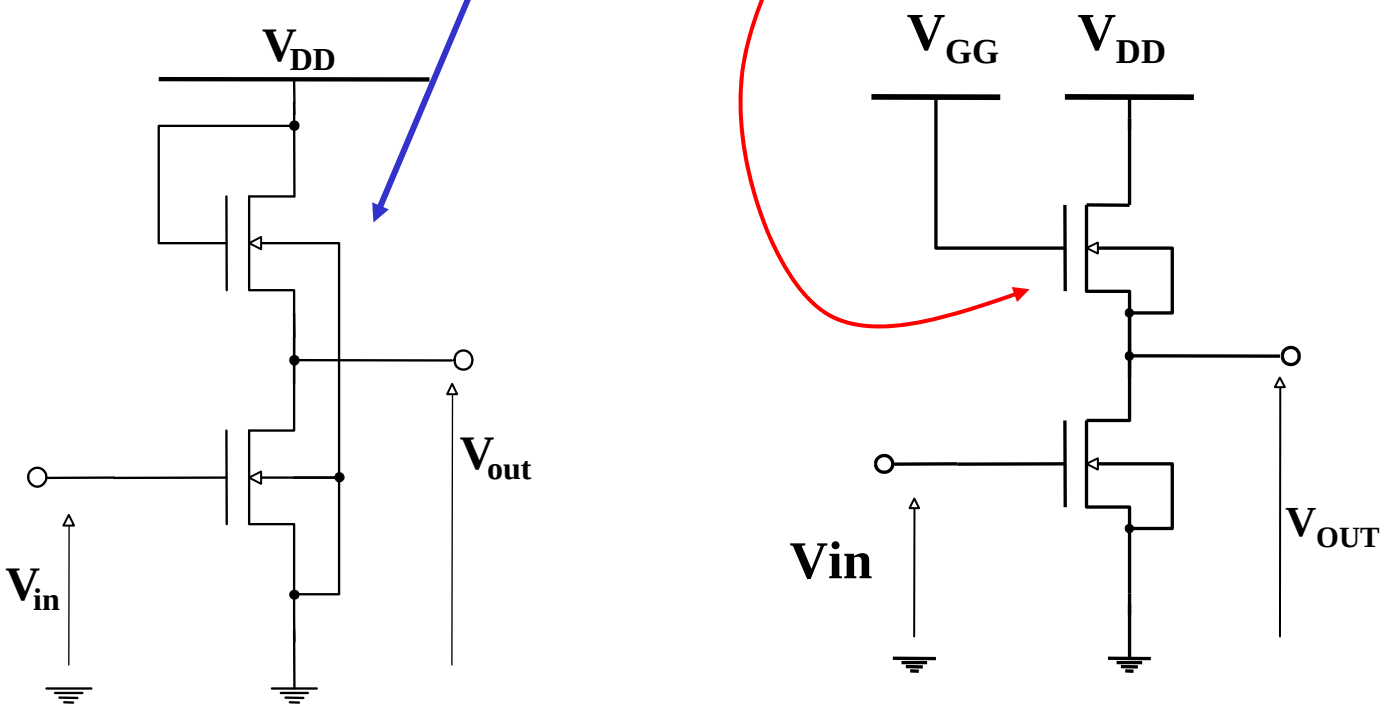
- larger resistor length
- greater switching delays

main disadvantage of resistor load:

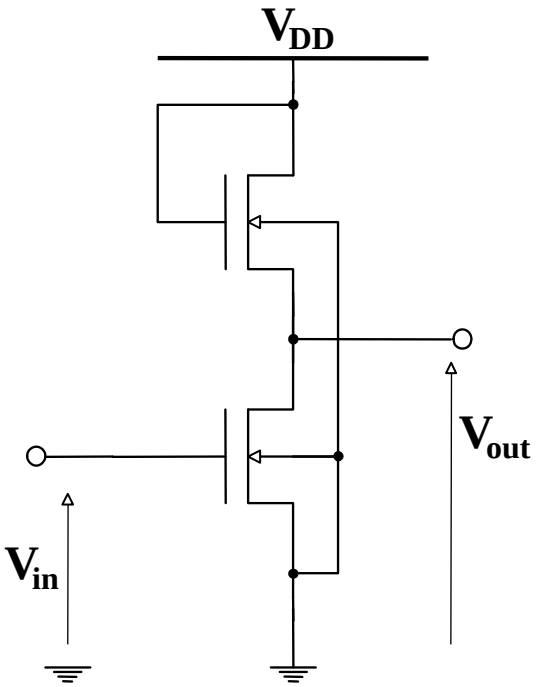
- occupies to much chip area (10s or 100s times the area of a single transistor!)

Using enhancement transistors as load devices

- Justification: Since VLSI resistors occupy to much chip space → use transistor in either saturation or linear region instead of resistor



Saturated enhancement load

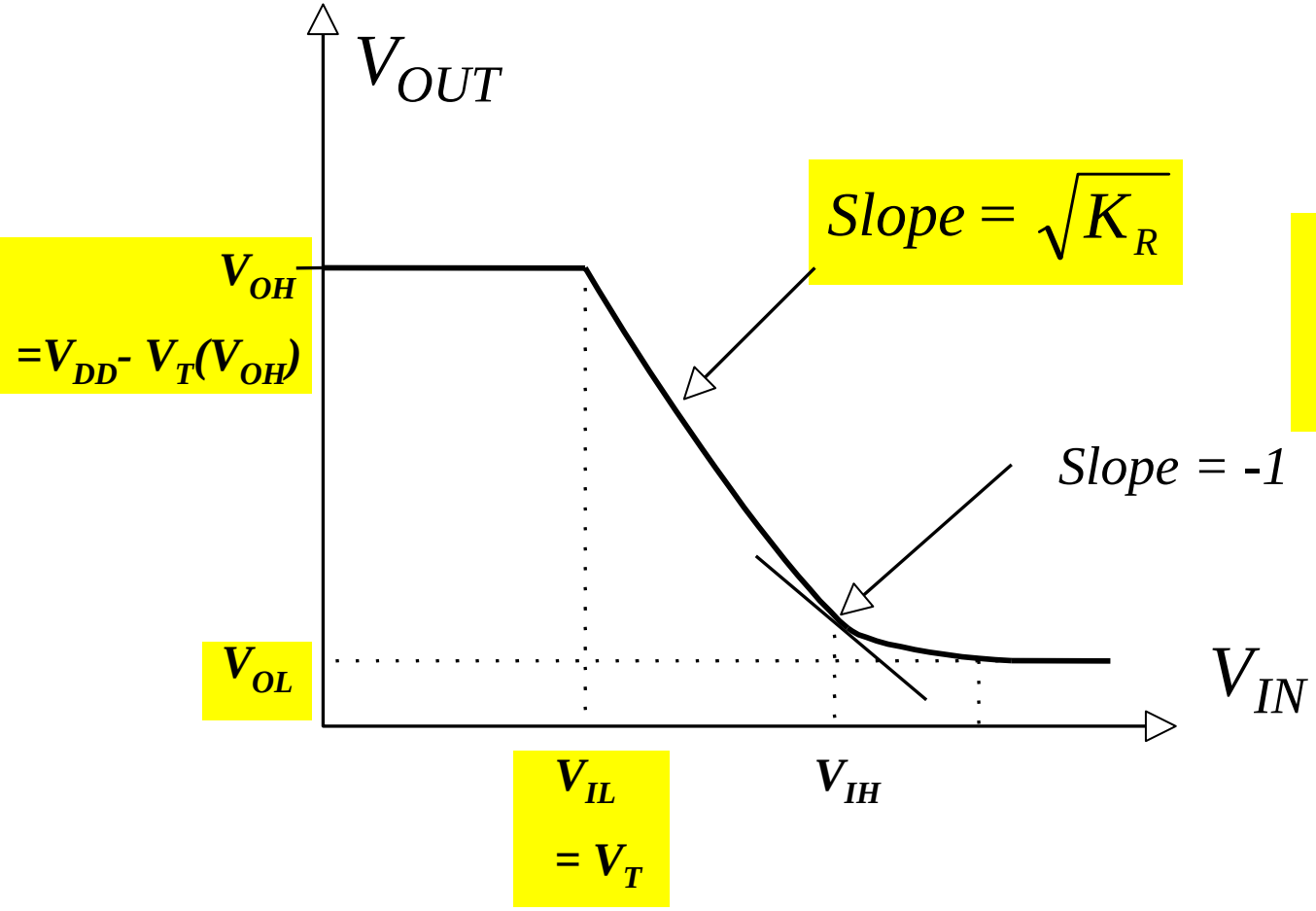


- Enhancement NMOS with $V_{GS} = V_{DS}$

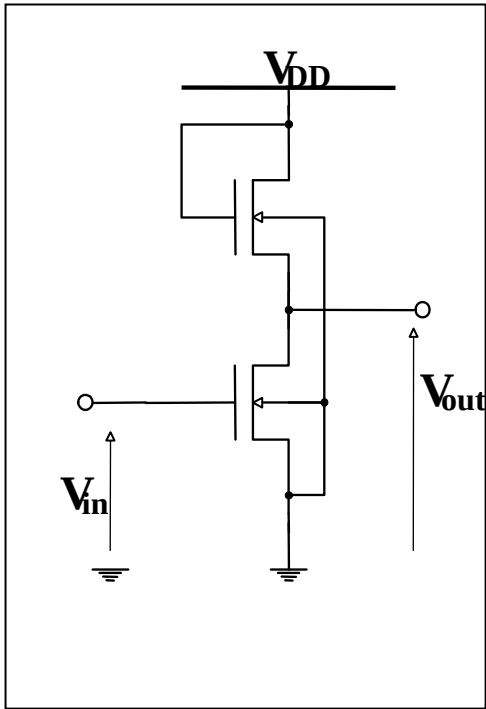
  → while $V_{OUT} < V_{DD} - V_T$
  the transistor will be in saturation
  because $V_{GS} > V_T$ & $V_{DS} > V_{GS}-V_T$

  → If V_{OUT} tries to go above $V_{DD}-V_T$,
  transistor goes cutoff
  (because $V_{GS} < V_T$)

Saturated enhancement load - VTC

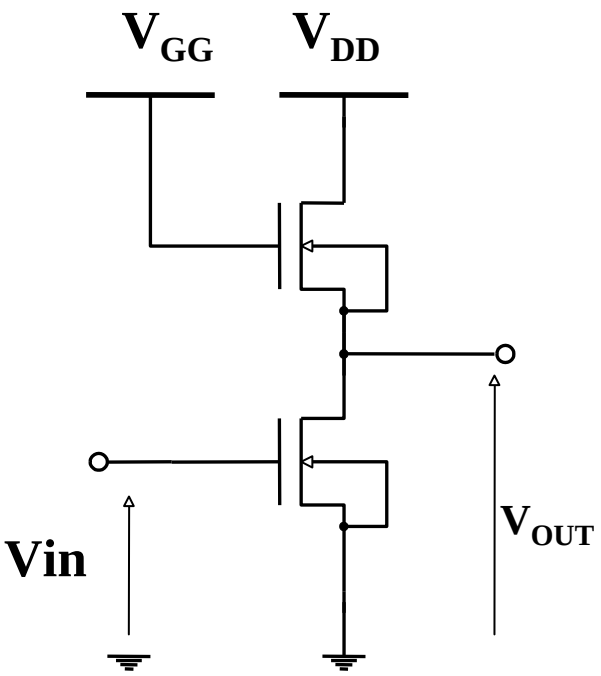


$$K_R = \frac{(W/L)_{inverter}}{(W/L)_{load}}$$



$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

Linear enhancement load

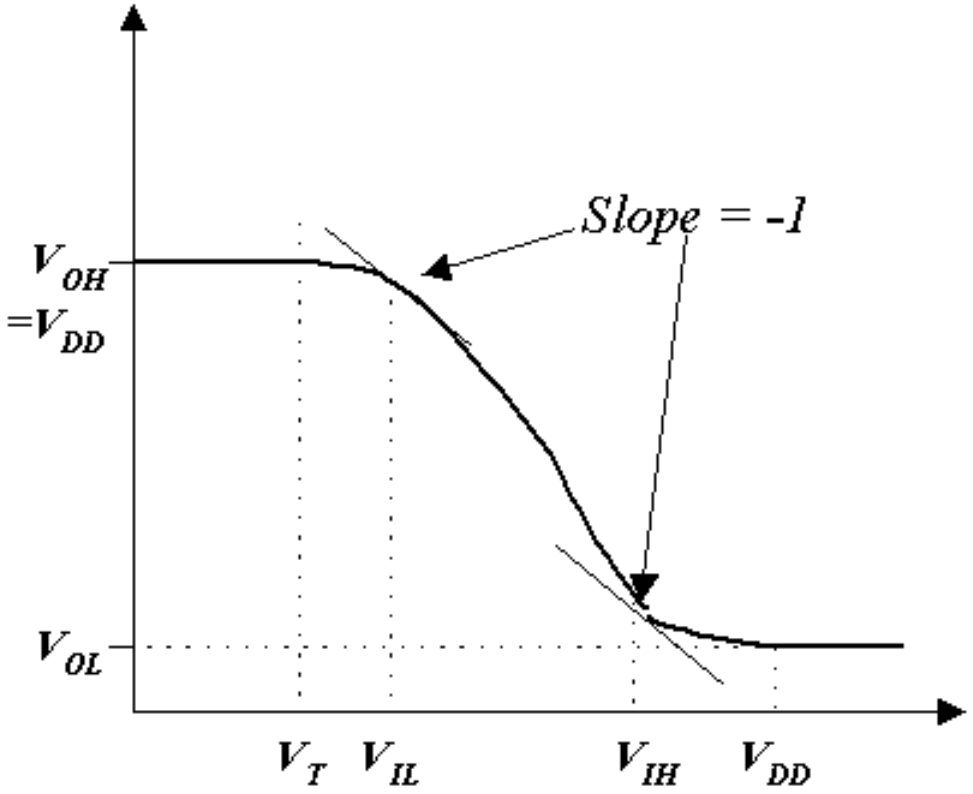


- Enhancement NMOS with $V_{GG} > V_{DD}+V_T$

→ since $V_{DS} = V_{DD}-V_{OUT}$
and $V_{GS} = V_{GG}-V_{OUT} > V_{DD}+V_T - V_{OUT}$
→ **$V_{DS} < V_{GS} - V_T$**

since $V_{GS} > V_T$:
the load is always on linear region

Linear enhancement load - VTC



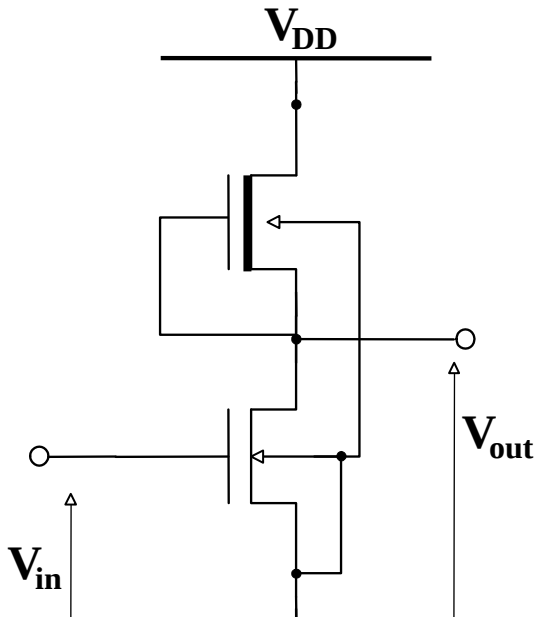
Pro:

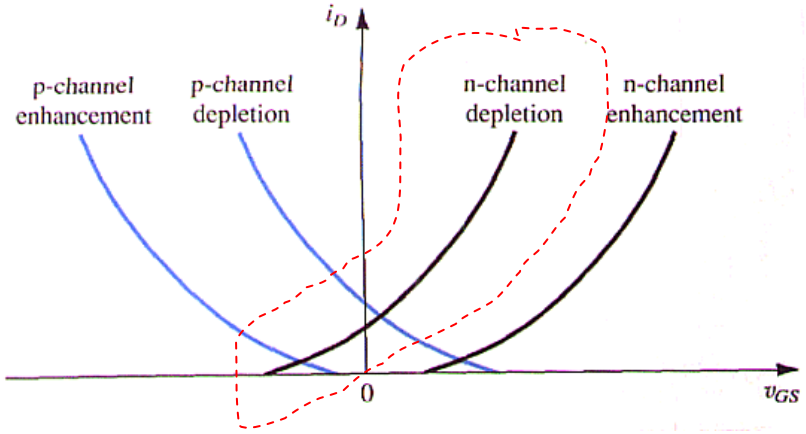
- $V_{OH} = V_{DD}$

Disadvantage:

- Additional voltage source
- K_R must be even larger than for saturated load for decent slope

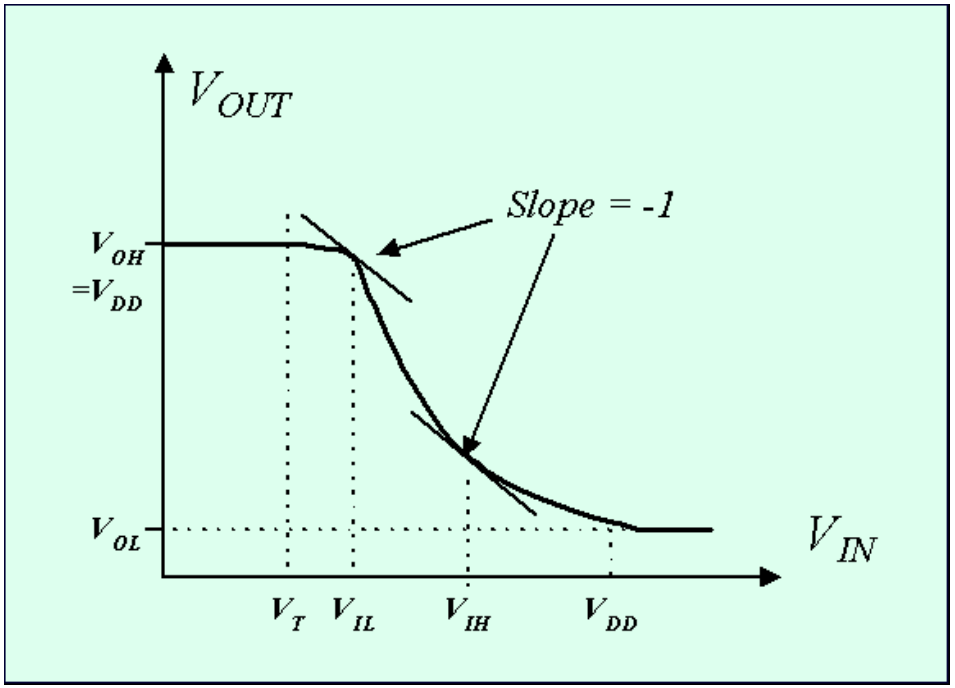
Depletion load





- Depletion NMOS with $V_{GS} = 0$

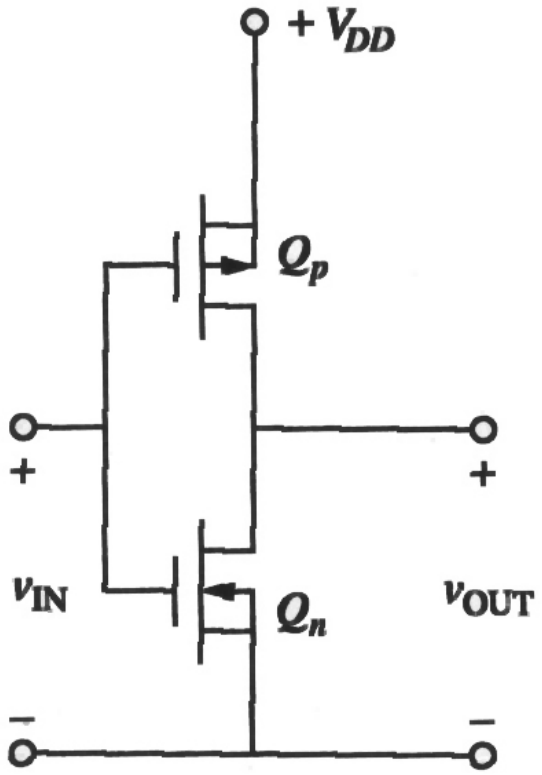
→ $V_{GS} > V_T$: always conducting



Good: $V_{OH} = V_{DD}$
no additional V source

Bad: addit. fab. process steps

Complementary MOSFET inverter



Features:

• Complementary MOS (CMOS) Inverter analysis makes use of both NMOS and PMOS transistors in the same logic gate.

+ All static parameters of CMOS inverters are superior to those of NMOS inverters

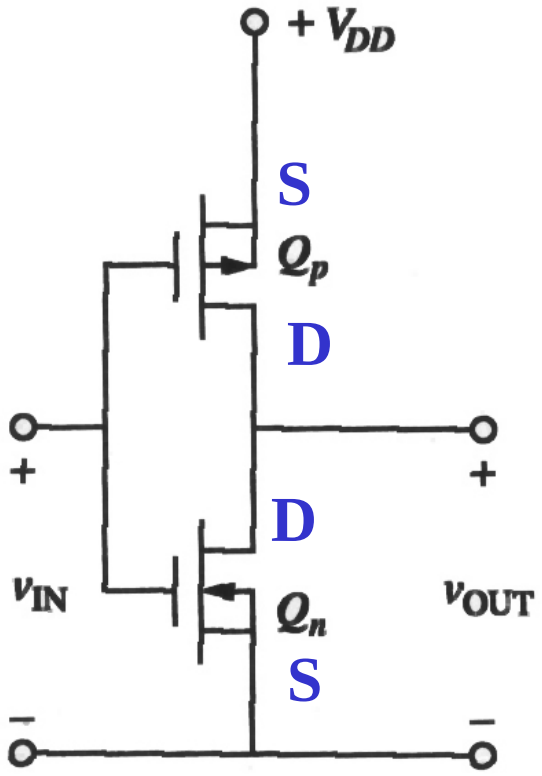
+ CMOS is the most widely used digital circuit technology in comparison to other logic families.

· lowest power dissipation

· highest packing density

-Increased process complexity (to provide isolated transistors of both polarity types)

Complementary MOSFET (CMOS) inverter



Intuitively:

$\underline{V_{IN} \approx 0}$

NMOS open ckt. ($V_{GSn} < V_{Tn}$)

PMOS conducting ($V_{GSp} > V_{Tp}$)

→ $V_{OUT} = V_{DD}$

$V_{OH} = V_{DD}$ (Good!)

$\underline{V_{IN} \approx V_{DD}}$

NMOS conducting

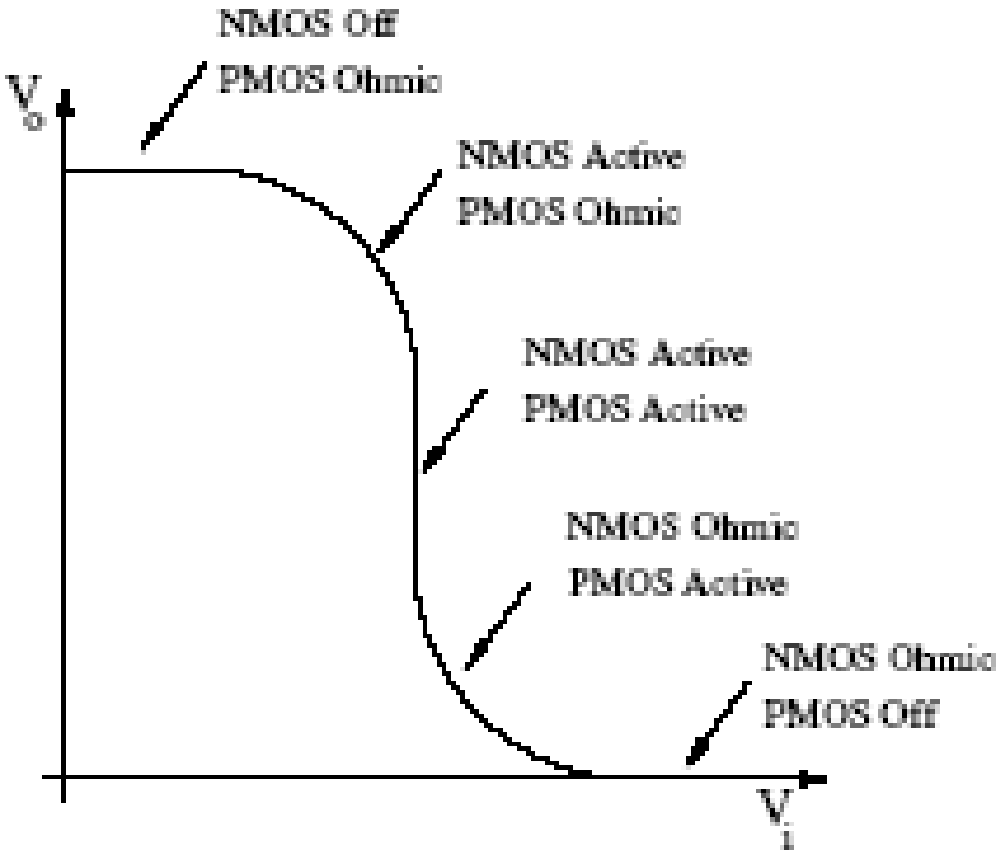
PMOS open ckt.

→ $V_{OUT} = 0$

$V_{OL} = 0$ (Great!)

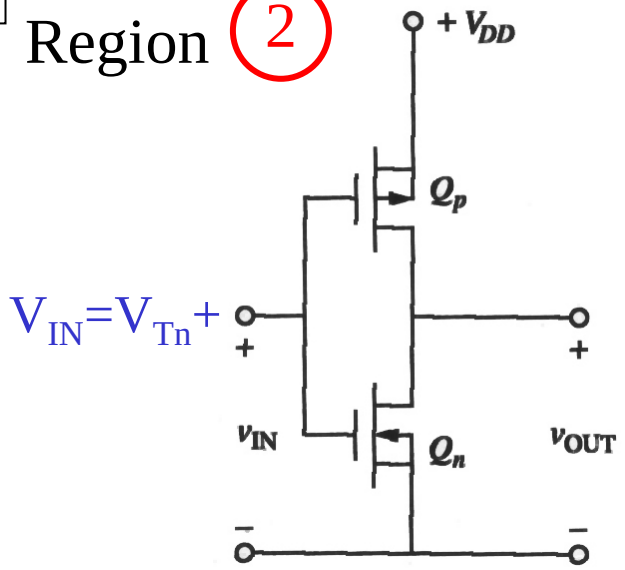
CMOS inverter - VTC

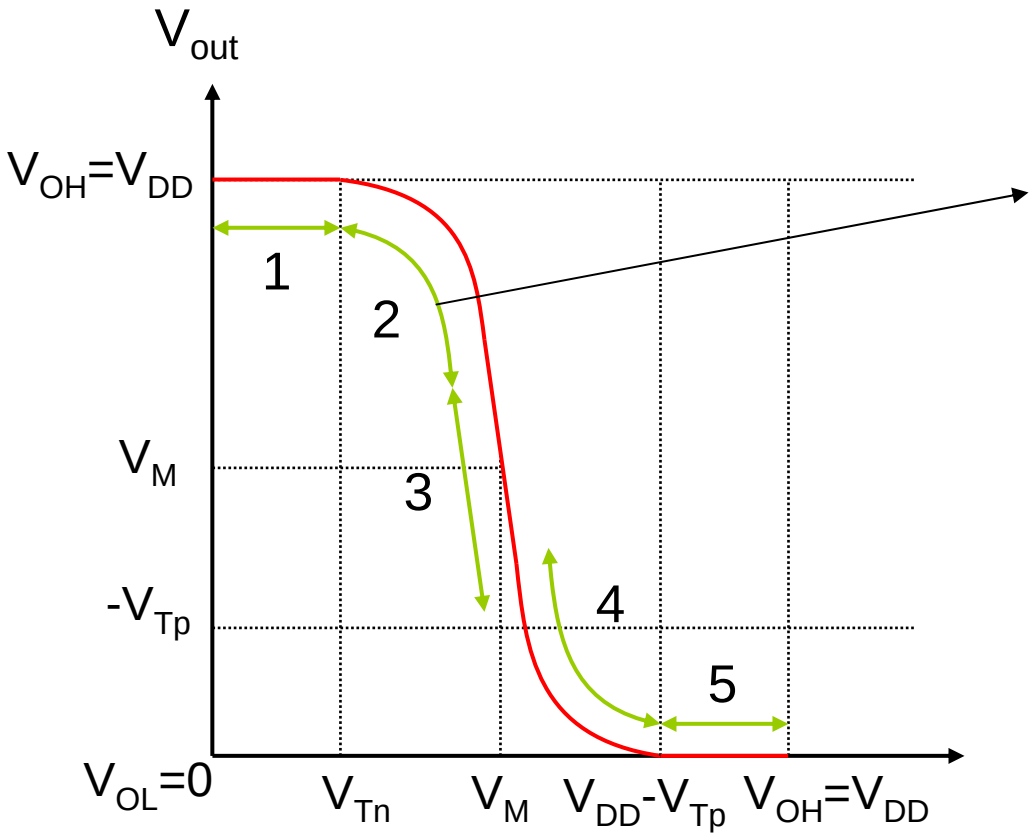
1. PMOS linear, NMOS off
2. PMOS linear, NMOS sat
3. PMOS, NMOS both sat
4. PMOS sat, NMOS linear
5. PMOS off, NMOS linear



CMOS inverter – Region 2

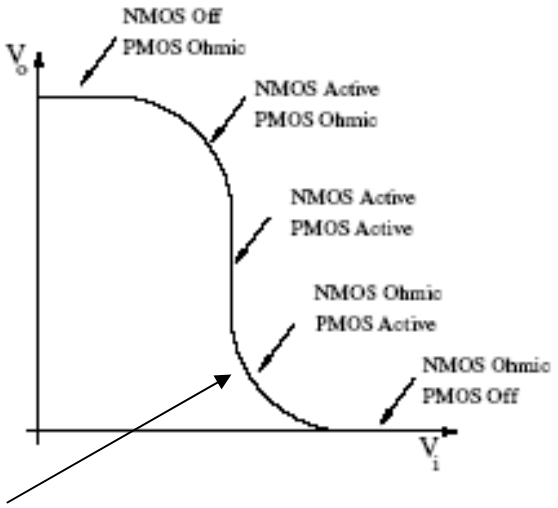
Region 2





PMOS linear, NMOS saturation

CMOS inverter – Param. Calculation Example



NMOS linear, PMOS saturation

Calculate V_{IH}

$$I_{Dn} = \frac{k_n}{2}\left[2(V_{IH} - V_{Tn})V_{OUT} - V_{OUT}^{\ 2}\right] \quad (1)$$

$$I_{Dp} = \frac{k_p}{2}(|V_{GSp}| - |V_{Tp}|)^2$$

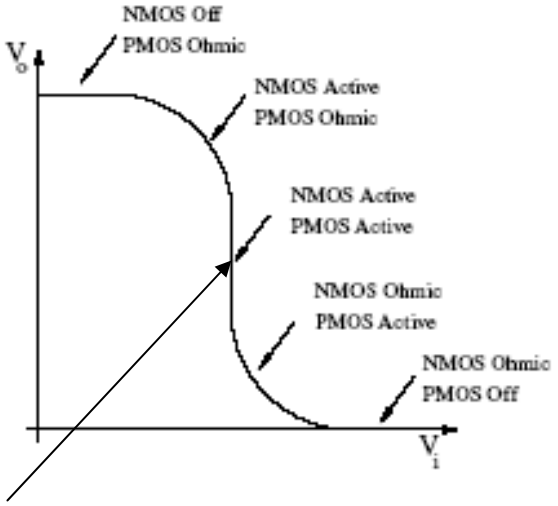
$$\frac{dV_{out}}{dV_{in}} = -\frac{dI_{Dp} - dI_{Dn}}{dV_{in}}\frac{dV_{out}}{dI_{Dp} - dI_{Dn}} = -1$$

$$\frac{dV_{out}}{dV_{in}} = -\frac{k_n V_{OUT} + k_p(V_{DD} - V_{IH} - V_{Tp})}{k_n(V_{IH} - V_{OUT} - V_{Tn})} = -1$$

$$V_{IH} = \frac{2V_{OUT} + V_{Tn} + (k_p / k_n)(V_{DD} - |V_{TP}|)}{1 + (k_p / k_n)}$$

Substitute in (1), then solve for V_{OUT}, finally obtain V_{IH}

CMOS inverter – Param. Calculation Example



NMOS & PMOS saturation

Calculate V_M

$$I_{Dn} = \frac{k_n}{2}(|V_{GSn}| - |V_{Tn}|)^2$$

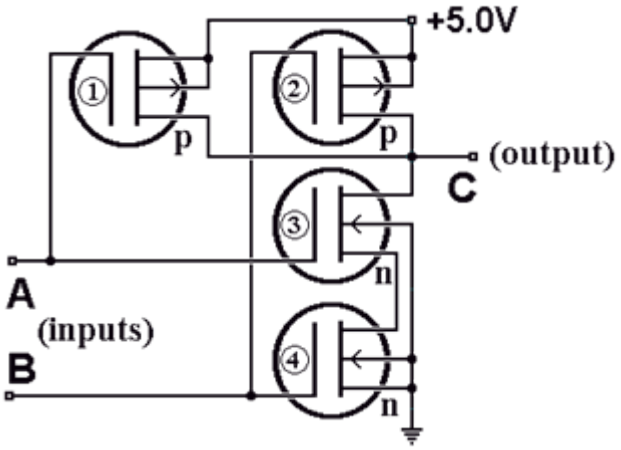
$$I_{Dp} = \frac{k_p}{2}(|V_{GSp}| - |V_{Tp}|)^2$$

$$\frac{k_n}{2}(|V_M| - |V_{Tn}|)^2 = \frac{k_p}{2}(V_{DD} - V_M - |V_{Tp}|)^2$$

.. Solve for V_M

Summary

• CMOS inverter – most used, smallest, lowest power dissipation, best inverter characteristics.
…base for more complex logic gates



• Calculation of static parameters: V_{IH}, V_{IL}, V_{OH}, V_{OL}, V_M.
  - •Important: Deduce the region of operation of the transistors (verify later)
  - • V_{IH}, V_{IL} ← slope = -1, use chain rule to simplify calculations
  - • VTC affected by R, K_R

Recordatorio

- Buscar copias de Dr. Jimenez en Reproducciones ($1-$2) – “Digital circuits using MOS transisitors”