Characteristics of Digital ICs
CHARACTERISTICS OF DIGITAL ICs

Quality Metrics in IC Design

1. Cost
   - Resource investment to produce a batch of ICs
2. Functionality
   - IC ability to perform the function it was designed for
3. Performance
   - Circuit speed: delay, operating frequency, and processing capability
4. Robustness
   - Ability to withstand process variations and noise disturbances
5. Power and Energy Consumption
   - Energy consumed for IC operation and heat dissipation
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Cost of an Integrated Circuit

• Non-recurrent Engineering (NRE) Costs (Fixed)
  *One-time cost factors. Independent from production volume*
  - Design time and effort
  - Mask generation
  - Indirect costs: R&D, infrastructure, marketing, etc.

• Recurrent Costs (Variable)
  *Cost directly attributable to a manufactured product. Proportional to chip area and product volume*
  - Silicon processing
  - Die testing
  - IC packaging

Cost per IC = Recurrent Cost per IC + \( \frac{NRE\ Cost}{Volume} \)
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Fixed Costs

- Increase with:
  - Technology scale-down
  - Stringent design specifications
  - Chip complexity

- Decrease with:
  - Design automation level
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Variable Costs

<table>
<thead>
<tr>
<th>Wafer Manufacturing</th>
<th>Die Fabrication</th>
<th>Testing</th>
<th>Packaging</th>
</tr>
</thead>
</table>

Source: "http://www.amd.com"
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Variable Cost Computation

Fabrication capital cost per transistor (Moore’s law)

Variable cost = \frac{\text{Die cost} + \text{Testing cost} + \text{Packaging cost}}{\text{Test yield}}
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Die Cost and Yield

Dies per wafer = \( \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2} \times \text{die area}} \)

Yield = \( \frac{\text{No. of good chips per wafer}}{\text{Total number of dies per wafer}} \times 100\% \)

Die cost = \( \frac{\text{Wafer cost}}{\text{Dies per wafer} \times \text{Die yield}} \)
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Estimating Variable Costs

• Cost estimation during design phase
  – Based on process characterization information and design information

\[
\text{Die yield} = \left( 1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha} \right)^{-\alpha}
\]

\(\alpha\) is approximately 3

\[\text{die cost} = f(\text{die area})^4\]
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A Few Cost Examples

Based on production data back in 1994

<table>
<thead>
<tr>
<th>Chip</th>
<th>Metal layers</th>
<th>Line width</th>
<th>Wafer cost</th>
<th>Def./ cm²</th>
<th>Area mm²</th>
<th>Dies/wafer</th>
<th>Yield</th>
<th>Die cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>386DX</td>
<td>2</td>
<td>0.90</td>
<td>$900</td>
<td>1.0</td>
<td>43</td>
<td>360</td>
<td>71%</td>
<td>$4</td>
</tr>
<tr>
<td>486 DX2</td>
<td>3</td>
<td>0.80</td>
<td>$1200</td>
<td>1.0</td>
<td>81</td>
<td>181</td>
<td>54%</td>
<td>$12</td>
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<tr>
<td>Power PC 601</td>
<td>4</td>
<td>0.80</td>
<td>$1700</td>
<td>1.3</td>
<td>121</td>
<td>115</td>
<td>28%</td>
<td>$53</td>
</tr>
<tr>
<td>HP PA 7100</td>
<td>3</td>
<td>0.80</td>
<td>$1300</td>
<td>1.0</td>
<td>196</td>
<td>66</td>
<td>27%</td>
<td>$73</td>
</tr>
<tr>
<td>DEC Alpha</td>
<td>3</td>
<td>0.70</td>
<td>$1500</td>
<td>1.2</td>
<td>234</td>
<td>53</td>
<td>19%</td>
<td>$149</td>
</tr>
<tr>
<td>Super Sparc</td>
<td>3</td>
<td>0.70</td>
<td>$1700</td>
<td>1.6</td>
<td>256</td>
<td>48</td>
<td>13%</td>
<td>$272</td>
</tr>
<tr>
<td>Pentium</td>
<td>3</td>
<td>0.80</td>
<td>$1500</td>
<td>1.5</td>
<td>296</td>
<td>40</td>
<td>9%</td>
<td>$417</td>
</tr>
</tbody>
</table>
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Performance

• Computational speed of a digital circuit:
  – Microprocessor: MIPS
  – Digital Gate: Propagation Delay

  *Amount of time it takes an input stimulus to produce a change in the gate output*

  – Parameters:
    • \( t_{PHL} \) = Low-high propagation delay
    • \( t_{PHL} \) = High-low propagation delay
    • \( t_{PD} \) = Average propagation delay
    • \( t_r \) = Rise time
    • \( t_f \) = Fall time
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Delay Definitions

$$t_{PD} = \frac{1}{2} (t_{PLH} + t_{PHL})$$

![Diagram showing delay definitions](image)
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Ring Oscillator

\[ T = 2 \times t_{PD} \times N \]

\[ N \text{ odd} \]

\[ T \gg t_r + t_f \]
A First-Order RC Network

\[ v_{out}(t) = (1 - e^{-t/\tau}) V \]

\[ t_p = \ln(2) \tau = 0.69 \text{ RC} \]

Important model – matches delay of inverter
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Functionality and Robustness

• Sources of Noise in Digital Ics:
  – Crosstalk (Inductive and capacitive coupling)
  – Reflections and ringing
  – Power Supply Noise
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Robustness Parameters

• Voltage Transfer Characteristic
• Noise Immunity
• Regenerative Property
• Directivity
• Fan-in and Fan-out
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Voltage Transfer Transfer Characteristic

$$V(x)$$

$$V(y)$$

$$V_{OH}$$

$$V_{OL}$$

$$V_{OL} = f(V_{OH})$$

$$V_{OH} = f(V_{OL})$$

$$V_M = f(V_M)$$

$$V(y) = V(x)$$

Inverting VTC

VTC: $$v_{out} = f(v_{in})$$

Nominal Voltage Levels
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VTC Thresholds

- $V_{IH}$
- $V_{OH}$
- $V_{OL}$
- $V_{IL}$
- $V_{supply}$
- $V_{out}$

Transition Region

Slope = -1

V ground reference
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Noise Margins

Noise Margin High (NM_H)

Noise Margin Low (NM_L)

Logic Swing

Gate Input

Gate Output

Transition Region

\[ NM_L = V_{IL} - V_{OL} \]
\[ NM_H = V_{OH} - V_{IH} \]

Logic Swing = \[ V_{OH} - V_{OL} \]

Transition Region: From \( V_{IL} \) to \( V_{IH} \)
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Example: Inverting VTC

VOH = 3.5V
VOL = 0.45V
VM = 1.64V
VIH = 2.35V
VIL = 0.66V
MNL = 0.21V
NMH = 1.15V
LS = 3.05V

Transition region 0.66V to 2.35V