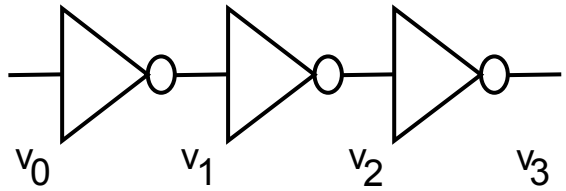
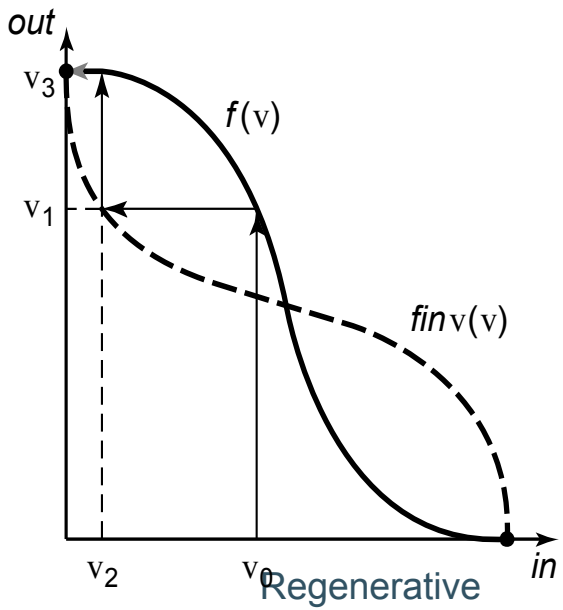
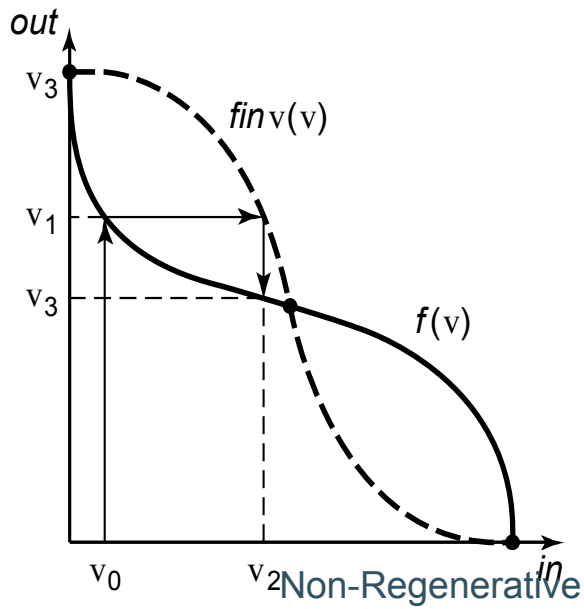
CHARACTERISTICS OF DIGITAL ICs

Regenerative Property



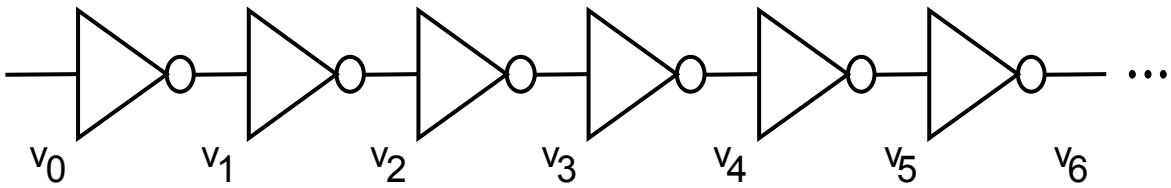


Regenerative

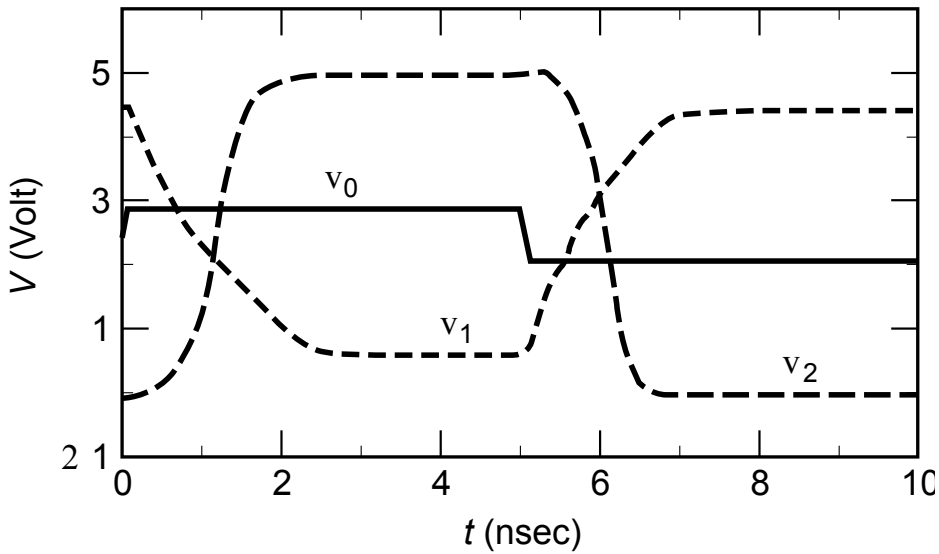


Non-Regenerative

Effect of Regenerative Property



A chain of inverters



Simulated response

CHARACTERISTICS OF DIGITAL ICs

Key Reliability Properties

- Absolute noise margin values are deceptive
  - A floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)
- Noise immunity is the most important metric
  - Defines the circuit capability to suppress noise sources
- Key metrics:
  - Noise transfer functions
  - Output impedance of the driver
  - Input impedance of the receiver

Noise Budget

- Allocates gross noise margin to expected sources of noise
- Differentiate between fixed (V_{Nf}) and proportional (V_{sw}) noise sources

$$V_{NM} = \frac{V_{sw}}{2} \geq \sum_i f_i V_{Nfi} + \sum_j g_j V_{sw}$$

- Sources: supply noise, cross talk, interference, offset

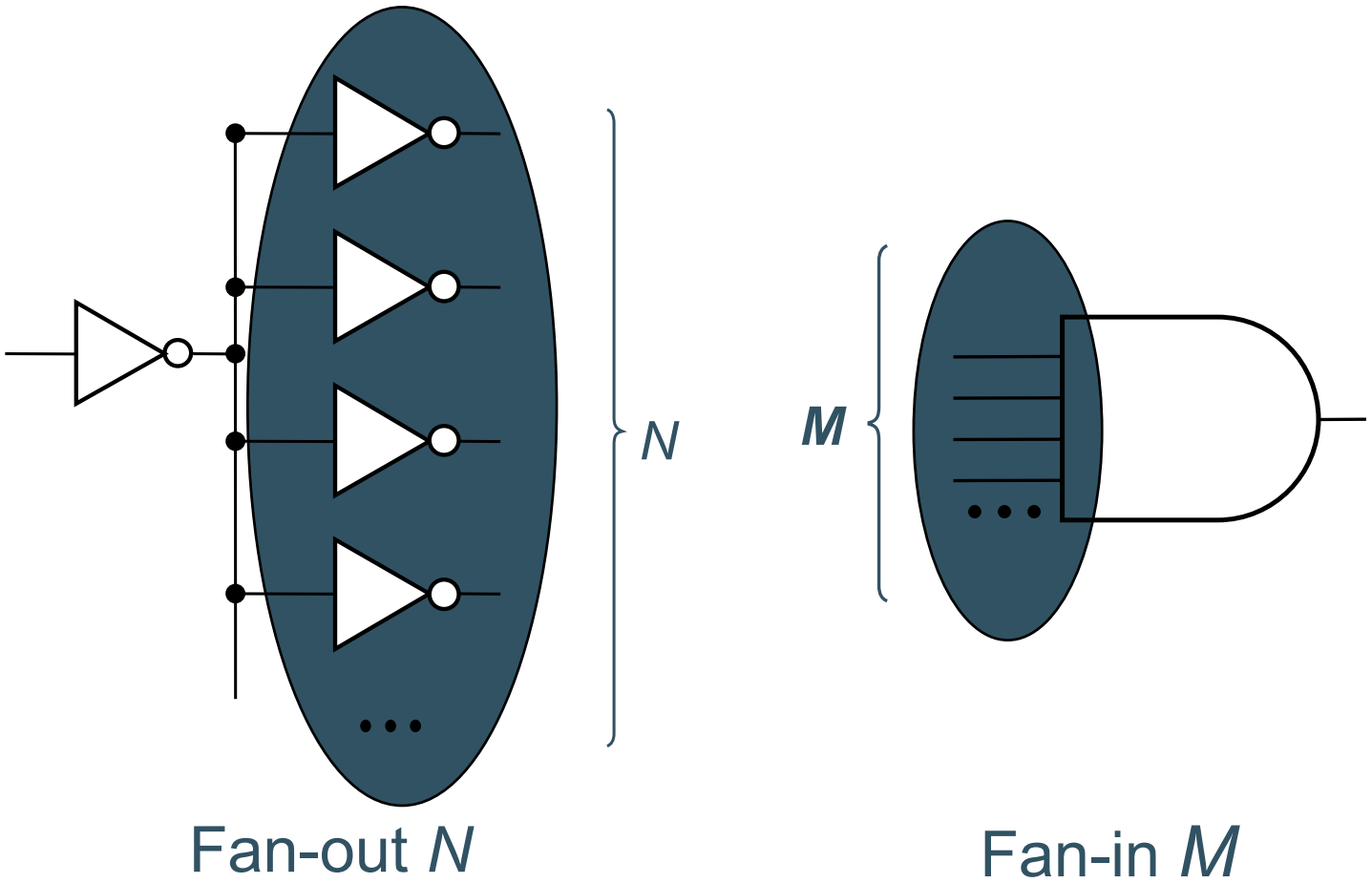
CHARACTERISTICS OF DIGITAL ICs

Directivity

- Digital gates are expected to be Unidirectional
  - Changes in the output should not affect the signals at the input
- Fully directivity cannot be achieved
  - Feedback
  - Coupling

CHARACTERISTICS OF DIGITAL ICs

Fan-in and Fan-out



Fan-out Criteria

- Fan-Out Definition:

  Maximum number of loads (N) that a gate can handle without degrading its functionality or performance.

  – Current-voltage criteria

$$N = \min\left\{\left|\frac{I_{OH}}{I_{IH}}\right|, \left|\frac{I_{OL}}{I_{IL}}\right|\right\}$$

  – Performance criteria

$$N = \min\left\{\left|\frac{C_{LH\max}}{C_{in}}\right|, \left|\frac{C_{HL\max}}{C_{in}}\right|\right\}$$

CHARACTERISTICS OF DIGITAL ICs

Power Dissipation

Instantaneous power:

$$p(t) = v(t)i(t) = V_{supply}i(t)$$

Peak power:

$$P_{peak} = V_{supply}i_{peak}$$

Average power:

$$P_{ave} = \frac{1}{T}\int_{t}^{t+T} p(t)dt = \frac{V_{supply}}{T}\int_{t}^{t+T} i_{supply}(t)dt$$

Power Components

$$P_T = P_S + P_D$$

- Static Power (PS):
  - Consumed to hold a static logic level
- Dynamic Power (PD):
  - Associated to level transitions on the gate

Energy and Energy-Delay

Power-Delay Product (PDP) =

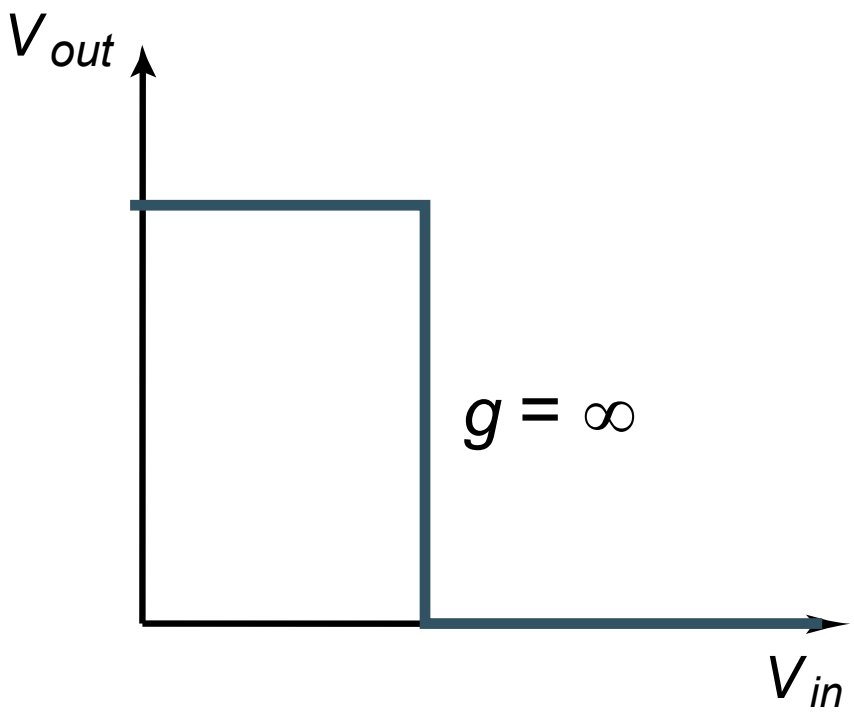
E = Energy per operation = $P_{av} \times t_p$

Energy-Delay Product (EDP) =

quality metric of gate = $E \times t_p$

CHARACTERISTICS OF DIGITAL ICs

The Ideal Gate



$$Z_i = \infty$$

$$Z_O = 0$$

$$N = \infty$$

$$LS = V_{DD} - V_{SS}$$

$$NM_H = NM_L = \frac{V_{swing}}{2}$$

$$t_{PD} = 0$$

$$P_D = 0$$