CHARACTERISTICS OF DIGITAL ICs

Regenerative Property

\[ f(v) \]

![Regenerative Property Diagram](image)
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Effect of Regenerative Property

A chain of inverters

Simulated response
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Key Reliability Properties

• Absolute noise margin values are deceptive
  – A floating node is more easily disturbed than a node driven by a low impedance (in terms of voltage)

• Noise immunity is the most important metric
  – Defines the circuit capability to suppress noise sources

• Key metrics:
  – Noise transfer functions
  – Output impedance of the driver
  – Input impedance of the receiver
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Noise Budget

• Allocates gross noise margin to expected sources of noise

• Differentiate between fixed \( V_{Nf} \) and proportional \( V_{sw} \) noise sources

\[
V_{NM} = \frac{V_{sw}}{2} \geq \sum_{i} f_i V_{Nfi} + \sum_{j} g_j V_{sw}
\]

• Sources: supply noise, cross talk, interference, offset
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Directivity

• Digital gates are expected to be Unidirectional
  – Changes in the output should not affect the signals at the input

• Fully directivity cannot be achieved
  – Feedback
  – Coupling
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Fan-in and Fan-out

Fan-out $N$

$N$

$M$

Fan-in $M$
Fan-out Criteria

• Fan-Out Definition:

Maximum number of loads (N) that a gate can handle without degrading its functionality or performance.
  – Current-voltage criteria

\[
N = \min\left\{ \frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}} \right\}
\]

  – Performance criteria

\[
N = \min\left\{ \left| \frac{C_{LH_{\max}}}{C_{in}} \right|, \left| \frac{C_{HL_{\max}}}{C_{in}} \right| \right\}
\]
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Power Dissipation

Instantaneous power:
\[ p(t) = v(t)i(t) = V_{\text{supply}}i(t) \]

Peak power:
\[ P_{\text{peak}} = V_{\text{supply}}i_{\text{peak}} \]

Average power:
\[ P_{\text{ave}} = \frac{1}{T} \int_{t}^{t+T} p(t)dt = \frac{V_{\text{supply}}}{T} \int_{t}^{t+T} i_{\text{supply}}(t)dt \]
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**Power Components**

\[ P_T = P_S + P_D \]

- **Static Power (PS):**
  - Consumed to hold a static logic level
- **Dynamic Power (PD):**
  - Associated to level transitions on the gate
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Energy and Energy-Delay

Power-Delay Product (PDP) =

\[ E = \text{Energy per operation} = P_{av} \times t_p \]

Energy-Delay Product (EDP) =

quality metric of gate = \[ E \times t_p \]
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The Ideal Gate

\[ g = \infty \]

\[
\begin{align*}
Z_i &= \infty \\
Z_O &= 0 \\
N &= \infty \\
LS &= V_{DD} - V_{SS} \\
NM_H &= NM_L = \frac{V_{swing}}{2} \\
t_{PD} &= 0 \\
P_D &= 0
\end{align*}
\]