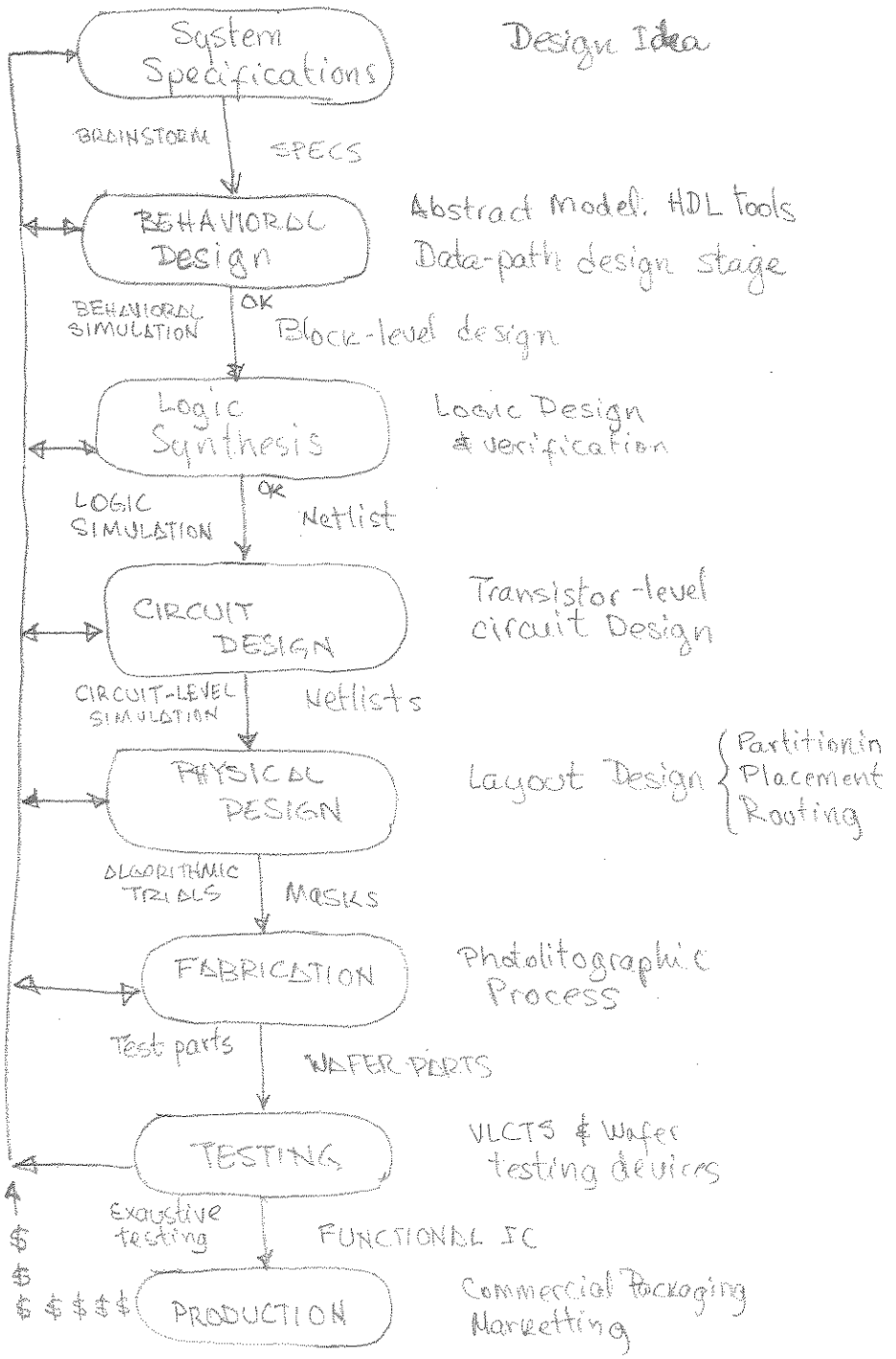
VLSI Overview

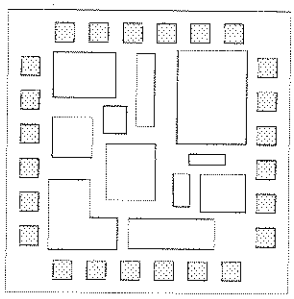
VLSI: Very Large Scale Integration = IC with over 10^6 gates

Current level: Over 10^8 transistors

Design Hierarchy: Sequence of design steps required to complete a design

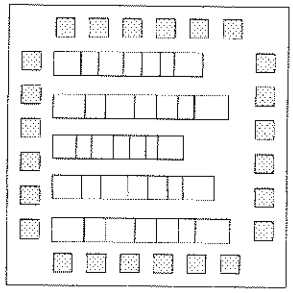


ASIC Design Styles:

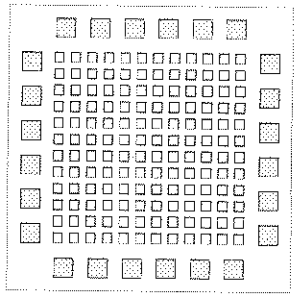


Macro Blocks

Full-custom



Standard Cells



Gate Arrays

Semi-custom

Full custom: Handcrafted design. Manually optimized Highly optimized. Very expensive. Also called MACRO-BLOCK style

Semi-Custom: Employs libraries of pre-defined building blocks.

Specific sub-styles depend on employed structures. Most commonly used styles include standard cells and Gate arrays

Moore's Law: "The number of transistors on a chip will double about every 18 months"

Gordon Moore, 1970

How long will it continue?

Now-a-days at about 10^8

Logic Design with MOSFETs

Book terminology:

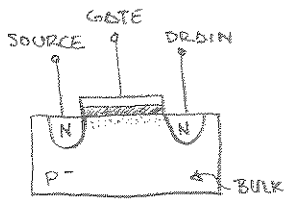
Assertion-level : Level of control signal required for an action to take place

Asserted-high Vs. Asserted-low

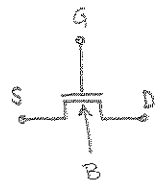
Series-connection ⇒ anded control signals

Parallel-connection ⇒ ored control signals

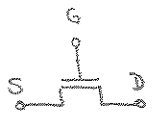
MOSFETs as switches



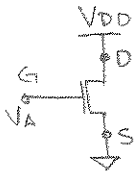
NMOS

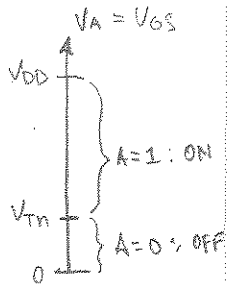


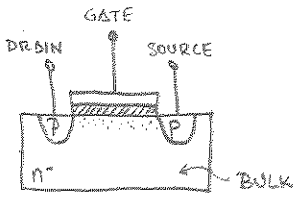
4-Terminal NMOS



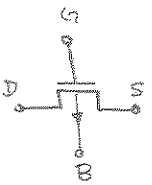
NMOS Switch



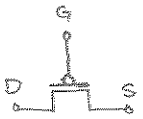




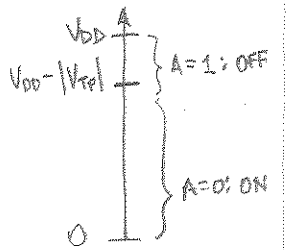
PMOS



4-Terminal PMOS

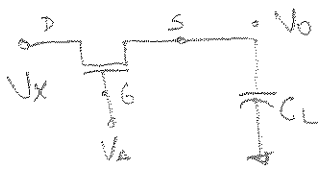


PMOS SWITCH



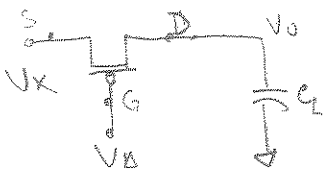
Threshold Voltage V_T : $V_{GSn} \leq V_{Tn}$ ← NMOS OFF

$V_{GSp} \geq V_{Tp}$ ← PMOS OFF



When $V_X = 0V$, $V_A = V_{DD}$, $V_O = 0V$
Strong Low

When $V_X = V_{DD}$, $V_A = V_{DD}$, $V_{O_{MAX}} = V_{DD} - V_{Tn}$
Weak high



$V_X = 0V$, $V_A = 0V$ $V_O = V_{Tp}$
weak low

$V_A = 0V$, $V_A = 0V$ $V_O = V_{DD}$
strong high

MOSFETs pass characteristics can be summarized as

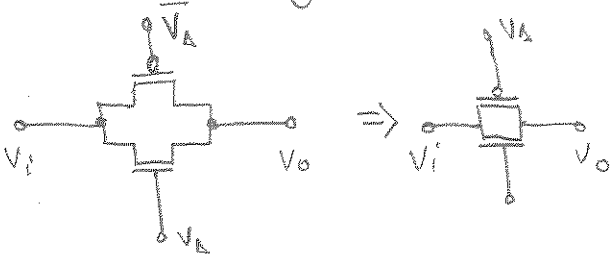
NMOS:

V_A	V_i	V_o
L	X	Z
H	L	L
H	H	h

PMOS:

V_A	V_i	V_o
L	L	l
L	H	H
H	X	Z

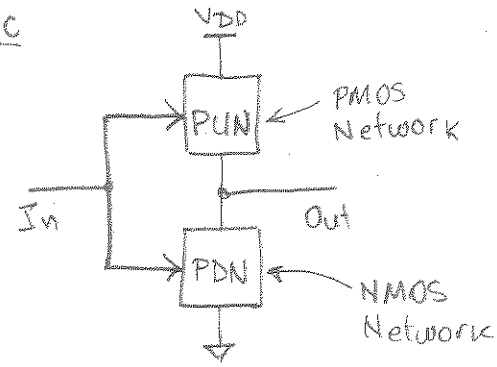
Transmission gates:



Provides both strong L and strong H due to complementary structure.

CMOS Logic

Structure:



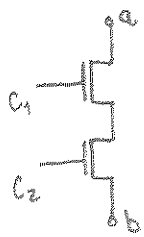
PUN = Pull-up network
Takes the output to high

PDN = Pull-down network
Takes the output to low

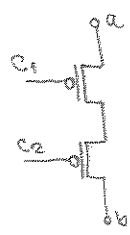
Constructing the PDN & PUN:

Recall that:

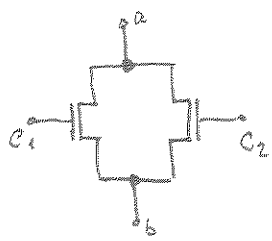
- anded variables ⇒ series connection
- ored variables ⇒ paralled connection
- NMOS imply non-inverted variables ($V_{Tn} > 0$)
- PMOS " inverted variables ($V_{Tp} < 0$)



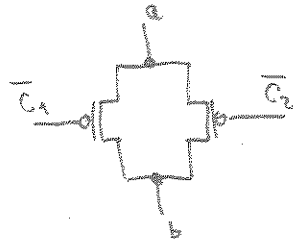
$C_1 \cdot C_2$
Low



$\overline{C_1} \cdot \overline{C_2}$
High



$C_1 + C_2$
Low

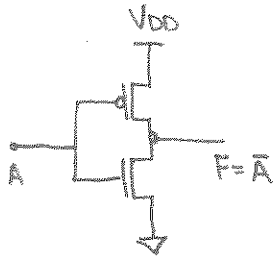


$\overline{C_1} + \overline{C_2}$
High

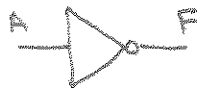
MOSFET connections & equations for passing a⇔b

• CMOS gates are intrinsically inverting gates.

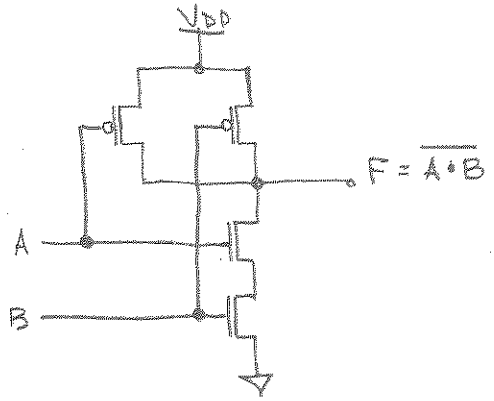
Inverter: $F = \overline{A}$



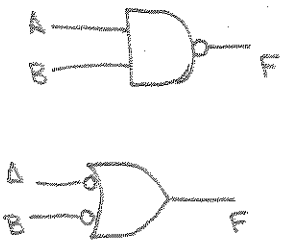
A	F
L	H
H	L



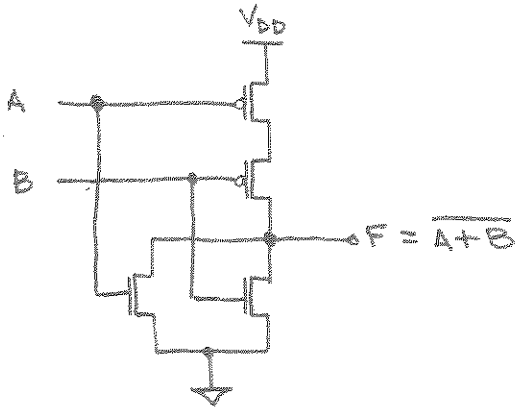
NAND Gate



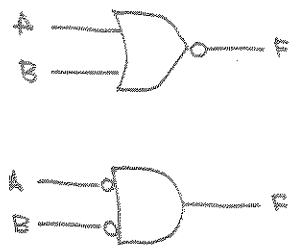
A	B	F
L	L	H
L	H	H
H	L	H
H	H	L



NOR Gate



A	B	F
L	L	H
L	H	L
H	L	L
H	H	L



General Approach

① Separate the function into complementary subfunctions for

- PUN → f(H) → Drives F to High
- PDN → f(L) → Drives F to Low

② Make: $f(H) = F$, applying D'Morgan until you get single inverted variables

$f(L) = \overline{F}$, also apply D'Morgan if necessary to obtain single non-inverted variables

③ Construct & connect the networks using series/parallel FETS

Example: $F = \overline{A + B \cdot (C+D)}$

$$f(H) = F = \overline{A + B \cdot (C+D)} = \overline{A} \cdot \overline{B \cdot (C+D)}$$

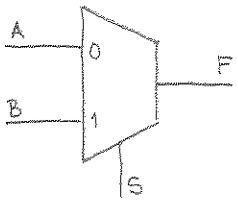
$$= \overline{A} \cdot (\overline{B} + \overline{(C+D)})$$

$$= \overline{A} \cdot (\overline{B} + (\overline{C} \cdot \overline{D})) \quad \text{OK}$$

$$f(L) = \overline{F} = \overline{\overline{A + B \cdot (C+D)}} = A + B \cdot (C+D) \quad \text{OK}$$

Multiplexers (MUX)

Consider a 2-to-1 MUX

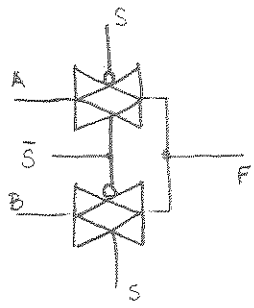


Symbol

A	B	S	F	
L	X	L	L	A
H	X	L	H	A
X	L	H	L	B
X	H	H	H	B

Truth table

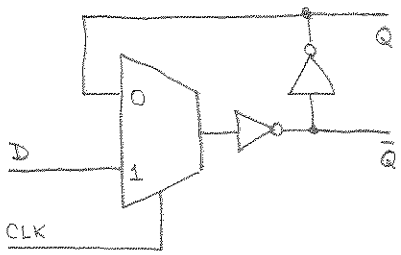
$F = A\bar{S} + BS$



Schematic

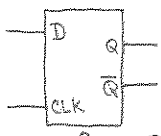
Memory Elements

Level sensitive data latch:



Operation: CLK = 1 → Load → Q = D

SYMBOL



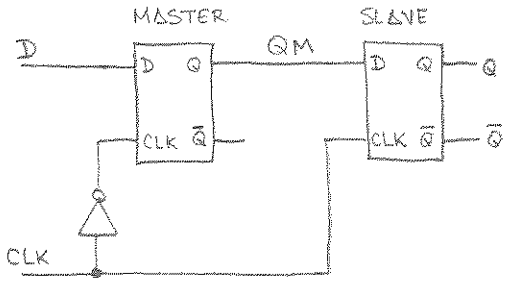
CLK = 0 → Hold → $Q = Q_{t-1}$

Q_{t-1} = Previous value of Q

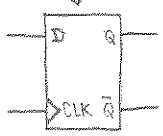
Positive level sensitivity

How would you convert it to negative level sensitivity?

Edge Sensitive data latch:



Rising (or positive) edge sensitivity



Symbol

How would you change it to falling edge sensitivity?

Operation:

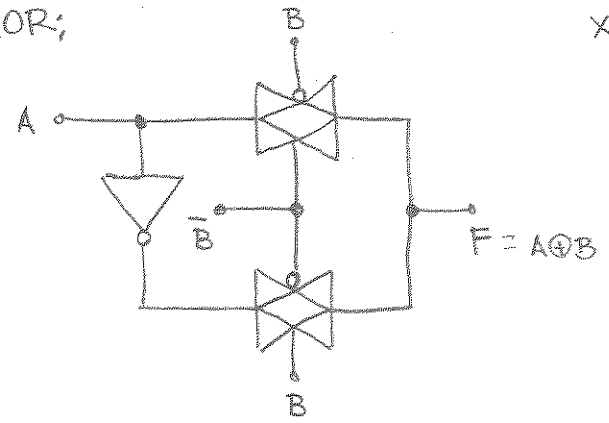
CLK = 0 master is loaded while slave holds the previous value

CLK = 0 → 1 master stops sampling and slave begins sampling the master's output (QM).

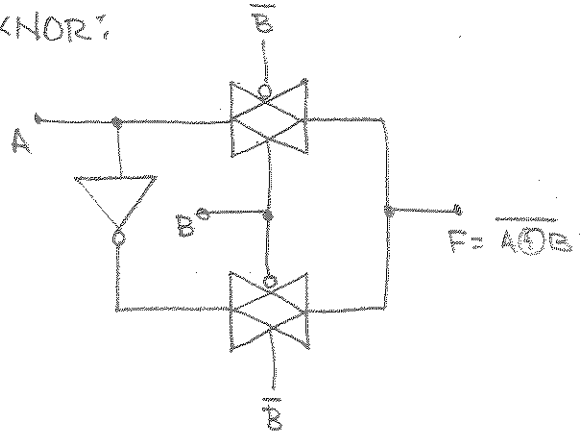
CLK = 1 → 0 master samples and slave holds.

A Few TG-based Circuits:

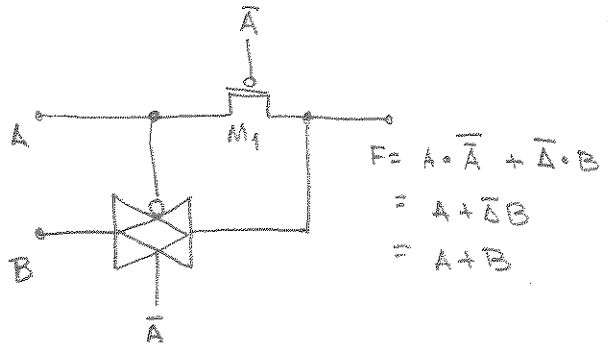
XOR:



XNOR:

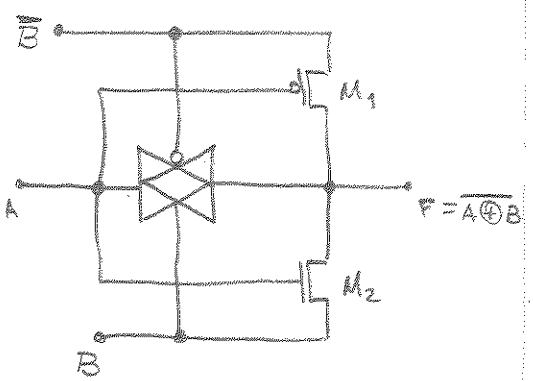


OR:



Note that M_1 only passes A = High

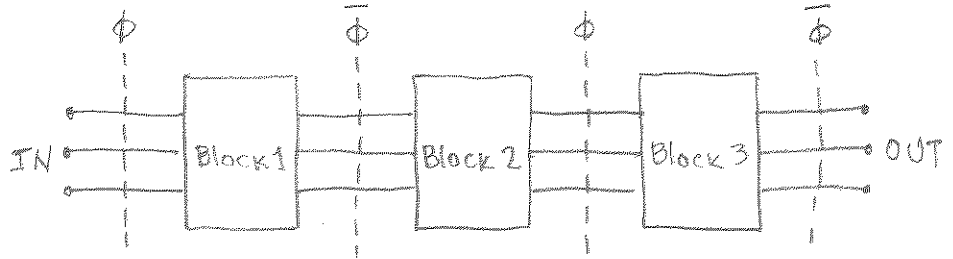
XNOR:



Exchange B & $\bar{B}$ to get XOR

Clocking with TG

- Made possible by $t_{hold} \neq 0$ at the TG output.
- Requires $(T/2) < t_{hold}$
- Phase of clk signal is alternated between stages



- Very useful in synchronous combinational circuits & pipelines as long as $T/2 < t_{hold}$
- Longer T values require explicit latches