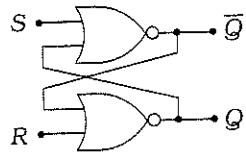
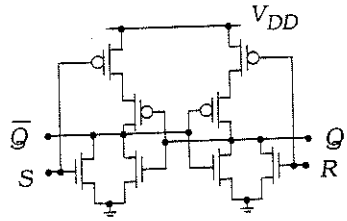
A couple of latch implementations:

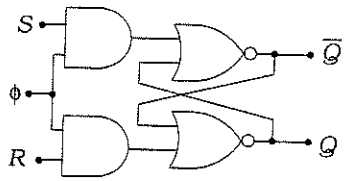


(a) Logic diagram

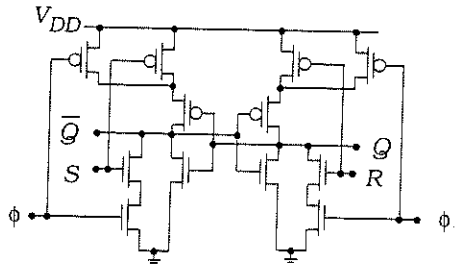


(b) CMOS circuit

Simple NOR-based SR latch



(a) Logic diagram



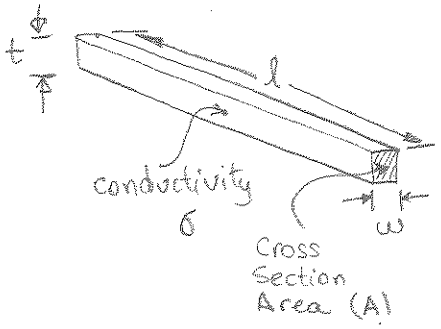
(b) CMOS circuit

Clocked SR latch. Implementation based on AOI gates

Physical Structure of CMOS ICs

Current IC technology stacks alternating layers of metal & insulator on top of the substrate.

Resistance: Any current-conducting trace will exhibit a finite parasitic resistance.



l = trace length
t = " thickness
w = " width
} all in cm

σ = trace conductivity → $[\Omega\text{-cm}]^{-1}$ known for a given material

$\rho = 1/\sigma$ = resistivity in Ω-cm

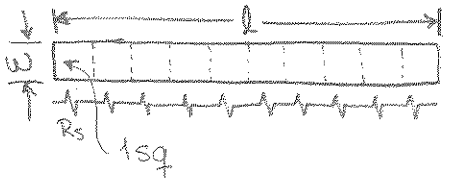
$$R_{line} = \frac{l}{\sigma A} = \rho \frac{l}{A}$$

VLSI process cannot control t or σ so $R_{line} = \frac{1}{\sigma t}\left(\frac{l}{w}\right)$

Sheet resistance $R_S = \frac{1}{\sigma t} = \rho/t \rightarrow \Omega$

- Conducting layers are characterized by their sheet resistance
- Note that if $w = l \Rightarrow R_{line} = R_S \frac{w}{w} = R_S$
- R_S is usually given units of "Ω per square"
- Line resistance can be computed using these units as:

$$R_{line} = R_S n, \quad \text{where} \quad n = l/w$$



← A line trace of length l and width w (top view)

Capacitance: Any two conducting bodies electrically separated will develop a parasitic capacitance between them

$Q = CV$ ← Charge in the positive side
Capacitance value → ↑ voltage difference

Since $I = dQ/dt$ the I-V equation for a capacitor is

$$I = C\, dV/dt$$

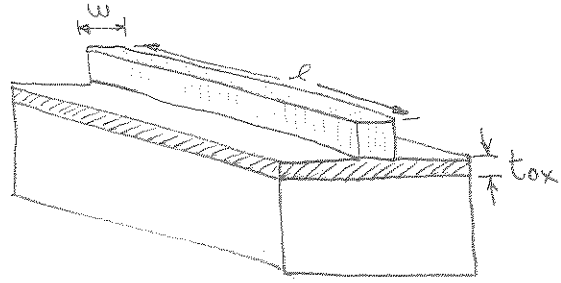
For a conducting trace of:

length ℓ
width w
separated from the substrate t_{ox}

$$C_{line} = \varepsilon_{ox} \frac{w\,\ell}{t_{ox}}$$

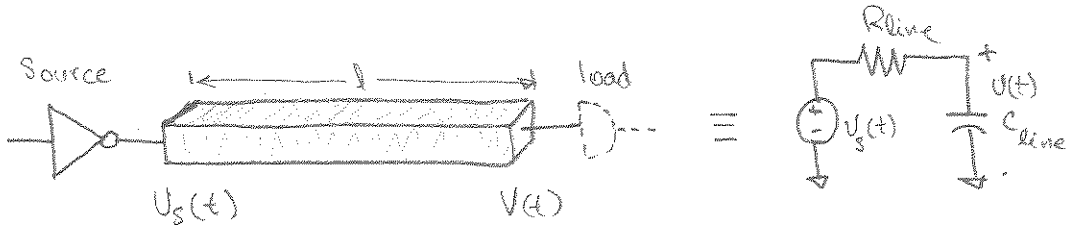
ε_{ox} = Oxide permittivity in F/cm

C_{line} obtained as above ignores the fringing fields due to the wire geometry and mutual effects of surrounding conductors

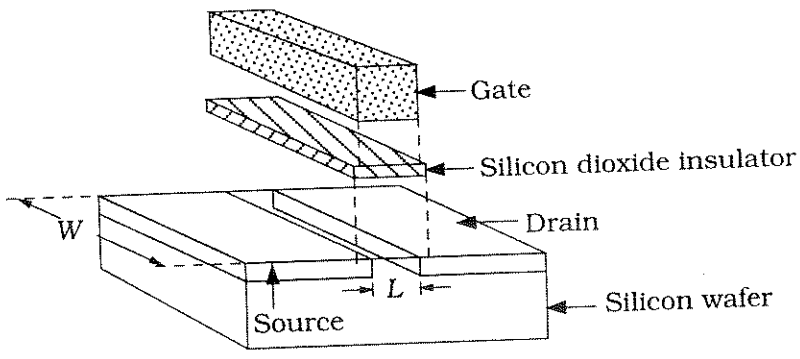


Line delay: Is a function of the line time constant

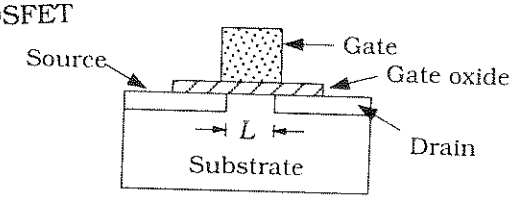
$$\tau = R_{line} C_{line}$$



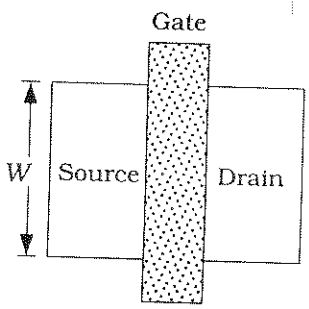
MOSFETs Layout:



Layers used to create a MOSFET



(a) Side view



(b) Top view

Views of a MOSFET

- Pure silicon is a semiconductor (intrinsic material)

$$N_{Si} = 5 \times 10^{22} \text{ atoms/cm}^3$$

- Only thermally liberated carriers exist in a pure semiconductor
- Intrinsic electron density at room temperature

$$N_i = 1.45 \times 10^{10} \text{ cm}^{-3} \quad @ 300^\circ K$$

- N_i increases with temperature
- Free electrons Vs holes : Electron-hole pair (n, p)
- In an intrinsic material $n = p \Rightarrow n \cdot p = n_i^2$
- Silicon conductivity enhanced by impurities
- Impurities added through a doping process
- Impurity type determines resulting material (p or n)
- Impurity concentrations:

$N_a \rightarrow$ acceptor concentration

$N_d \rightarrow$ donor concentration

Electron density: $n_n = N_d \text{ cm}^{-3}$ ← majority carriers

Hole density (in n-sample) = $p_n = \frac{n_i^2}{N_d} \text{ cm}^{-3}$ ← Minority carrier

Same applies for a p-sample. (based on N_a)

Conductivity of a semiconductor region with carrier densities p & n

$$\sigma = q(\mu_n n + \mu_p p)$$

μ_n μ_p → Electron & hole mobility factors in $\text{cm}^2/\text{V-sec}$

For intrinsic silicon: $\mu_n = 1360$ $\mu_p = 480$

For doped silicon:

$$\sigma_n = q \mu_n n_n \leftarrow \text{n-type}$$

$$\sigma_p = q \mu_p p_p \leftarrow \text{p-type}$$

Impurity scattering: mobility is a function of doping concentration N

$$\mu(N) = \mu_1 + \frac{\mu_2 - \mu_1}{1 + \left(\frac{N}{N_{ref}}\right)^a}$$

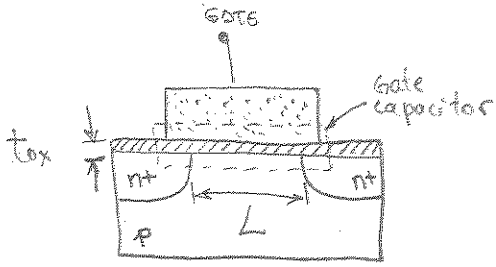
In general $\mu_n > \mu_p$

- In CMOS processing, region types are determined by dominant concentrations.

So $n_n = N_d - N_a$ $\quad p_n = \frac{n_i^2}{(N_d - N_a)}$ ← n-type

Likewise for p-type

For a MOS transistor (NMOS)



$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ ← oxide permittivity

$C_G = W \cdot L \cdot C_{ox}$

Threshold Voltage: Minimum V_G required to take the gate capacitor into inversion mode. This creates the channel

$Q_c = -C_G (V_G - V_{Tn})$
↖ channel charge

Once in inversion mode ($V_G - V_{Tn} > 0$) $I = \frac{|Q_c|}{\tau_t}$ Coulomb/sec

τ_t = transit-time; mean-time for carriers to travel from S to D

$\tau_t = \frac{L}{v}$ ← electron velocity

So $I = \frac{C_G}{(L/v)} (V_G - V_{Tn}) = v\, C_{ox}\, W (V_G - V_{Tn})$

Using $v = \mu E$ where $E = \frac{V}{L}$
↖ electric field

Combining these equations we obtain

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_G - V_{tn}) V \qquad (1)$$

Making $\mu_n C_{ox} \frac{W}{L} = \beta_n$ → Device transconductance. Also called K_n

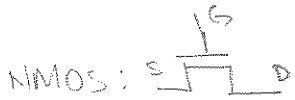
$$R_n = \frac{V}{I} = \frac{1}{\beta_n (V_G - V_{tn})}$$ ← Linear NMOS Resistance (Similarly for PMOS)

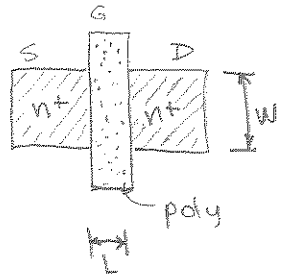
CMOS processing:

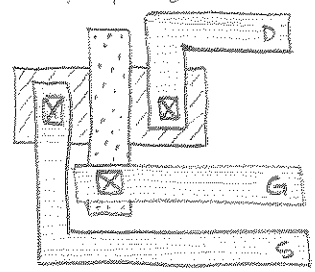
- Substrate p- (or simply p)
- n-well
- source-drain diffussions (n^+ or p^+)
- Gate-oxide
- Poly
- Metalization

Transistors are created at the intersection of poly & difossion

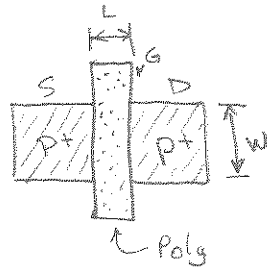
NMOS:



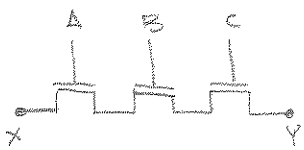


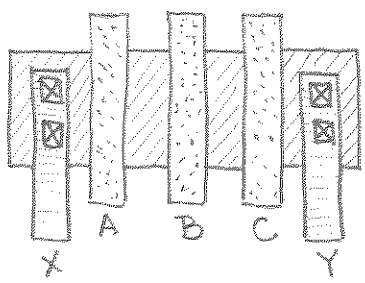


PMOS:



Series MOSFETS

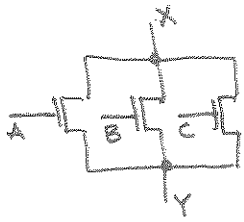


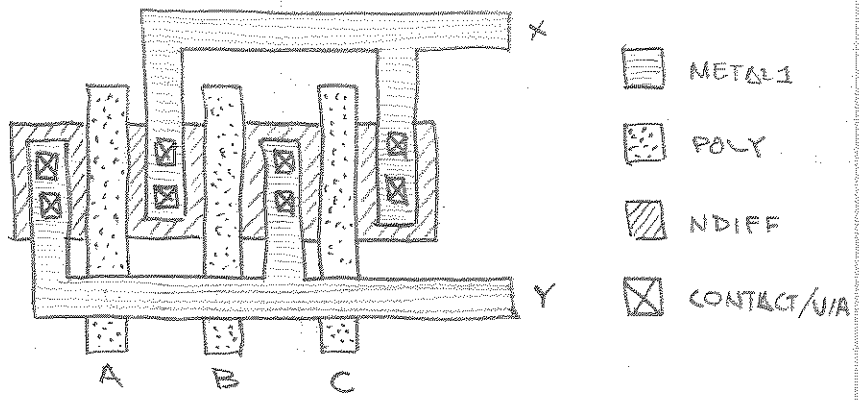


Multiple devices can share S/D regions allowing for compact layouts

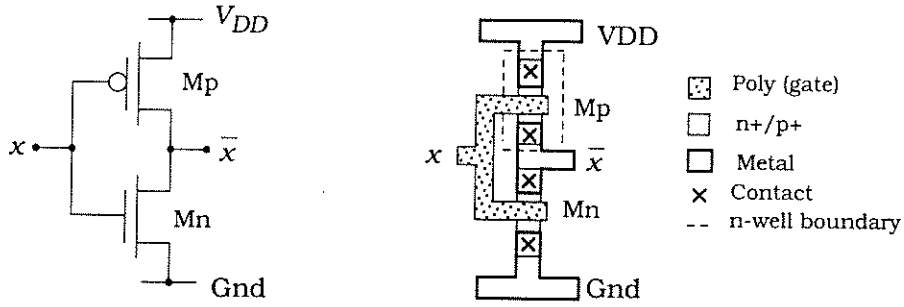
Note that all S/D areas share a single n^+ diffusion

Parallel MOSFETS



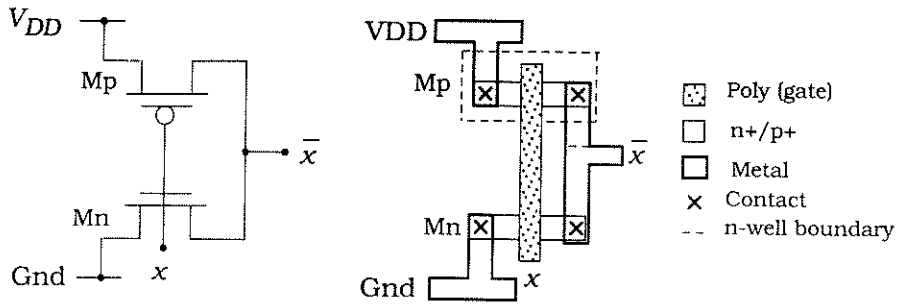


CMOS Layout :



(a) Circuit (b) Layer patterning

Figure 3.31 Translating a NOT gate circuit to silicon



(a) Circuit (b) Layer patterning

Figure 3.32 Alternate layout for a NOT gate

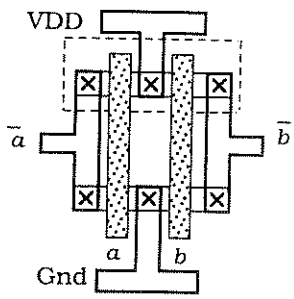
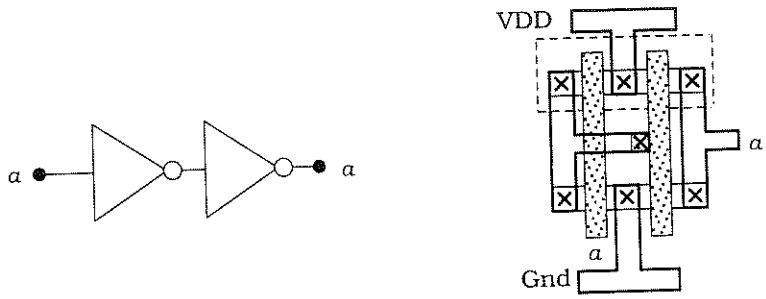


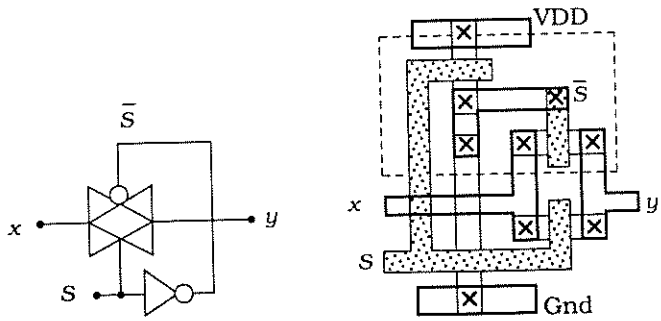
Figure 3.33 Two NOT gates that share power supply and ground

(Continue to handout : "Complex Gates Layouts")



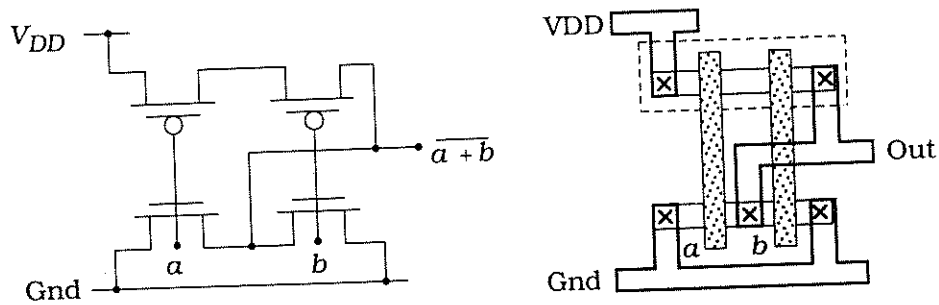
(a) Logic diagram (b) Layout

Figure 3.34 Non-inverting buffer



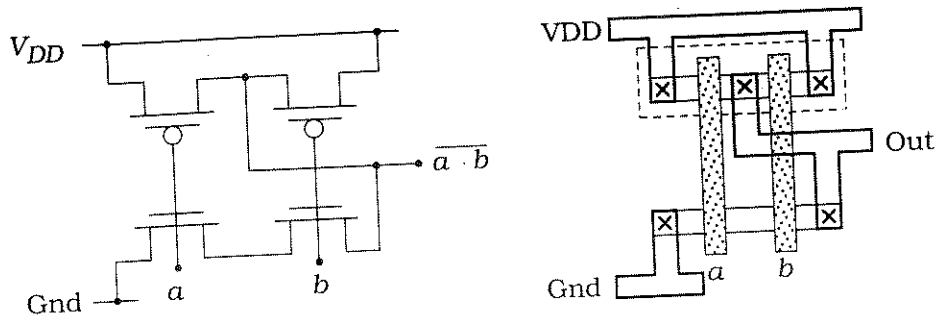
(a) Logic diagram (b) Layout

Figure 3.35 Layout of a transmission gate with a driver



(a) Circuit (b) Layer design

Figure 3.37 NOR2 gate design



(a) Circuit (b) Layer design

Figure 3.36 NAND2 layout