CMOS Fabrication

Definitions:

Wafer: circular Silicon sheet, typically 100-300 mm diameter, 0.4 - 0.7 mm thick where ICs are fabricated

Die: Square containing a single IC. Large die: about 1cm x 1cm

Die site: location of an IC on a wafer

Flat: Reference plane for die sites in a wafer

Wafer Starts (per week): No. of fresh wafers introduced for fabrication in a week. Its a measure of a FAB capacity

Yield: Efficiency of a fabrication process

$$Y = \frac{N_G}{N_T} \ (\%)$$

N_G = No. of good ICs
N_T = Total No of die sites per wafer

$$N_T = \pi \frac{(d - d_e)^2}{4 A_{die}}$$

(costly)

d = Raw wafer diameter
d_e = Wasted edge distance
A_{die} = die area

Empirical Yield estimate

$$Y = e^{-\sqrt{D A_{die}}}$$

D = Defect density factor in cm^{-2} (Intrinsic density of silicon defects $\sim 1\ cm^{-2}$)

or

$$Y = \frac{1}{\left(1 + \frac{A_{die} D}{c}\right)^2}$$

c = cluster constant when defects tend to occur in clusters

See [3] for a more complete treatment of this subject.

or

$$Y \cong (1 - g) e^{-A_{die} D}, \text{ where } g = \frac{A_{fail}}{A_{wafer}}, \text{ and}$$

A_{fail} = Fail area, when defects tend to be related to relatively large areas of a wafer

Model to be used depends on process (EXPERIENCE)

Fabrication Process

Mostly a Chemical-optical process composed of several steps of deposition & etching of material layers.

Deposition typically affect the entire wafer
Etching uses photo masks to leave only the desired patterns

MATERIALS:

- Silicon Dioxide (SiO_2):
  - Excellent insulator
  - Highly adhesive
  - Can be grown or deposited
  - Highly controlable even on very thin layers

Thermal Oxide: Formed by chemical reaction on the wafer surface, under heat.

$$Si + O_2 \xrightarrow{\Delta} SiO_2$$

Dry oxidation: Uses pure oxigen. Slow and precise layers

Wet oxidation: Uses water vapor. Faster & less precise

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

Thermal oxide is also called "native oxide": it grows from the wafer itself.

A layer X_{Si} is lost from the wafer to create an oxide layer of thickness x_{ox}

$$X_{Si} \approx 0.46\, x_{ox}$$

Oxide Deposition: Allows to grow oxide layers well above the silicon layer.
Uses silane gas (SiH_4)

$$\underset{\text{gas}}{SiH_4} + 2\underset{\text{gas}}{O_2} \rightarrow \underset{\text{solid}}{SiO_2} + 2\underset{\text{gas}}{H_2O}$$

→ CVD oxide Chemical Vapor Deposition

- Silicon Nitride (Si_3N_4):
  - Acts as a strong barrier against other atoms (overglass)

$$\underset{\text{gas}}{3SiH_4} + \underset{\text{gas}}{4NH_3} \rightarrow \underset{\text{solid}}{Si_3N_4} + \underset{\text{gas}}{12H_2}$$

Overglass: • Final protective coating on a chip
• Isolation of adjacent fets
• As dielectric on capacitors.

• Polysilicon: Deposition of highly doped Si on amorphous SiO_2 layer.

$$SiH_4 \xrightarrow{\Delta} Si + 2H_2$$

A similar process on crystaline silicon used to grow epitaxial layers.

• Metals: Aluminum (Al) & Copper (Cu)

Aluminum is the most widely used metal on IC fabrication

✓ Can be evaporated
✓ Excellent adhesion to Si
✓ Easy to pattern
✓ Low resistivity

$\rho_{Al} = 2.65\ \mu\Omega/cm$

x Prone to electromigration: Mass migration under the influence of current density

Voids: removed Al → open ckt
Hillocks: deposited Al → short ckt
} Source of failures in ICs

Copper has been gaining popularity

✓ Lower resistivity than Al

• Doped Silicon: Produced on the wafer to create n/p regions as needed:

Mechanisms:

1) Ion implantation: Impurities are ionized,

Design Rules:

λ Rules: Based on λ parameter dimension = mλ

Types:
- Width
- Spacing
- Surround
- Extension

Physical Design: Departs from a complete circuit design process.

1) Layout edition
   - Cell library
   - Cell instancing
2) Circuit Extraction
   - Simulation (SPICE)
3) Layout Vs. Schematic (LVS)
4) Design Rule Checking (DRC)
5) Place & Routing (PPR)
6) Electrical Rule Checking (ERC)

a) Symmetric
b) $t_{PLH} = \frac{2}{3} t_{PHL}$
c) $t_{PLH} = \frac{1}{3} t_{PHL}$
d)

Layout Structures: Typically limited to Manhattan geometry

Sequence (N-well process):

0. p-type substrate
1. n-Well
2. Active
3. Poly
4. pSelect
5. nSelect
6. Active Contact
7. Poly Contact
8. Metal 1
9. Via
10. Metal 2
11. Overglass

Width & Spacing (W & S): Refer to minimum line width w and minimum edge-to-edge separation between adjacent polygons