

CMOS Fabrication

Definitions:

Wafer: ^{circular} Silicon sheet, typically 100-300 mm diameter, 0.4-0.7 mm thick where ICs are fabricated

Die: Square containing a single IC. Large die: about 1cm x 1cm

Die site: Location of an IC on a wafer

Flat: Reference plane for die sites in a wafer

Wafer Starts (per week): No. of fresh wafers introduced for fabrication in a week. Its a measure of a FDB capacity

Yield: Efficiency of a fabrication process

$$Y = \frac{N_G}{N_T} (\%)$$

$N_G = \text{No. of good ICs}$
 $N_T = \text{Total No of die sites per wafer}$

$$N_T = \pi \frac{(d - d_e)^2}{4A_{die}}$$

costly \nearrow

$d = \text{Raw wafer diameter}$
 $d_e = \text{wasted edge distance}$
 $A_{die} = \text{die area}$

Empirical Yield estimate

$$Y = e^{-\sqrt{DA_{die}}}$$

$D = \text{Defect density factor in cm}^{-2}$
 (Intrinsic density of silicon defects $\sim 1 \text{ cm}^{-2}$)

or $Y = \frac{1}{\left(1 + \frac{A_{die} D}{c}\right)^2}$

$c = \text{cluster constant when defects tend to occur in clusters}$

See [3] for a more complete treatment of this subject.

$$\text{or } Y \approx (1-g) e^{-A_{die} D}, \text{ where } g = \frac{A_{fail}}{A_{wafer}} \text{ and}$$

$A_{fail} = \text{Fail area, when defects tend to be related to relatively large areas of a wafer}$

Model to be used depends on process (EXPERIENCE)



Fabrication Process

Mostly a Chemical-optical process composed of several steps of deposition & etching of material layers.

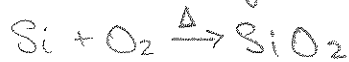
Deposition typically affect the entire wafer
Etching uses photo masks to leave only the desired patterns.

MATERIALS:

- Silicon Dioxide (SiO_2):

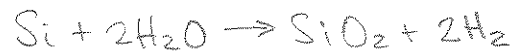
- Excellent insulator
- Highly adhesive
- Can be grown or deposited
- Highly controllable even on very thin layers

Thermal Oxide: Formed by chemical reaction on the wafer surface, under heat.



Dry oxidation: Uses pure oxygen. Slow and precise layers

Wet oxidation: Uses water vapor. Faster & less precise

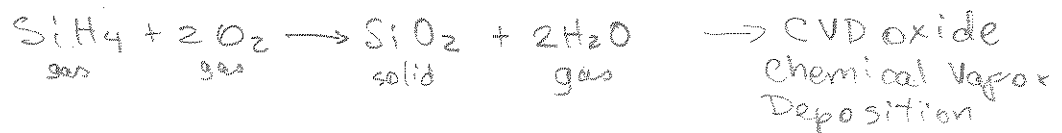


Thermal oxide is also called "native oxide": it grows from the wafer itself.

A layer X_{Si} is lost from the wafer to create an oxide layer of thickness X_{Ox}

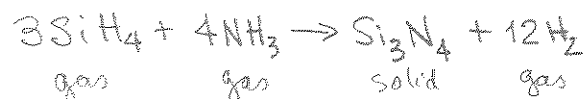
$$X_{\text{Si}} \approx 0.46 X_{\text{Ox}}$$

Oxide Deposition: Allows to grow oxide layers well above the silicon layer.
Uses silane gas (SiH_4)



- Silicon Nitride (Si_3N_4):

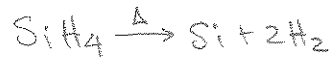
- Acts as a strong barrier against other atoms (overglass)



Overglass: Final protective coating on a chip

- Isolation of adjacent nets
- As dielectric on capacitors.

- Polysilicon: Deposition of highly doped Si on amorphous SiO_2 layer.



A similar process on crystalline silicon used to grow epitaxial layers.

- Metals: Aluminum (Al) & Copper (Cu)

Aluminum is the most widely used metal on IC fabrication

- ✓ Can be evaporated
- ✓ Excellent adhesion to Si
- ✓ Easy to pattern
- ✓ Low resistivity

$$\rho_{\text{Al}} = 2.65 \mu\Omega/\text{cm}$$

- x Prone to electromigration: Mass migration under the influence of current density

Voids: removed Al \rightarrow open ckt
 Hillocks: deposited Al \rightarrow short ckt } source of failures in ICs

Copper has been gaining popularity

- ✓ Lower resistivity than Al

- Doped Silicon: Produced on the wafer to create n/p regions as needed:

Mechanisms:

- 1) Ion implantation: Impurities are ionized,

Design Rules:

λ Rules: Based on λ parameter dimension = $m\lambda$

Types:

- Width
- Spacing
- Surround
- Extension

Physical Design: Departs from a complete circuit design process.

1) Layout edition

- Cell library
- Cell instancing

a) Symmetric

b) $t_{PLH} = \frac{2}{3} t_{PHL}$

c) $t_{PLH} = \frac{1}{3} t_{PHL}$

d)

2) Circuit Extraction

- Simulation (SPICE)

3) Layout Vs. Schematic (LVS)

4) Design Rule Checking (DRC)

5) Place & Routing (PPR)

6) Electrical Rule Checking (ERC)

Layout Structures: Typically limited to Manhattan geometry

Sequence (N-well process):

- | | |
|---------------------|-------------------|
| 0. p-type substrate | 6. Active Contact |
| 1. n-well | 7. Poly Contact |
| 2. Active | 8. Metal 1 |
| 3. Poly | 9. Via |
| 4. pSelect | 10. Metal 2 |
| 5. nSelect | 11. Overglass |

Width & Spacing (w & s): Refer to minimum line width w and minimum edge-to-edge separation between adjacent polygons

