Inel-6080
VLSI Systems Design

Design Rules for CMOS

Lecture 7

Electrical and Computer Engineering Department
University of Puerto Rico at Mayagüez

Fall 2008

Design Rules

- Allow for a ready translation of a circuit concept into an actual geometry in silicon
- Provide a set of guidelines for constructing the fabrication masks
  - Minimum line width
  - Minimum spacing between objects
- Multiple design rule specification methods exist
  - Scalable Design Rules (Lambda rules)
  - Micron Rules

Specifying Design Rules

- Lambda Rules:
  - Expressed in terms of a scaling parameter: Lambda (λ)
  - Minimum line width: 2λ
  - Main disadvantages:
    - Limited linear scaling
    - Too conservative
- Micron Rules
  - Express designs in absolute dimensions
  - Pro: Allow taking full advantage of technology
  - Con: Scaling and Porting becomes more complicated

Design Rule Entities

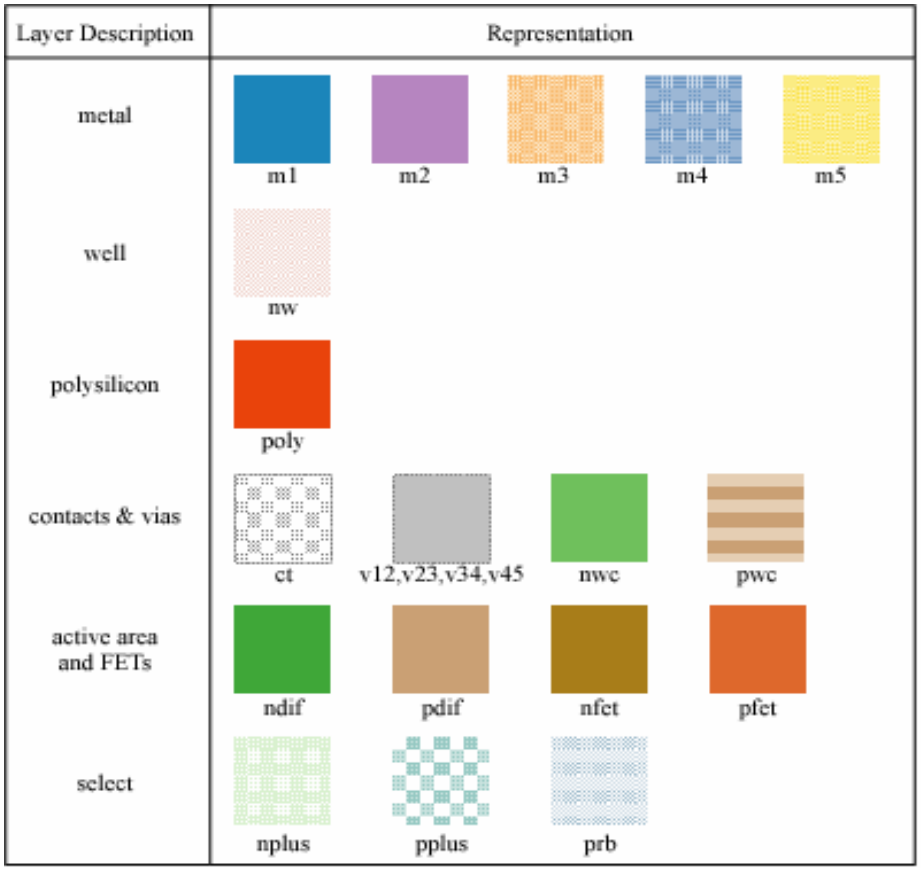
1. Layer Representations
   - Substrates and/or Wells
   - Diffusion Regions (Active areas)
     - Select regions: For contacts to substrate or well
   - Polysilicon Layers
   - Metal Interconnects
     - Contact: Metal to active
     - Via: Metal to metal
2. Intralayer Constraints
3. Interlayer Constraints

CMOS Process Layers

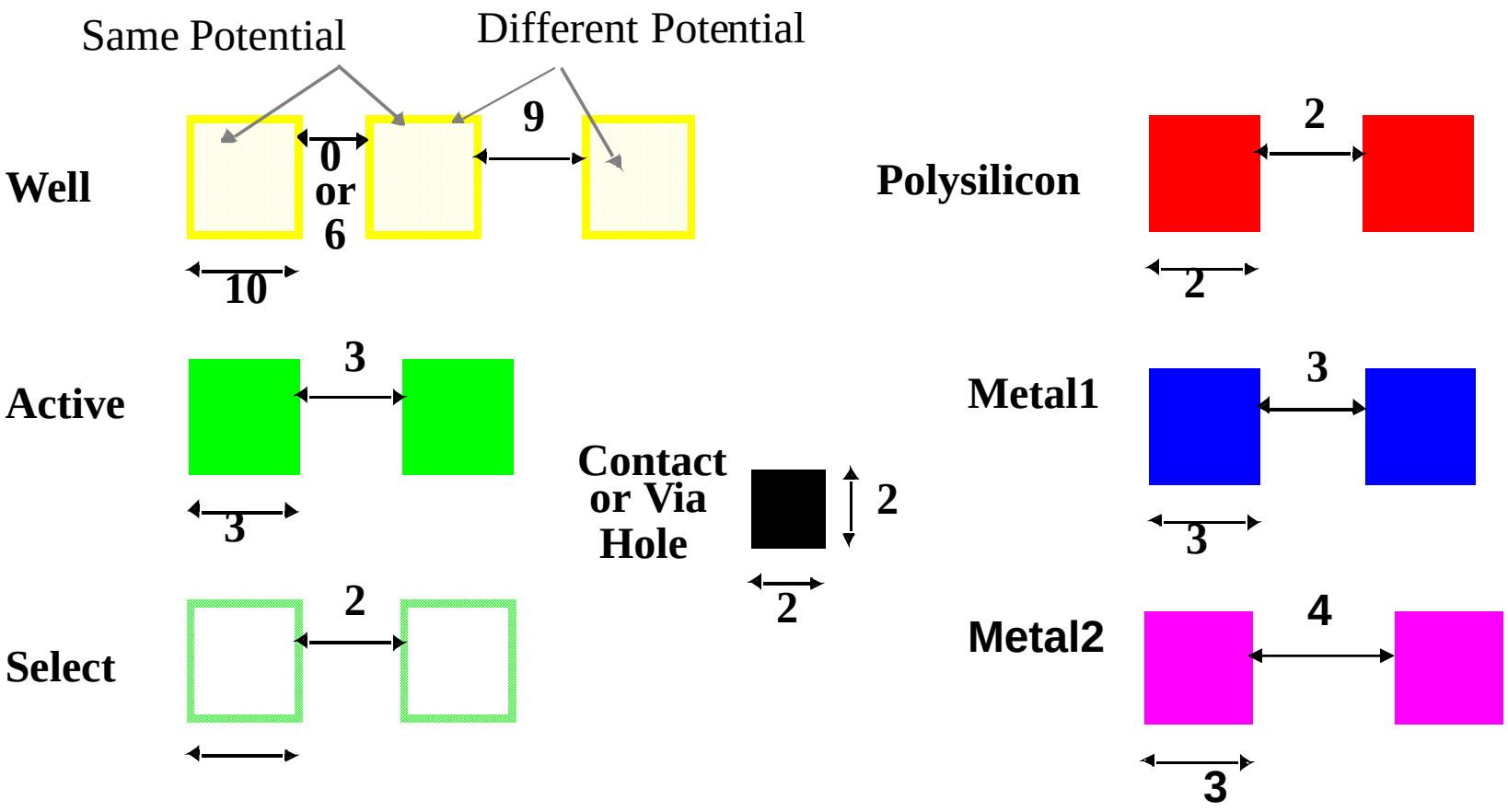
Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

DESIGN RULES AND LAYOUT

Layers in 0.25µm CMOS Process

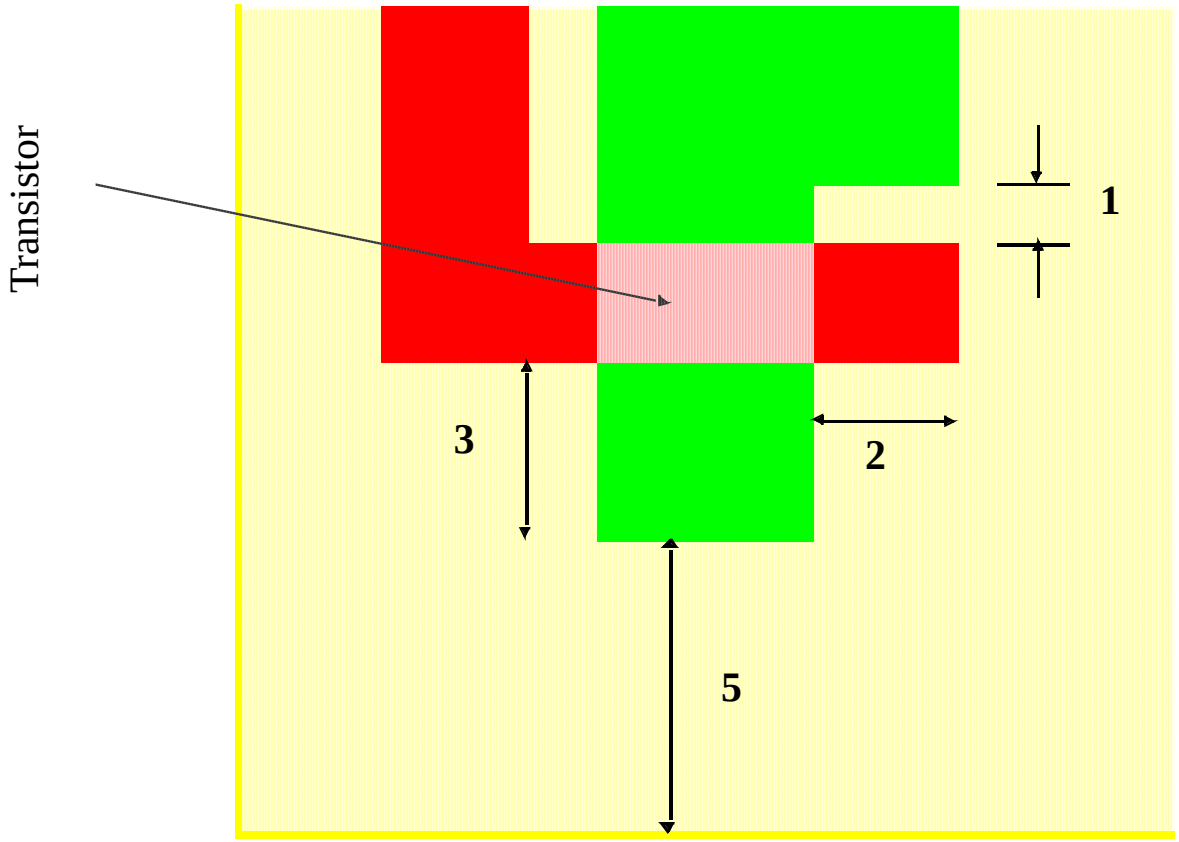


Intra-Layer Design Rules



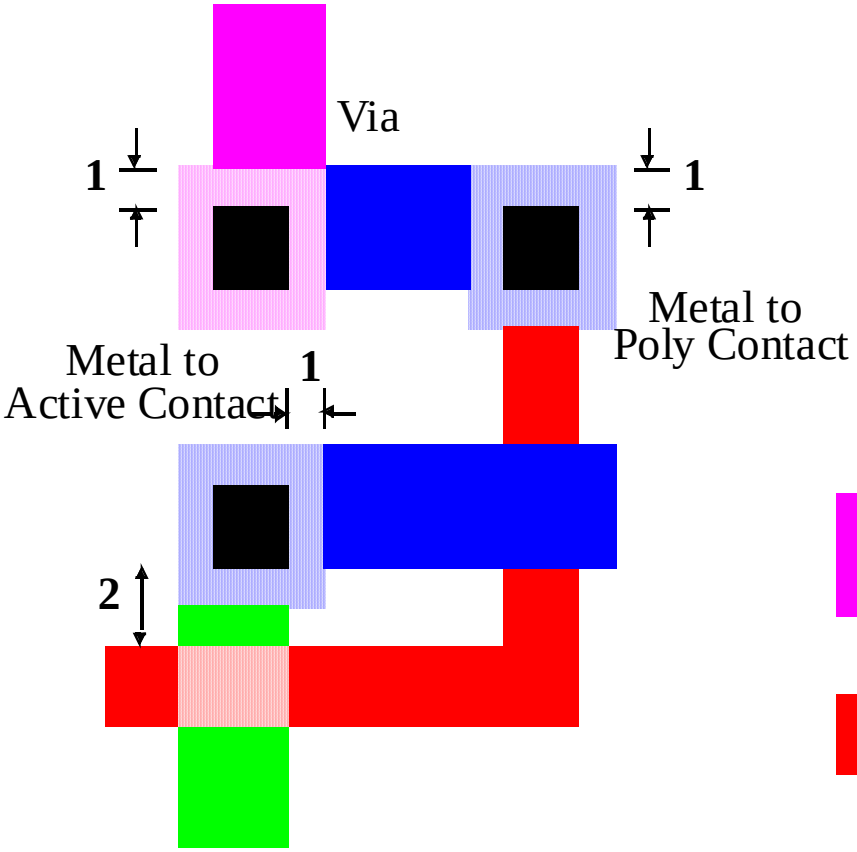
DESIGN RULES AND LAYOUT

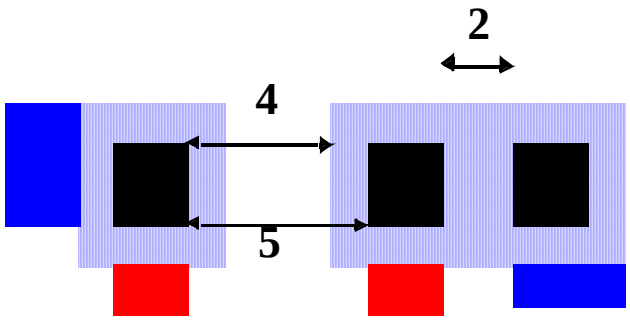
Single Transistor Layout

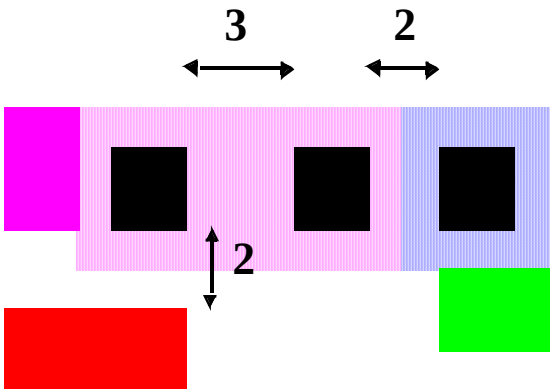


DESIGN RULES AND LAYOUT

Vias and Contacts

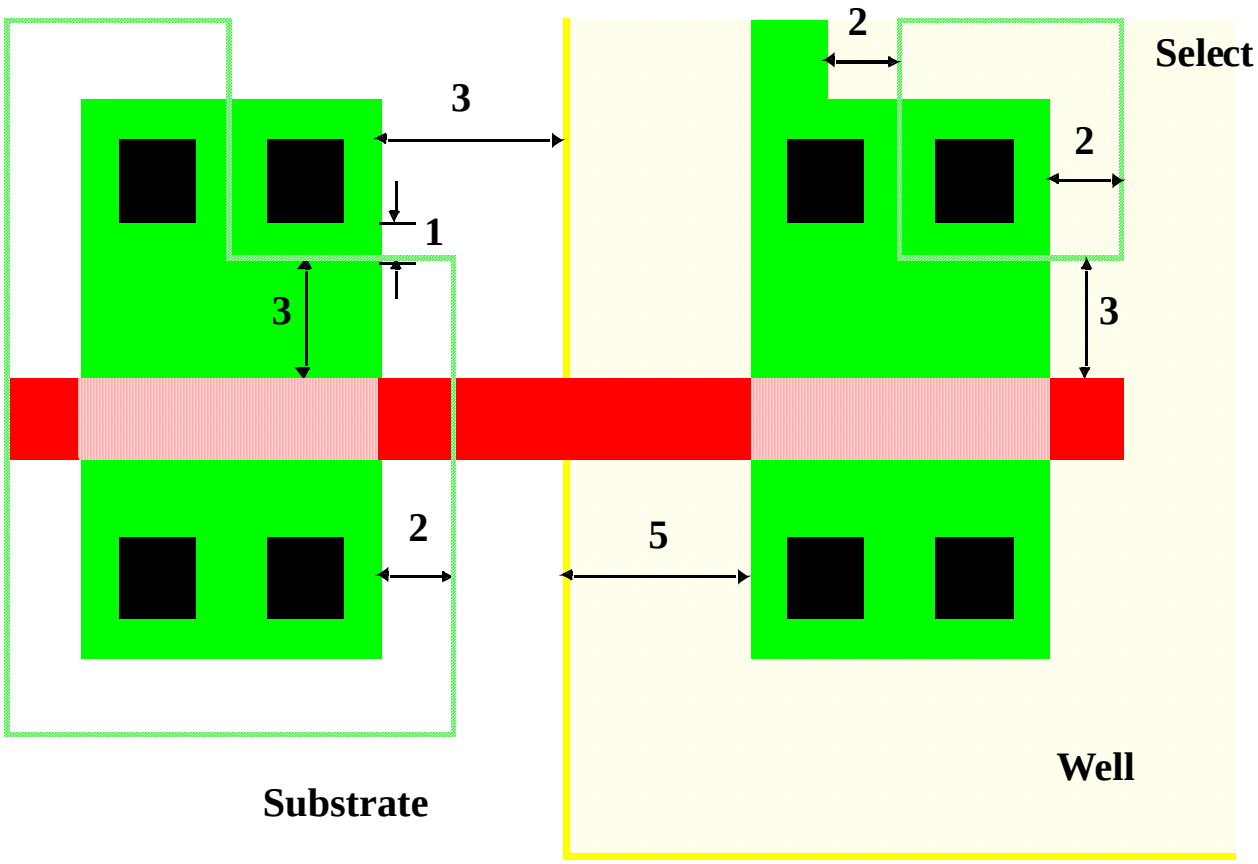






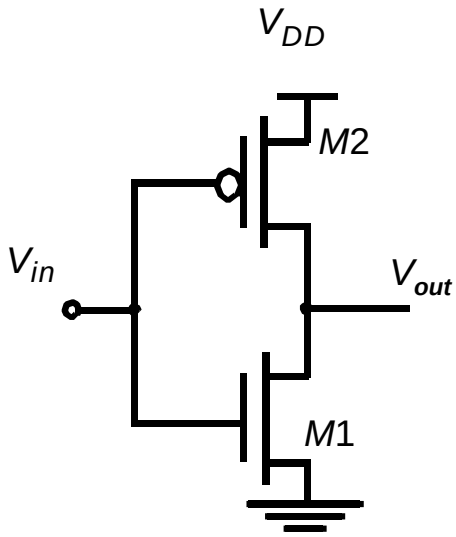
DESIGN RULES AND LAYOUT

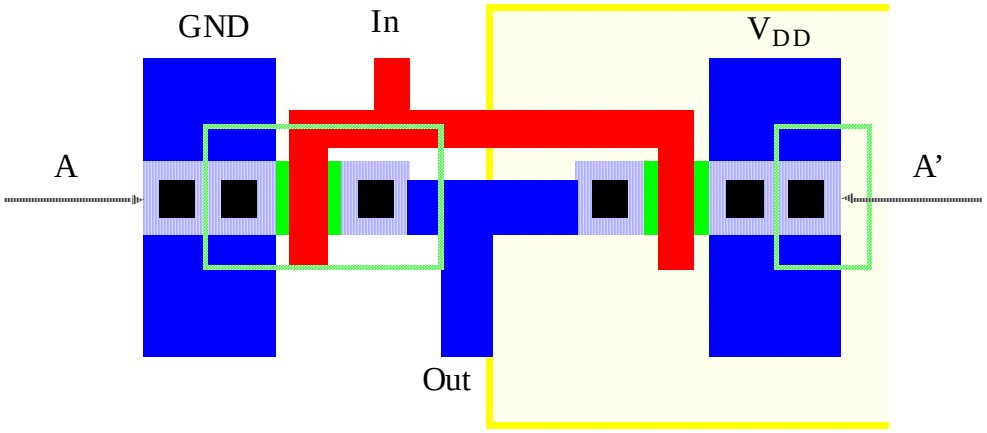
Select Layer



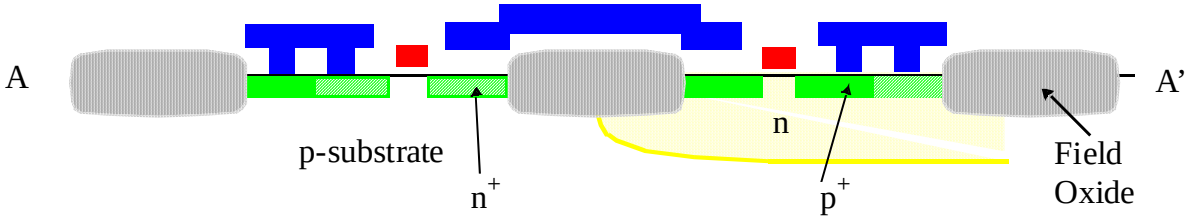
DESIGN RULES AND LAYOUT

CMOS Inverter Layout





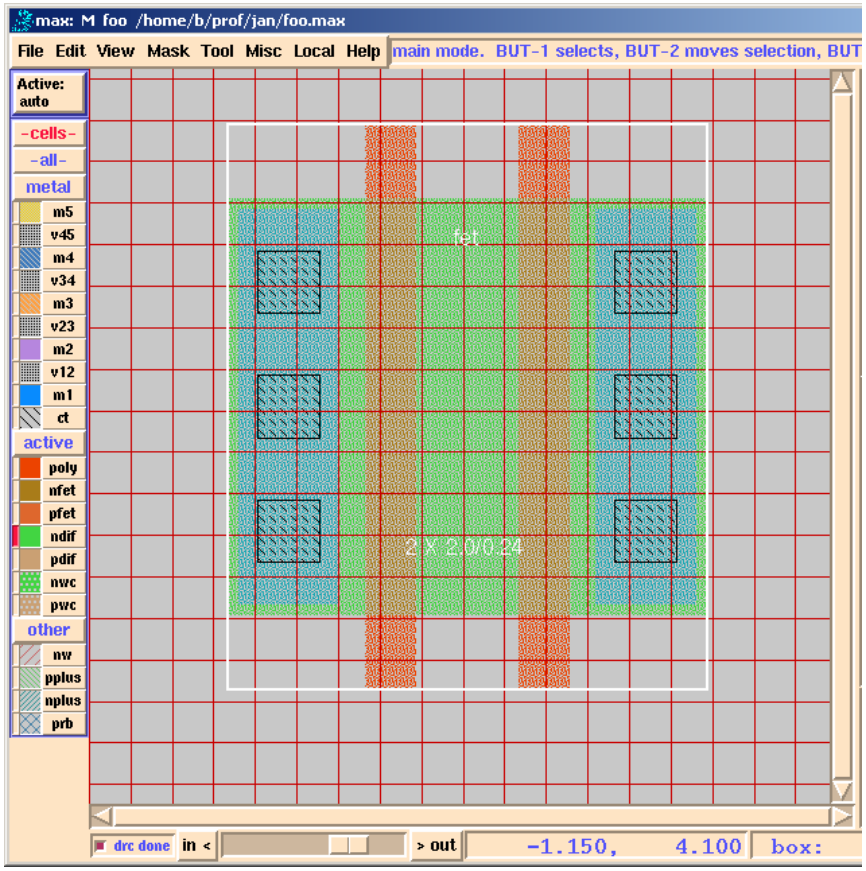
(a) Layout



(b) Cross-Section along A-A'

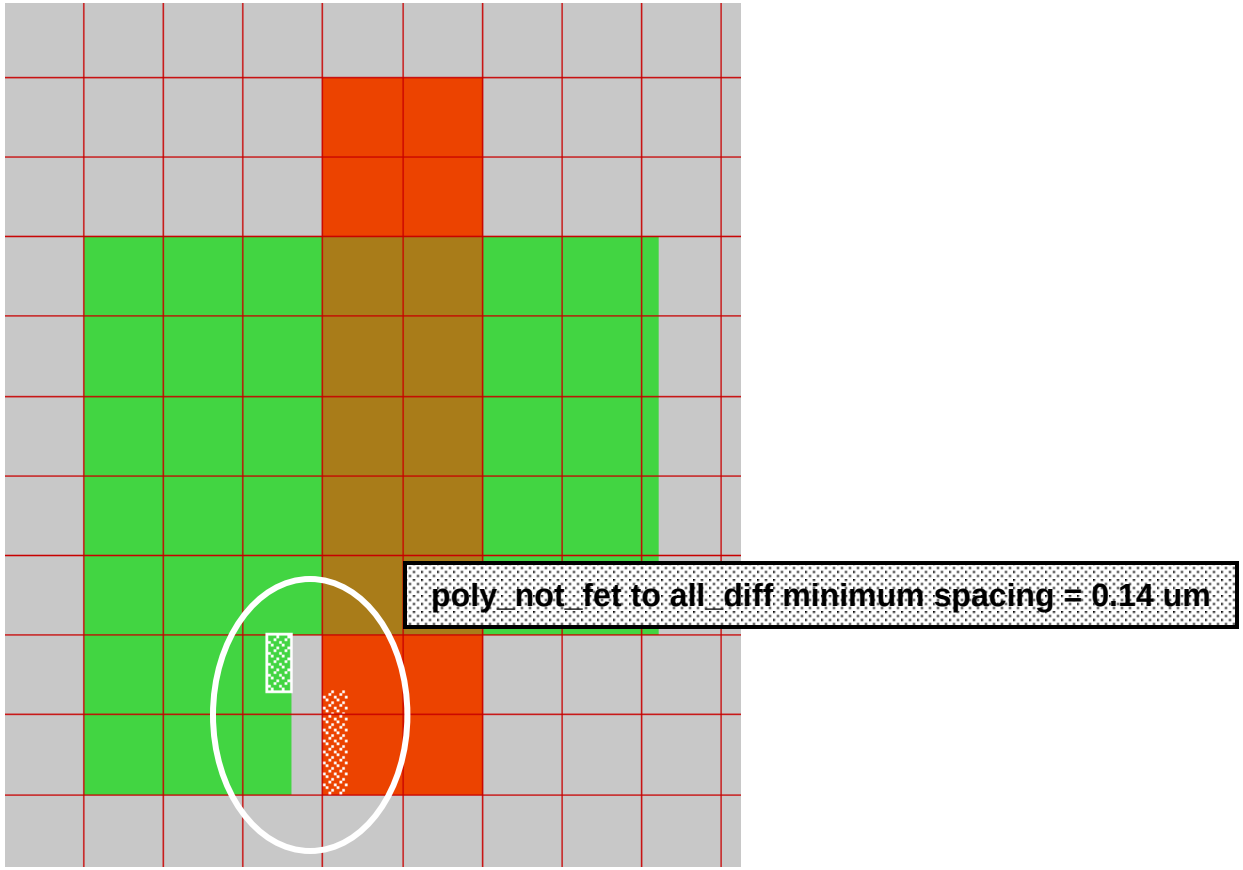
DESIGN RULES AND LAYOUT

Layout Editor

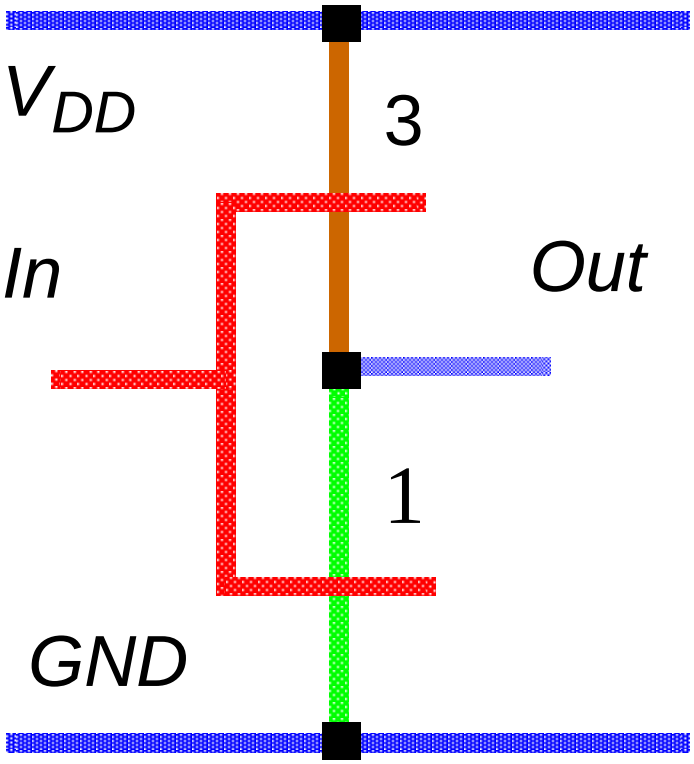


DESIGN RULES AND LAYOUT

Design Rule Checker



Stick Diagrams



Stick diagram of an inverter

- Dimensionless layout entities
- Only topology is important
- Final layout generated by "compaction" program (if available)