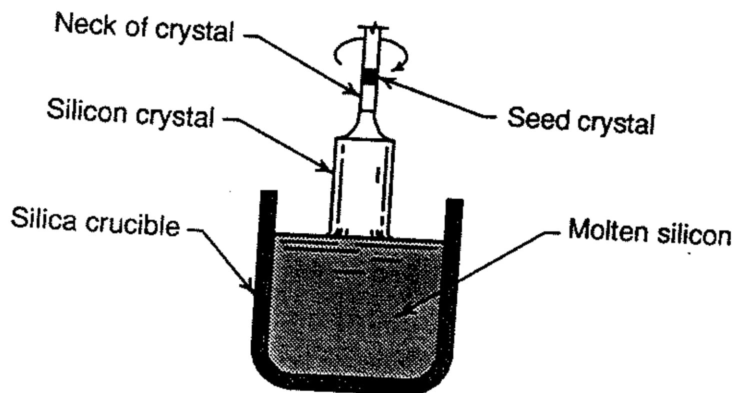
Wafer Manufacture



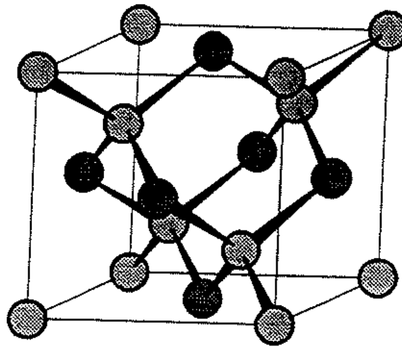
Czochralski process for growing silicon crystals.

- Production of semiconductor-grade polysilicon.
  - Crude, or metallurgical-grade silicon, is produced by reduction of silicon dioxide by carbon in an electric arc furnace.
  - The crude silicon is converted into a volatile compound, such as trichlorosilane, which is purified by fractional distillation.
  - The purified trichlorosilane is reduced to semiconductor-grade silicon using hydrogen.

- Production of a single-crystal silicon ingot.
  - A crucible charged with chunks of polysilicon is heated until the silicon melts.
  - A seed crystal lowered into the melt provides a surface upon which silicon atoms crystallize. As the crystal grows it is slowly withdrawn from the crucible.
  - The doping of the silicon crystal, or *ingot,* is adjusted by adding small amounts of doped polysilicon to the crucible.

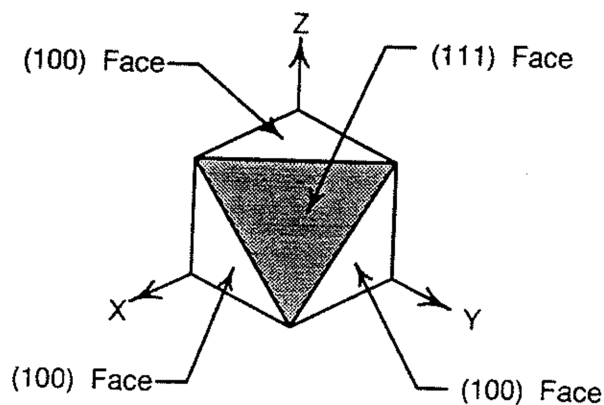
- Production of wafers.
  - The ingot is ground to form a cylinder. The crystal orientation is denoted by grinding a flat down the side of this cylinder.
  - The ingot is sliced using a diamond saw and the sections are polished upon one surface to form wafers.

The Crystal Structure of Silicon

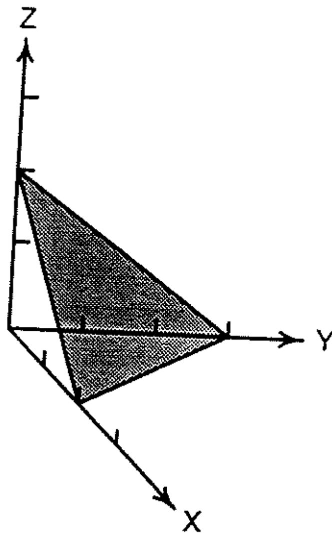


The diamond-lattice unit cell.

- Silicon crystals display a face-centered-cubic structure similar to that of diamond, consisting of repetitions of the unit cell pictured above.
  - The properties of a monocrystalline silicon surface depend upon the orientation of the surface to the unit cell.
  - Every plane surface which intersects the cubic unit cell can be described by a trio of numbers, known as *Miller indices.*
  - The two most important cuts through the unit cell correspond to the Miller indices (100) and (111), which are identified below:



Computing Miller Indices



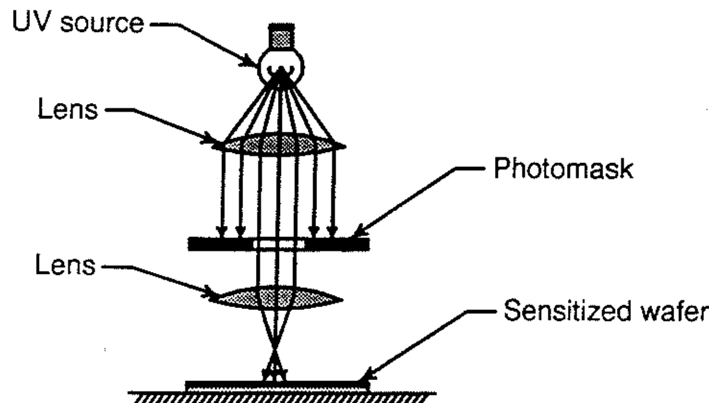
A plane with Miller indices (323).

- The following method allows computation of Miller indices for the cubic crystal system:
  - Extend the plane until it intersects the X,Y and Z axes.
  - Move the plane away from, or toward, the origin until the X,Y and Z-intercepts lie at integer multiples of the dimensions of the unit cell. In the above example, the intercepts are X=2, Y=3, Z=2.
  - Take the reciprocal of the intercepts. In the above example, these are (1/2, 1/3, 1/2).
  - Multiply the reciprocals by the smallest integer which will result in a trio of integers. In the above example, multiply by 6 to obtain (3,2,3).
  - Place the resulting triplet of numbers between parentheses to form the Miller indices: (323).

- Planes formed by permuting the Miller indices have the same properties, for example (100), (010) and (001).

- The vector normal to the plane (XYZ) is denoted [XYZ].

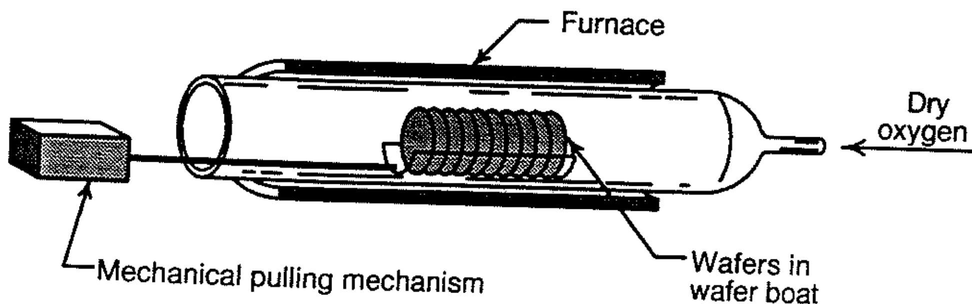
Photolithography



Simplified diagram of projection printing.

- *Photolithography* is a photographic process which can transfer an image to a wafer, allowing the selective removal or deposition of a material.
  - A thin film of photosensitive emulsion called *photoresist* is applied to the wafer.
  - The sensitized wafer is baked to drive off solvents and harden the photoresist for handling.
  - A *positive photoresist* chemically decomposes under UV light, so exposed areas wash away in a suitable solvent (the developer).
  - A *negative photoresist* polymerizes under UV light, so unexposed areas wash away in the developer.
  - Negative resists tend to swell during development, so most processes now employ positive resists.
- Formation of an image upon the photoresist requires the use of a patterned transparent plate called a *photomask.*
  - Modern processes often photoreduce the image by a factor of five or ten to help sharpen the image. The enlarged photomask is often called a reticle.
  - Because the size of the reticle is limited, multiple exposures are required to pattern the entire wafer. This process is called direct-step-on-wafer, or DSW.
  - The exposure process uses a machine called a stepper which repeatedly projects a photoreduced image of the reticle upon the wafer.

Oxidation



Simplified diagram of an oxidation furnace.

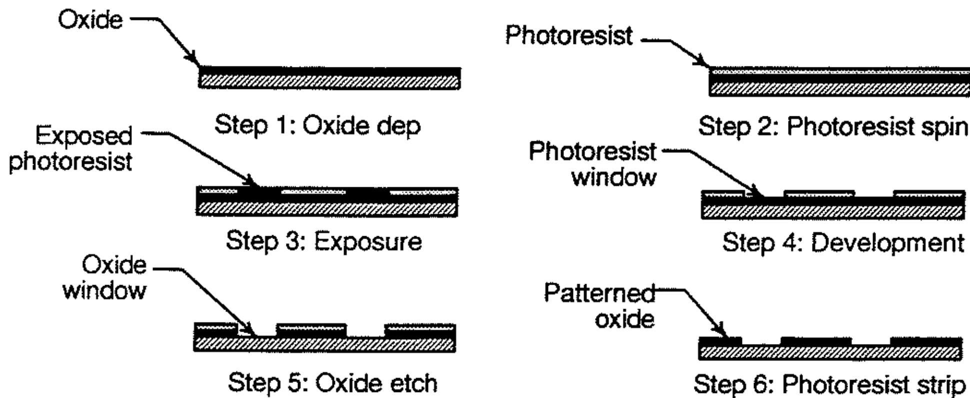
- Properties of silicon dioxide (oxide):
  - Can readily be formed in films as thin as 10-20Å.
  - Adheres tightly to silicon.
  - Resists attack by most chemicals, including dopants.
  - Easily dissolved using buffered hydrofluoric acid (HF).
  - Excellent dielectric for capacitors and MOS transistors.
  - Extremely low stress between oxide and (100) silicon produces very low surface state concentration.

- Oxide is grown by heating the wafers in an oxidizing atmosphere.
  - Pure dry oxygen will produce a slow-growing oxide with minimal surface defects (dry oxide).
  - Oxygen saturated with water vapor will produce a fast-growing oxide with many more surface defects (wet oxide). These defects can be partially eliminated by following a wet oxidation by a brief period of dry oxidation.

Times required to grow 0.1μm (1000Å) of oxide on (111) silicon.

Ambient	800°C	900°C	1000°C	1100°C	1200°C
Dry O_2	30 hr	6 hr	1.7 hr	40 min	15 min
Wet O_2	1.7 hr	20 min	6 min		

Oxide Removal



Steps in oxide growth and removal.

- Since photoresists cannot withstand high temperatures, a patterned oxide film is often used to selectively block dopants during high-temperature diffusion. A patterned oxide is formed as follows:

Step 1: A uniform thin film of oxide is thermally grown across the wafer.

Step 2: A photoresist is spun onto the wafer and baked to drive out solvents.

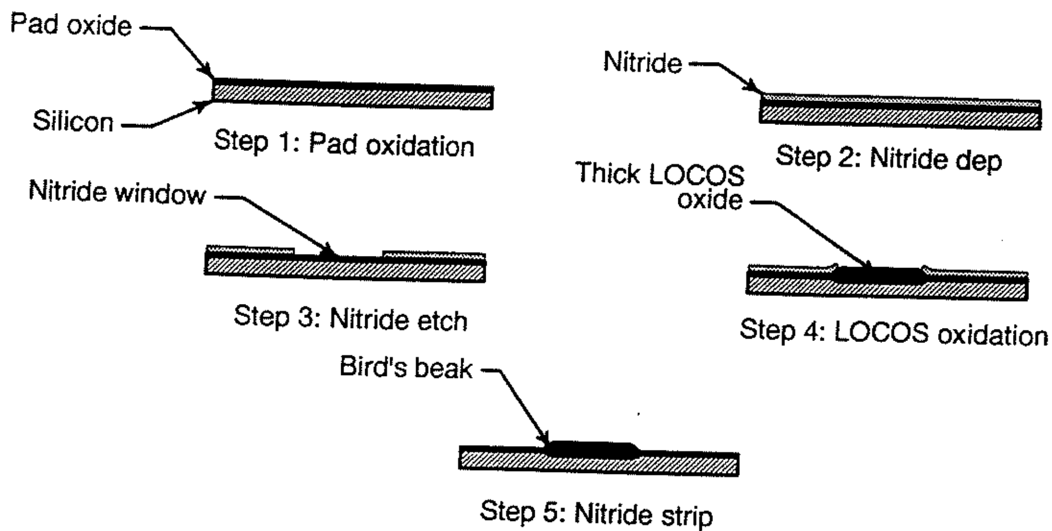
Step 3: The photoresist is exposed using a suitable photomask.

Step 4: The photoresist is developed, exposing the oxide in the bottom of the photoresist windows..

Step 5: The exposed oxide is etched using buffered HF.

Step 6: The photoresist is stripped off the wafer, leaving the patterned oxide layer.

LOCOS



Steps in LOCOS processing.

- Oxide can be selectively grown through a technique called local oxidation of silicon (LOCOS). The steps in this process are as follows:

  Step 1: A thin layer of oxide (the pad oxide) is grown across the wafer to protect the silicon from stresses induced by nitride growth.

  Step 2: A layer of low-pressure chemical vapor deposited (LPCVD) nitride is grown to act as an oxidation mask.

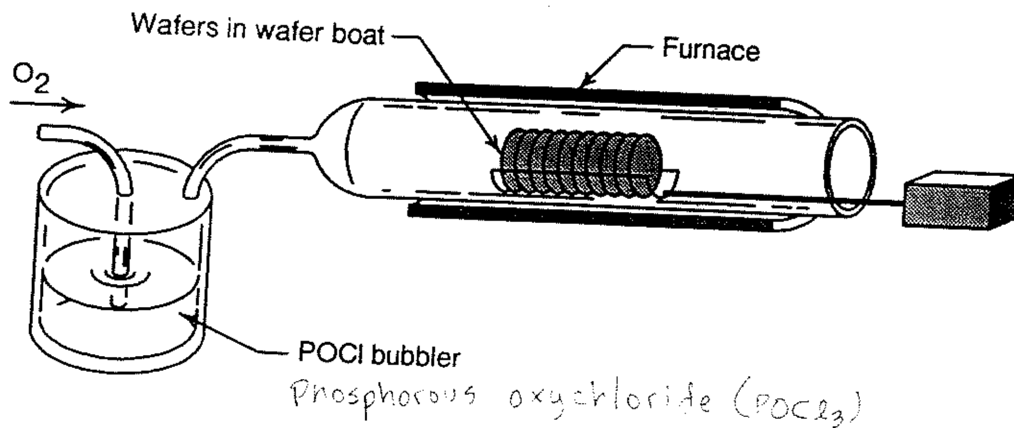
  Step 3: Photoresist is applied, patterned and developed. A nitride etch removes nitride in the photoresist windows, after which the remaining photoresist is stripped.

  Step 4: A thick oxide is grown in the nitride windows. The nitride film protects other areas of the silicon from oxidation.

  Step 5: The nitride is stripped to reveal the LOCOS oxide.

- Some oxidation occurs under the edges of the nitride mask, causing a curved transition region called a *bird's beak* about the edge of each thick LOCOS oxide region.

Diffusion



Simplified diagram of a diffusion furnace using a POCl source.

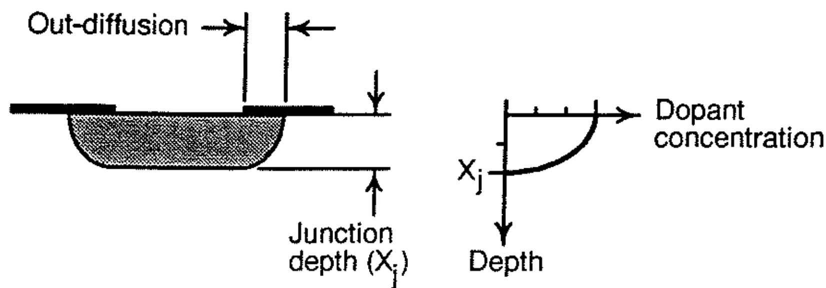
- Dopants become mobile and diffuse through silicon at sufficiently high temperatures.
  - Diffusion of dopants from an external source through a patterned oxide allows selective doping of specific regions of silicon (called *diffusions*).
  - In order to conduct a diffusion, an external source of dopant atoms must be brought in contact with the heated wafer so that some can diffuse into the silicon. This operation is called a *deposition.*
  - Following deposition, the wafers are removed from the furnace and the doped surface oxide is stripped. The wafers are then heated for a prolonged period to drive the dopants deeper into the silicon. This operation is called a *drive.*

- Dopants diffuse at different rates; boron and phosphorus move much faster than arsenic or antimony. All dopants diffuse more rapidly at higher temperatures.

Representative junction depths, in microns
(10^{20} cm^{-3} source, 10^{16} cm^{-3} background, 15min deposition, 1hr drive).

Dopant	950°C	1000°C	1100°C	1200°C
Boron	0.9	1.5	3.6	7.3
Phosphorus		0.5	1.6	4.6
Antimony			0.8	2.1
Arsenic			0.7	2.0

Diffusion *(continued)*

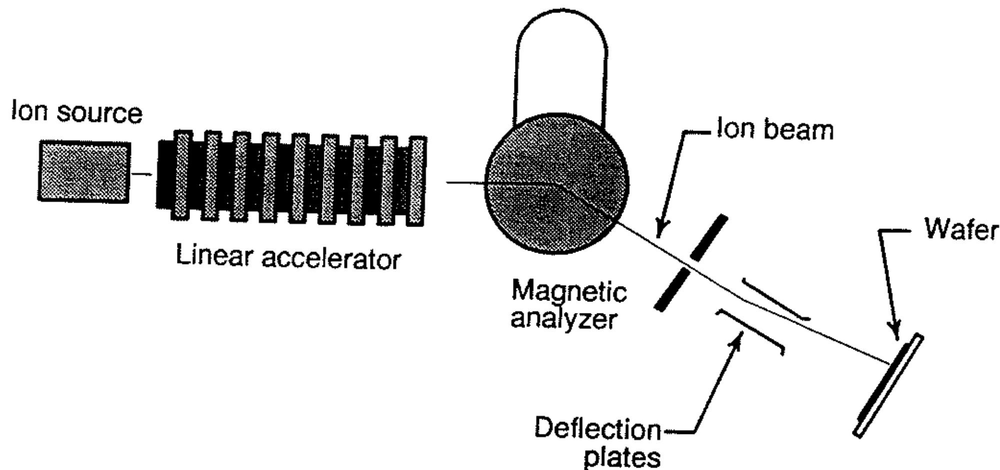


Cross-section and doping profile of a typical planar diffusion.

- A diffusion driven in from the surface of the wafer is called a *planar diffusion.*
  - Planar diffusions are usually patterned by means of oxide windows.
  - The dopants diffuse laterally underneath the edges of the oxide window about 80% of the junction depth x_j.
  - A planar diffusion is most concentrated at the surface and becomes less concentrated with depth.
  - The junction occurs at the point where the diffusion just counterdopes the background doping concentration.
  - Some dopant diffuses beyond the junction depth, but is insufficient to invert the polarity of the silicon.

- Multiple diffusions can be driven into one another to produce structures such as an NPN or a PNP transistor.

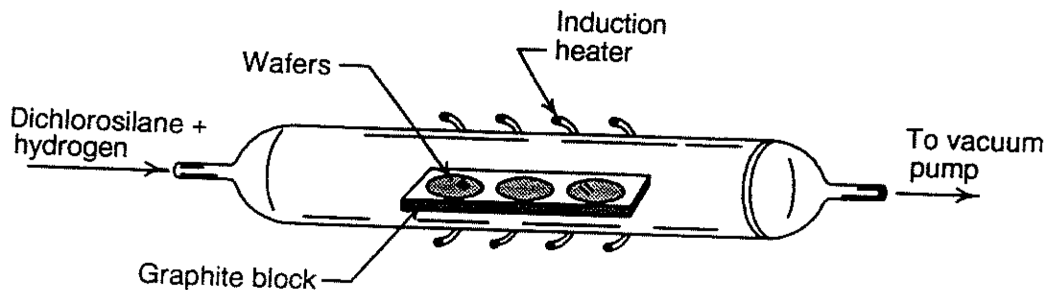
Ion Implantation



Simplified diagram of an ion implanter.

- An alternate method of doping silicon involves the use of a particle accelerator to drive dopant atoms into the silicon lattice.
  - Particle accelerators used in semiconductor manufacture are optimized for low acceleration energies (rarely more than 100kEv) and high beam currents (milliamps). Such machines are called *ion implanters.*
  - Implanted ions scatter from the silicon lattice as soon as they penetrate the surface. The ion beam spreads out and loses energy quickly, so most ion implantations are quite shallow.
  - The concentration of dopant atoms can be very precisely adjusted by properly selecting the total charge implanted (the *implant dose*) and the energy used to accelerate each atom (the *implant energy*).
  - Since ion implantation occurs at low temperatures, a layer of photoresist can mask the ion beam.
- Ion implantation damages the crystal structure of the silicon, requiring annealing.
  - High-velocity ions knock silicon atoms out of the lattice, and a sufficient dose will actually transform the silicon surface into an amorphous state.
  - If the implant-damaged silicon is heated, the silicon atoms will re-crystallize out using the remnants of the original lattice as seeds, a process called annealing.

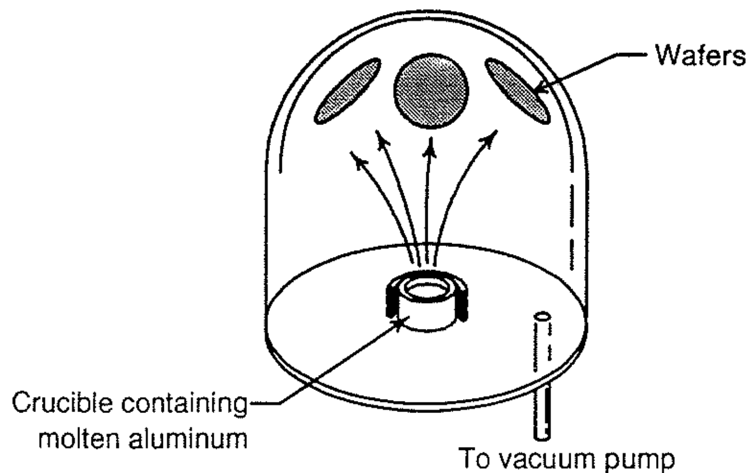
Vapor-phase Epitaxy



Simplified diagram of an epi reactor.

- A layer of monocrystalline silicon can be deposited upon a wafer through a process called *epitaxy*.
  - The most common form of epitaxy uses a low-pressure gas mixture as the source for the deposition. This type of epitaxy is called low-pressure chemical vapor deposited (LPCVD) epitaxy.
  - The chlorinated derivatives of silane (e.g, dichlorosilane) are the most common gaseous sources of silicon for epitaxy.
  - The crystal structure of an epitaxial layer exactly duplicates that of the underlying silicon. However, due to the extreme purity of the gaseous reactants and the tendency for defects to self-anneal, an epi layer is purer and more regularly ordered than its substrate.
  - Monocrystalline silicon can be epitaxially deposited upon sapphire or spinel because these materials have crystal structures similar to silicon.

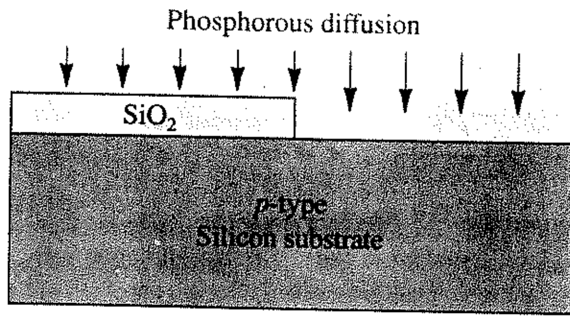
- LPCVD deposition of silicon upon an amorphous material such as oxide results in a polycrystalline aggregate.
  - Polycrystalline silicon (poly) is used to form MOS gate electrodes, resistors, capacitors, etc.



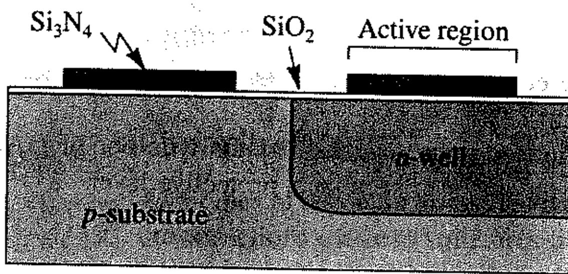
Simplified diagram of evaporation apparatus.

- Diffusions on a wafer are interconnected by opening oxide windows (contacts) and depositing a patterned layer of metal leads.
  - Aluminum is most often used because it is highly conductive and it adheres well to both oxide and silicon. The aluminum film can be deposited either by *evaporation* or by *sputtering*.

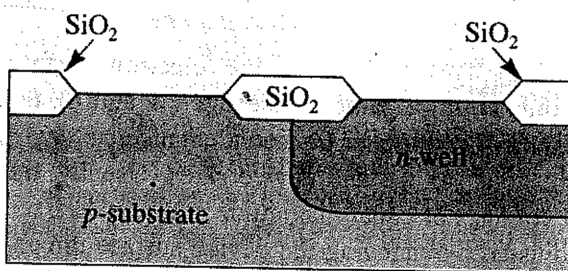
- Pure aluminum has a number of drawbacks.
  - Pure aluminum is relatively vulnerable to a long-term failure mechanism called electromigration. The addition of 0.5-2% of copper to the aluminum greatly reduces this vulnerability.
  - Pure aluminum alloys with silicon during contact sintering. Considerable silicon dissolves in the aluminum, causing erosion of the silicon surface. This can be controlled by the addition of 1-2% of silicon to the aluminum alloy.
  - Aluminum deposits anisotropically, leading to poor coverage of steep sidewalls. Certain refractory metals (such as titanium and tungsten) can be isotropically sputtered. These metals also display exceptional immunity to electromigration, but they are much more resistive than aluminum.
  - Many modern metal systems consist of a two-layer sandwich. The lower layer of refractory barrier metal (RBM) prevents overalloying of silicon with aluminum and increases step coverage. The upper layer of copper-doped aluminum provides a low-resistance conductor.



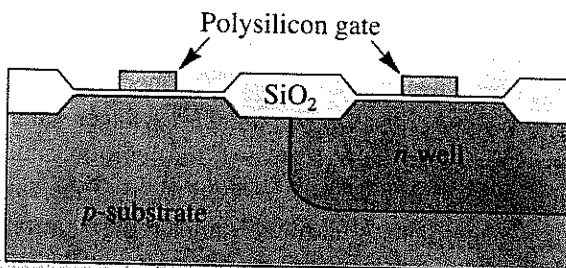
(a) Define n-well diffusion (mask 1)



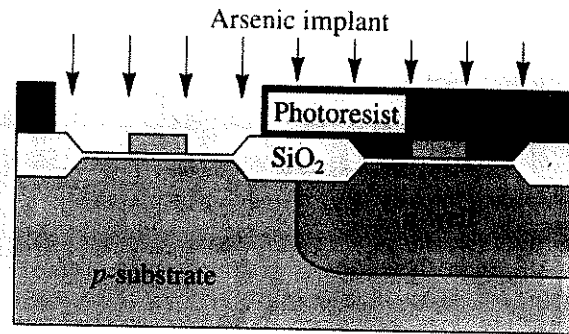
(b) Define active regions (mask 2)



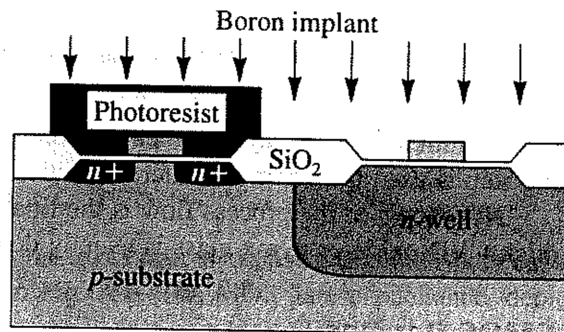
(c) LOCOS oxidation



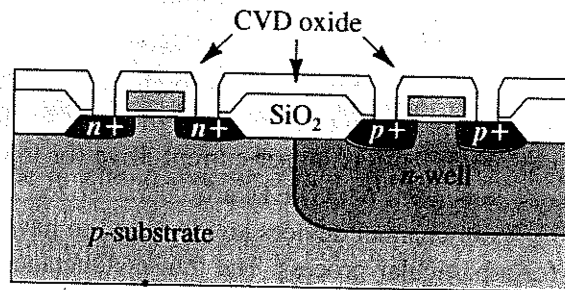
(d) Polysilicon gate (mask 3)



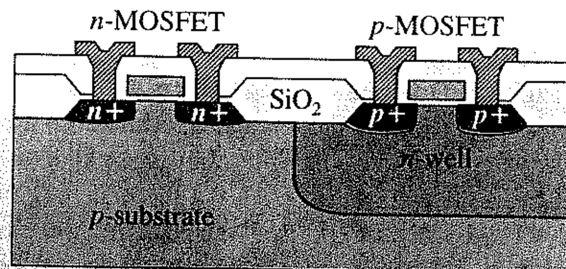
(e) $n+$ diffusion (mask 4)



(f) $p+$ diffusion (mask 5)



(g) Contact holes (mask 6)



(h) Metallization (mask 7)

Fig. A.3 A typical n-well CMOS process flow.