SEQUENTIAL LOGIC

INEL 4076 - Spring 2013

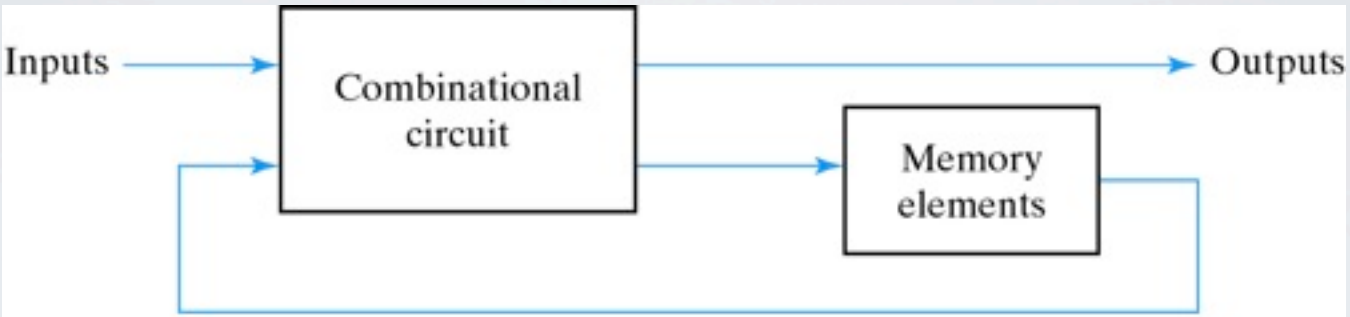
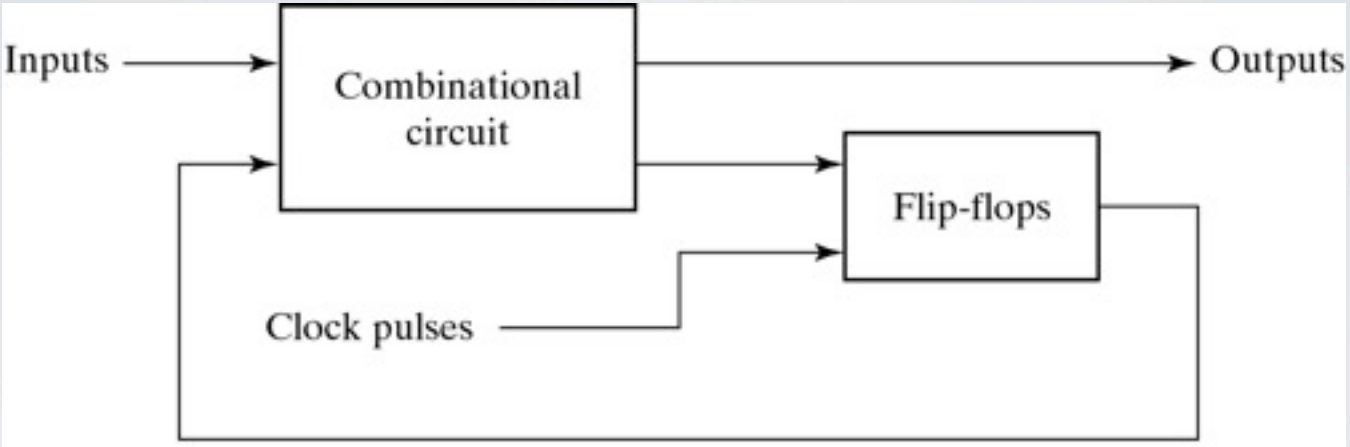


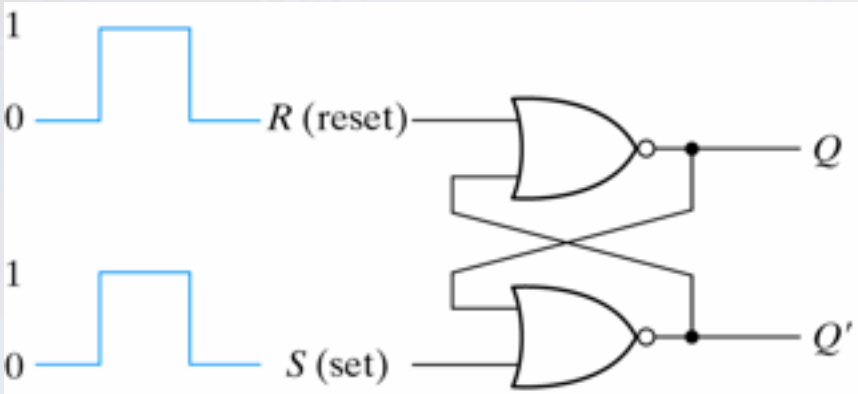
Fig. 5-1 Block Diagram of Sequential Circuit



(a) Block diagram

(b) Timing diagram of clock pulses

Fig. 5-2 Synchronous Clocked Sequential Circuit

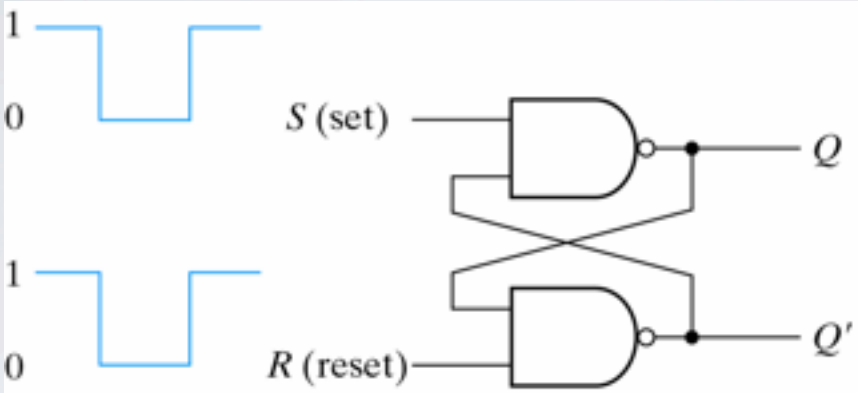


(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

(b) Function table

Fig. 5-3 *SR* Latch with NOR Gates

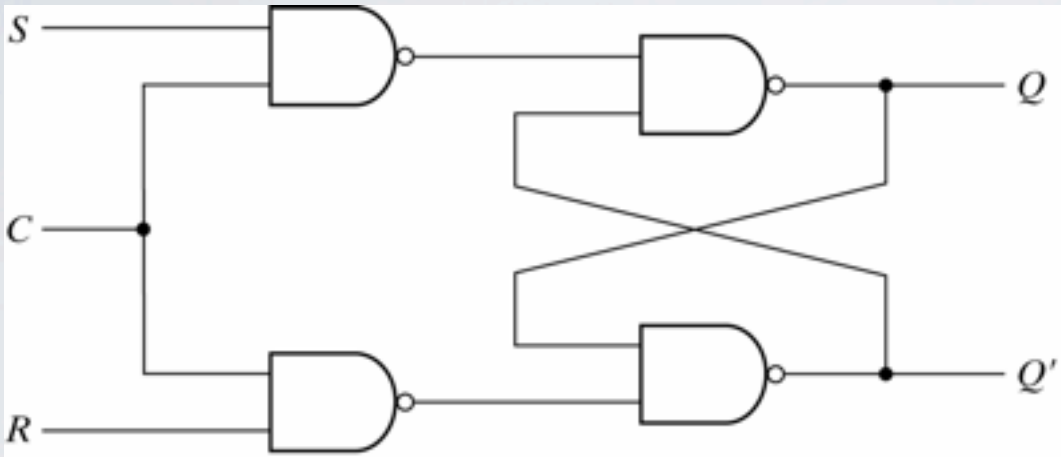


(a) Logic diagram

S	R	Q	Q'	
1	0	0	1	
1	1	0	1	(after $S = 1, R = 0$)
0	1	1	0	
1	1	1	0	(after $S = 0, R = 1$)
0	0	1	1	

(b) Function table

Fig. 5-4 *SR* Latch with NAND Gates

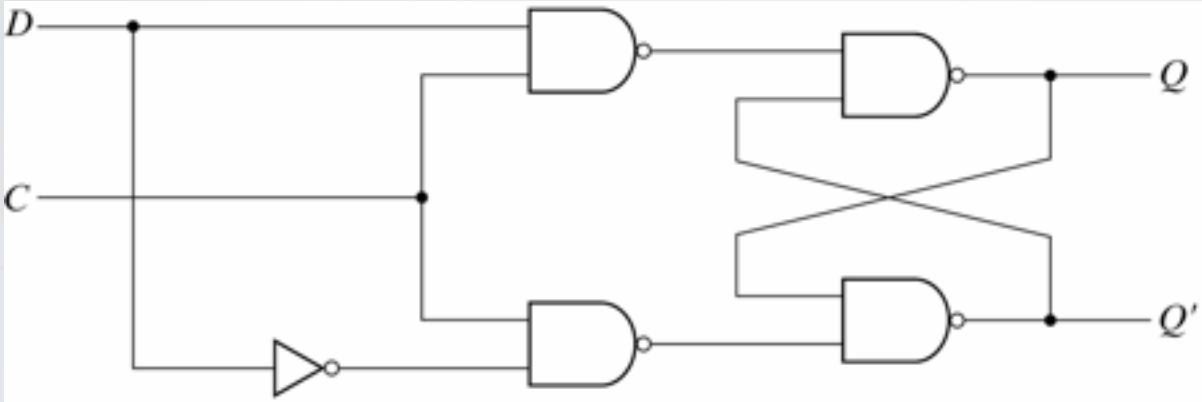


(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

(b) Function table

Fig. 5-5 SR Latch with Control Input



(a) Logic diagram

C	D	Next state of Q
0	X	No change
1	0	$Q = 0$; Reset state
1	1	$Q = 1$; Set state

(b) Function table

Fig. 5-6 D Latch

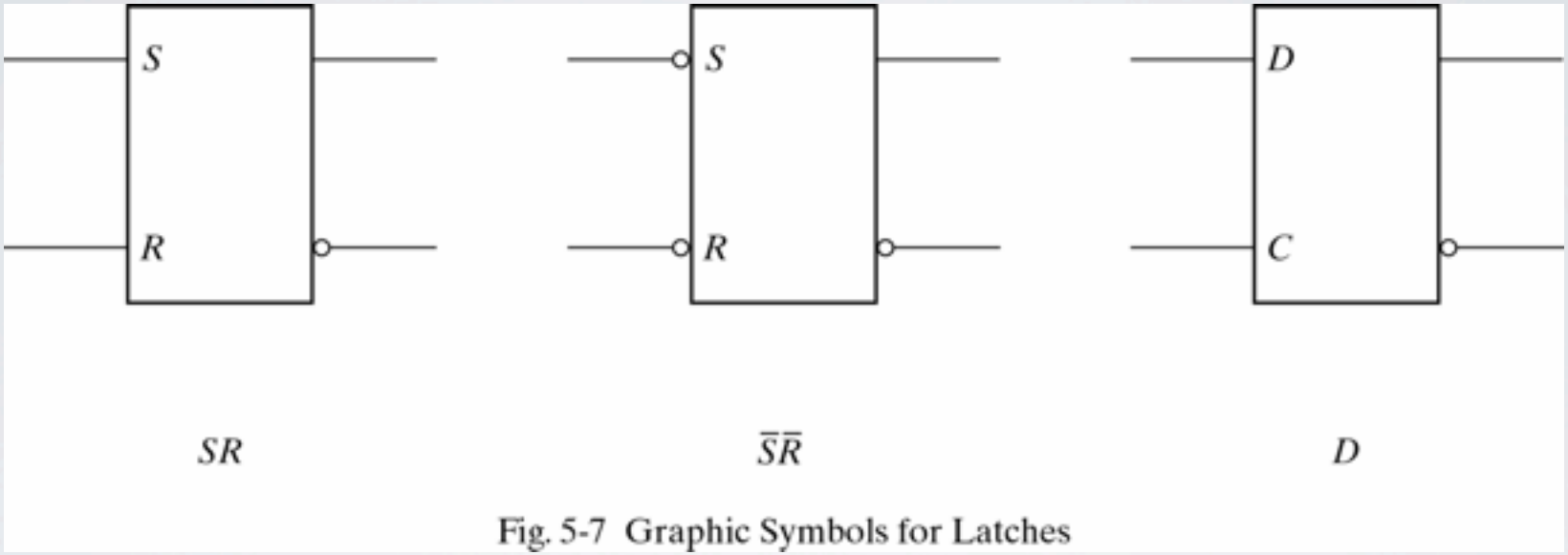


Fig. 5-7 Graphic Symbols for Latches

(a) Response to positive level

(b) Positive-edge response

(c) Negative-edge response

Fig. 5-8 Clock Response in Latch and Flip-Flop

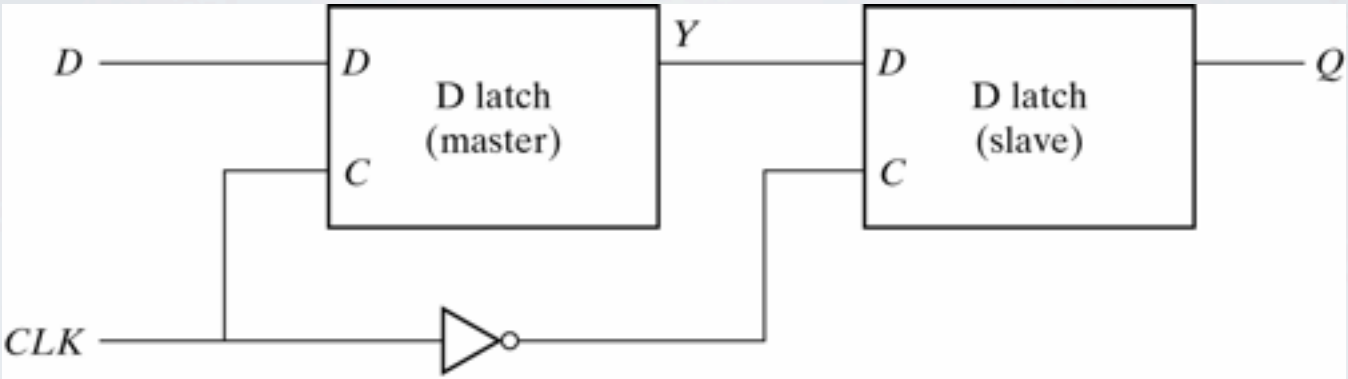


Fig. 5-9 Master-Slave *D* Flip-Flop

(a) Positive-edge (a) Negative-edge

Fig. 5-11 Graphic Symbol for Edge-Triggered *D* Flip-Flop

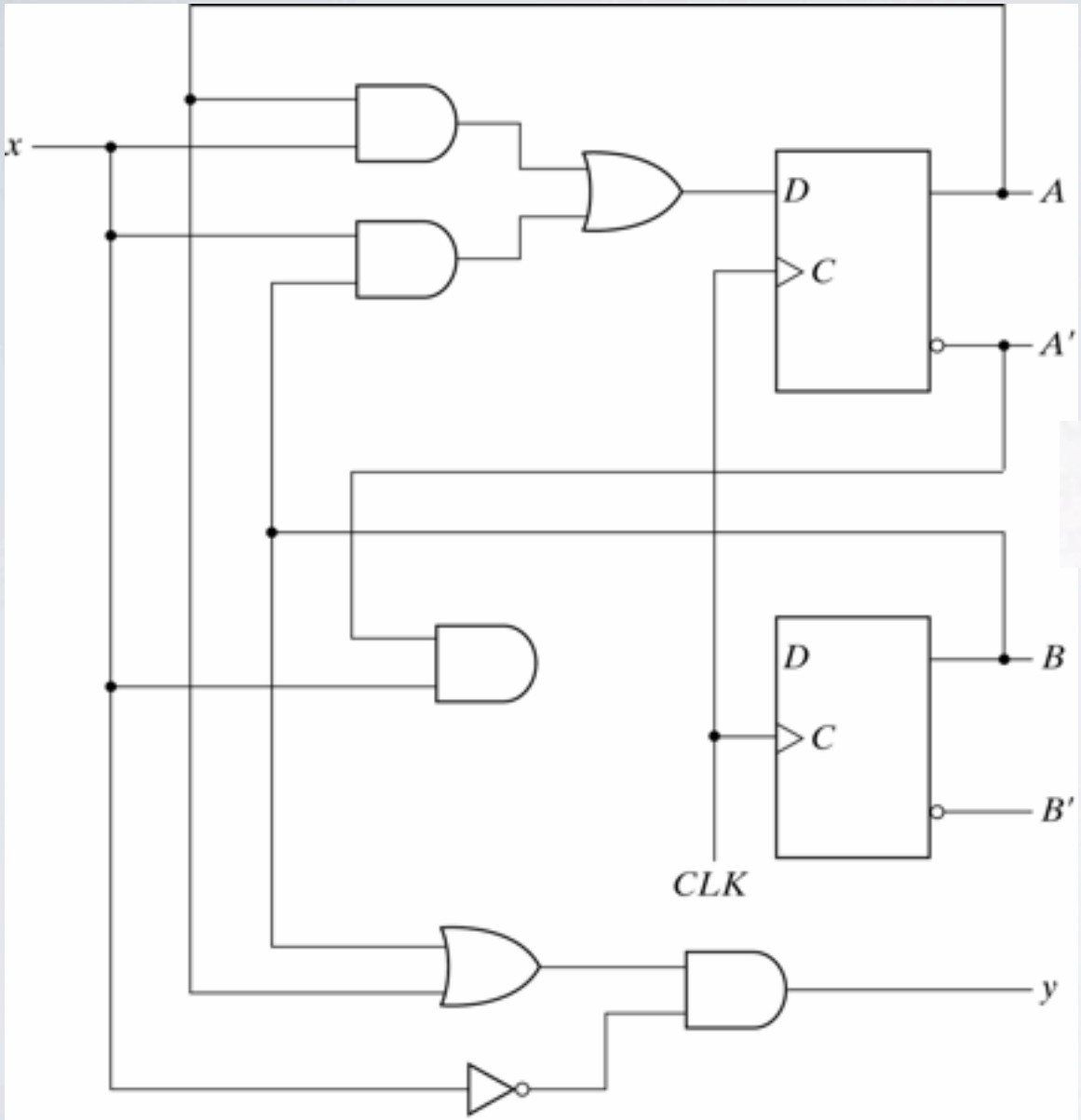


Fig. 5-15 Example of Sequential Circuit

$$A(t+1) = Ax + Bx$$
$$B(t+1) = A'x$$

$$y = (A + B)x'$$

$$A(t+1) = Ax + Bx$$
$$B(t+1) = A'x$$

State equations or transition equations

$$y = (A + B)x'$$

Output boolean equation

Table 5-2
State Table for the Circuit of Fig. 5-15

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Table 5-3
Second Form of the State Table

Present State	Next State		Output	
	x = 0	x = 1	x = 0	x = 1
AB	AB	AB	y	y
00	00	01	0	0
01	00	11	1	0
10	00	10	1	0
11	00	10	1	0

/0 represents the output during the present state with the given input

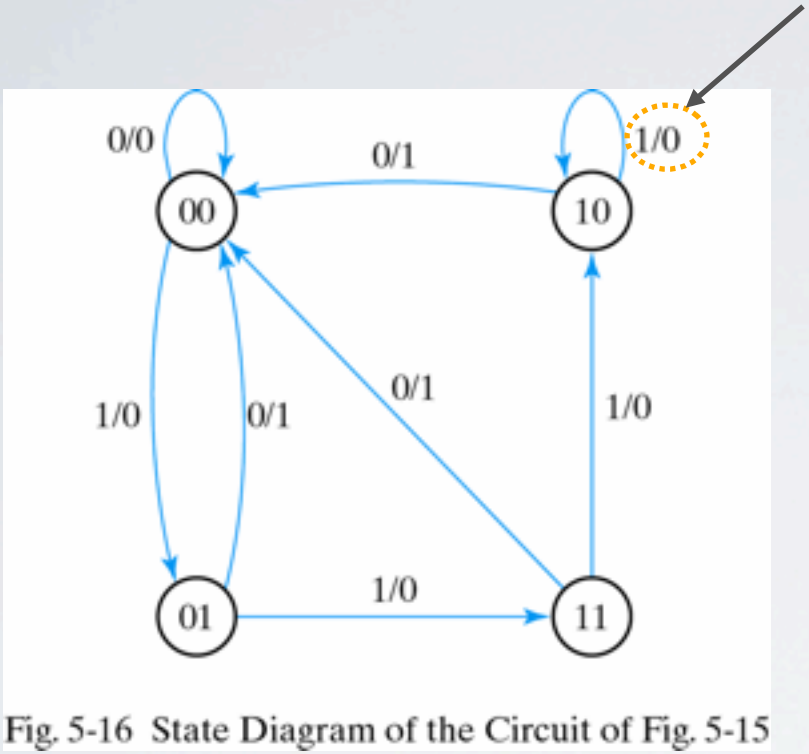
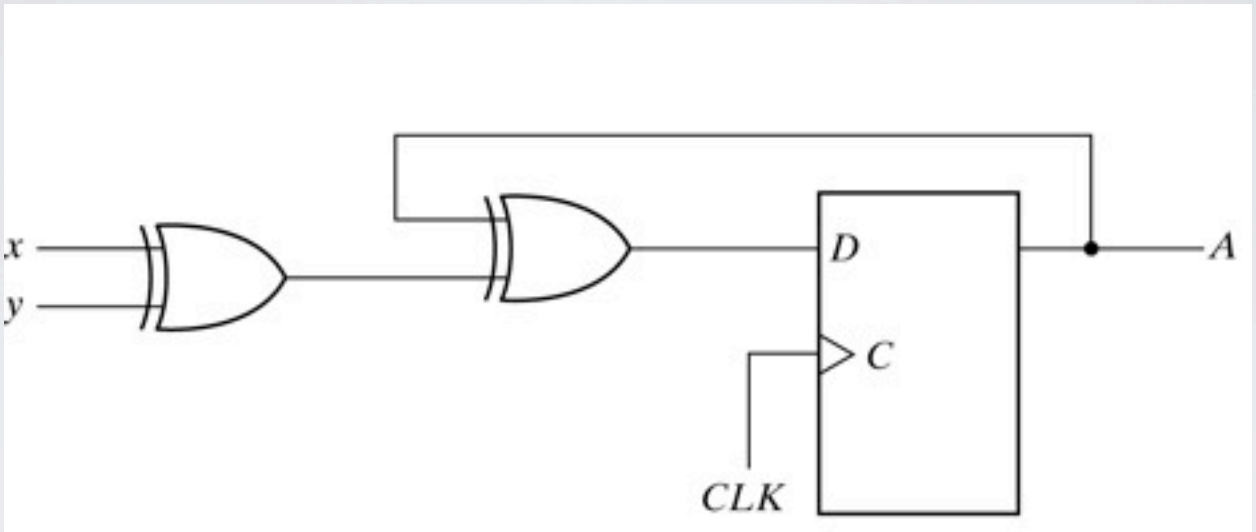


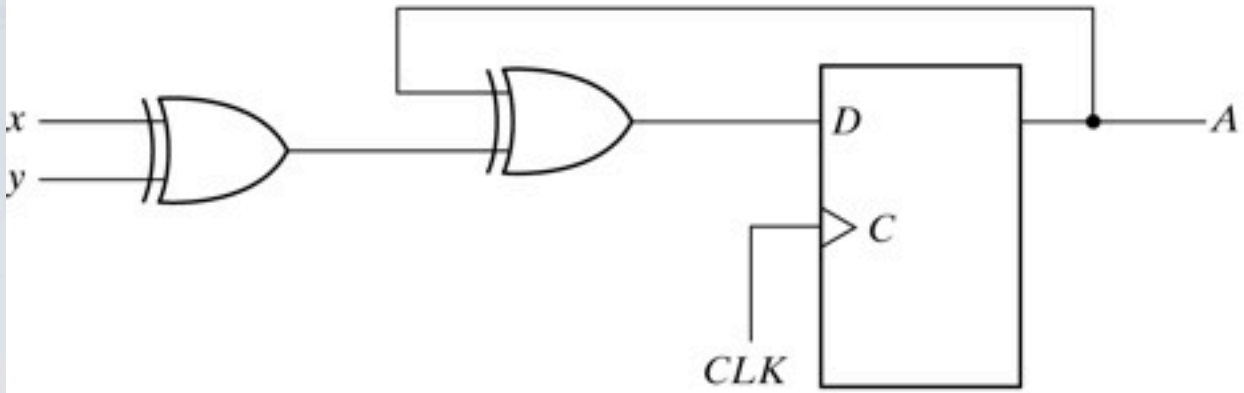
Fig. 5-16 State Diagram of the Circuit of Fig. 5-15

Mealy Finite State Machine (FSM) – output is a function of present state and input

Example:



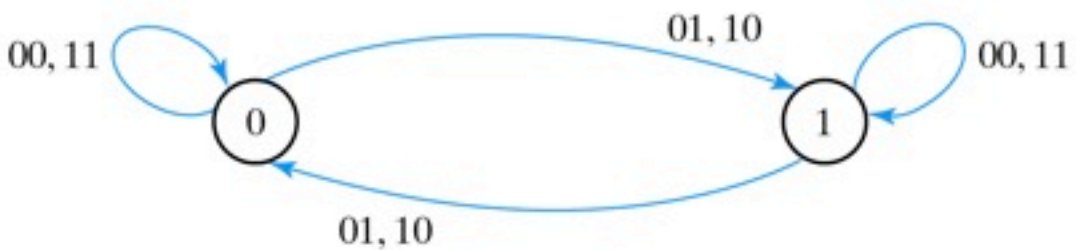
1. Find the state table
2. Draw the state diagram



(a) Circuit diagram

Present state	Inputs		Next state
A	*x*	*y*	*A*
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b) State table



(c) State diagram

Fig. 5-17 Sequential Circuit with *D* Flip-Flop

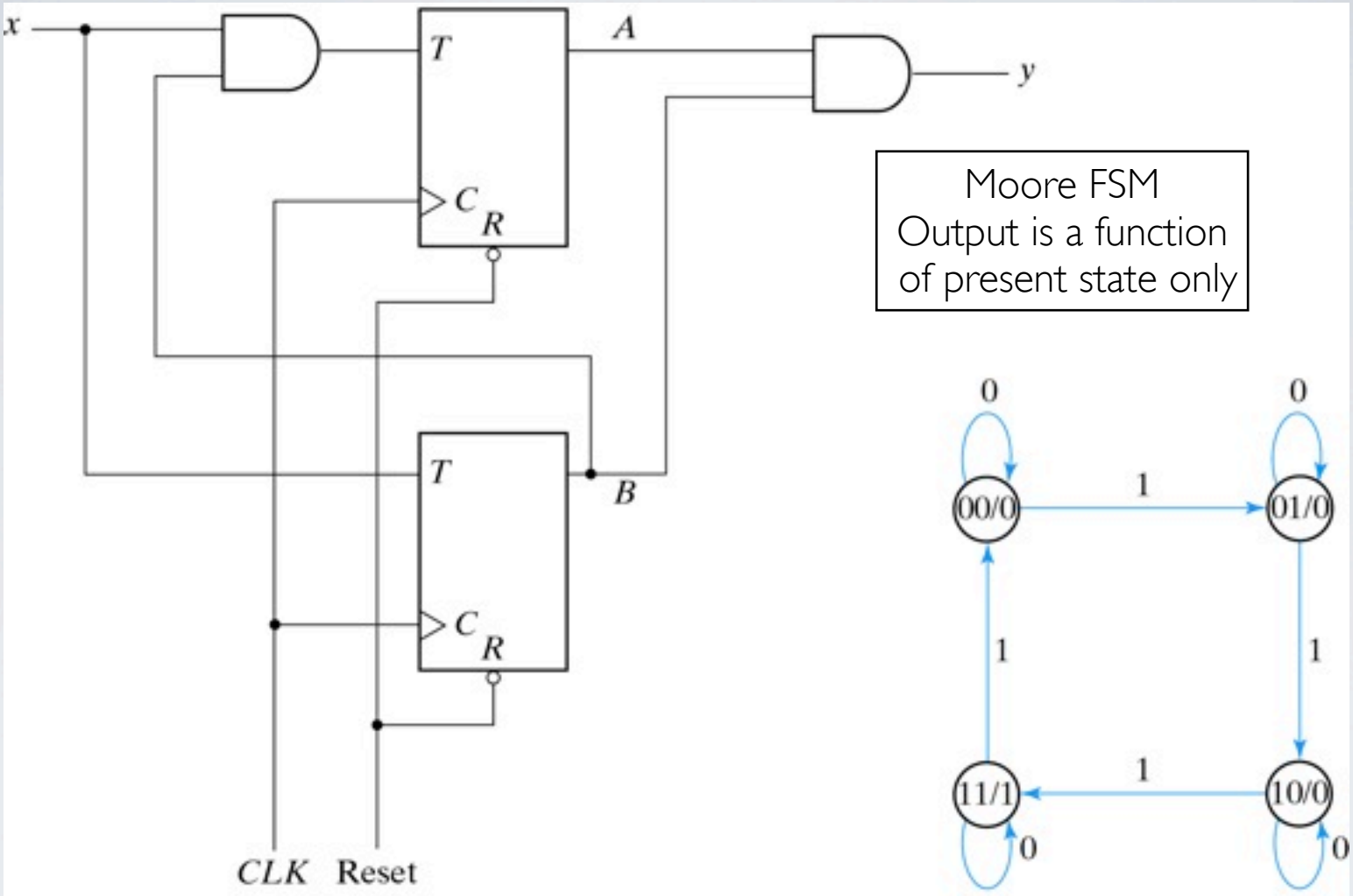
5-6 A sequential circuit with two D flip-flops, A and B; two inputs, x and y; and one output, z, is specified by the following next-state and output equations:

$$A(t+1) = x'y + xA$$
$$B(t+1) = x'B + xA$$
$$z = B$$

(a) Draw the logic diagram of the circuit.

(b) List the state table for the sequential circuit.

(c) Draw the corresponding state diagram.



(a) Circuit diagram

(b) State diagram

Fig. 5-20 Sequential Circuit with *T* Flip-Flops

Design Procedure

1. From the word description and specifications of the desired operation, derive a state diagram for the circuit.
2. Reduce the number of states if necessary.
3. Assign binary values to the states.
4. Obtain the binary-coded state table.
5. Choose the type of flip-flops to be used.
6. Derive the simplified flip-flop input equations and output equations.
7. Draw the logic diagram.

Sequence detector: circuit that detects 3 consecutive 1's in a string of bits coming through the input line

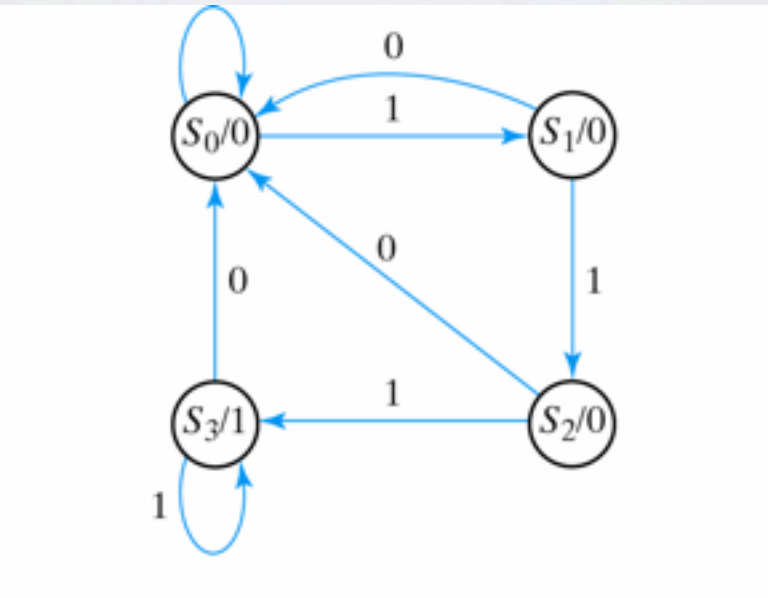


Fig. 5-24 State Diagram for Sequence Detector

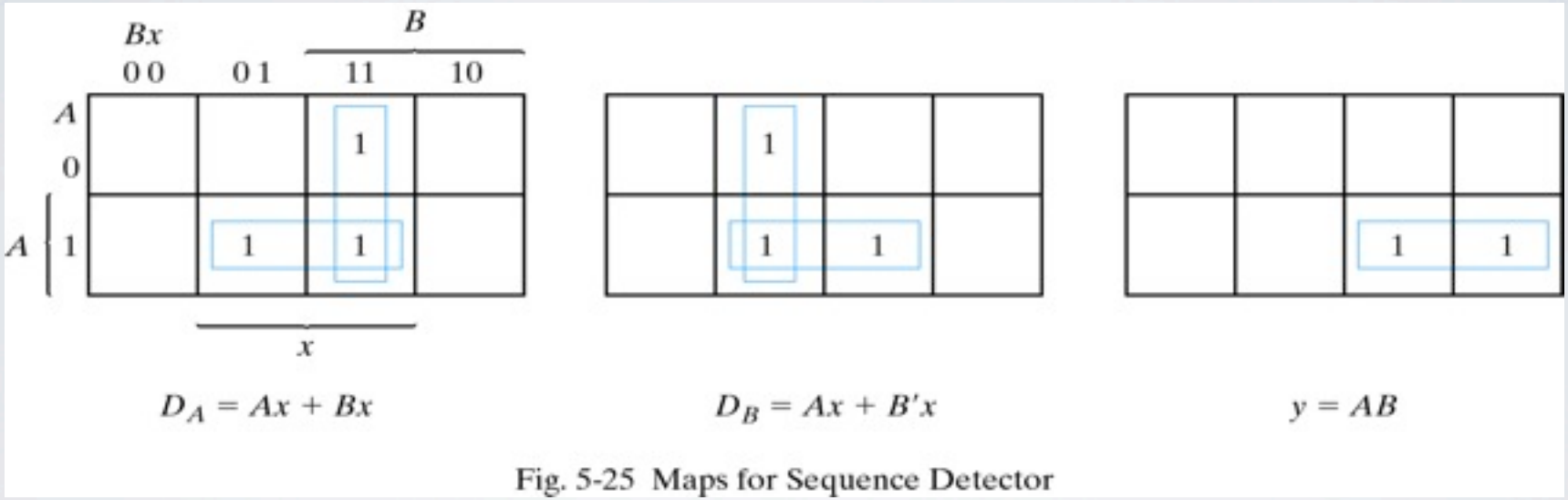


Fig. 5-25 Maps for Sequence Detector

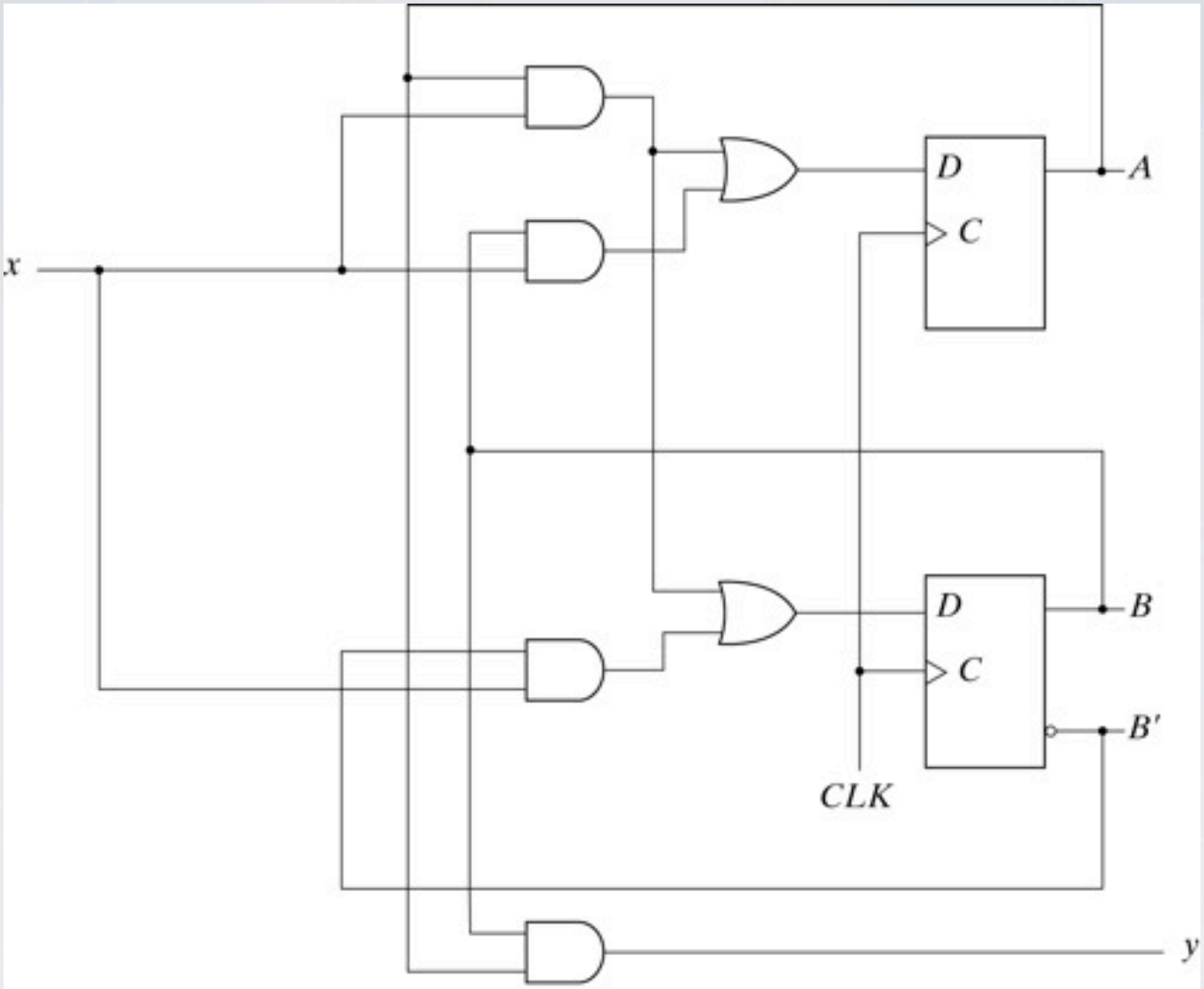


Fig. 5-26 Logic Diagram of Sequence Detector

5-19 A sequential circuit has three flip-flops A, B, C; one input x; and one output y. The state diagram is shown in Fig. P5-19. The circuit is to be designed by treating the unused states as don't-care conditions. Analyze the circuit obtained from the design to determine the effect of the unused states.

Use D flip-flops in the design.

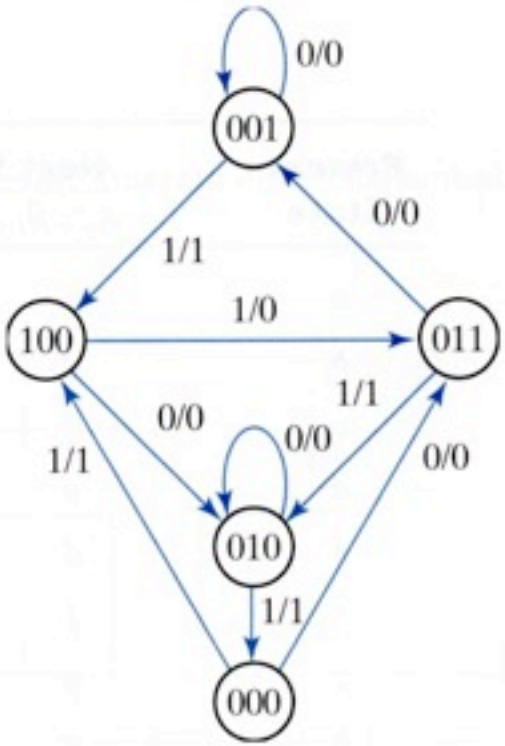
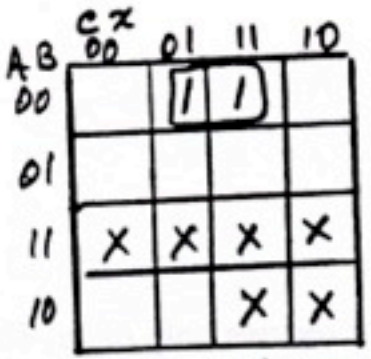


FIGURE P5-19

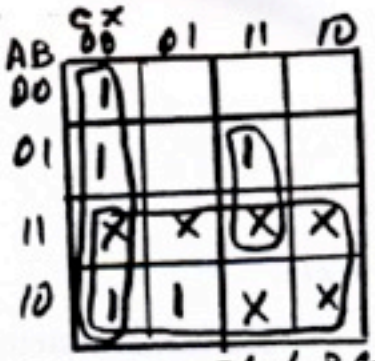
5-19 (a)

Present state ABC	Input x	Next state ABC	output y
000	0	011	0
000	1	100	1
001	0	001	0
001	1	100	1
010	0	010	0
010	1	000	1
011	0	001	0
011	1	010	1
100	0	010	0
100	1	011	0

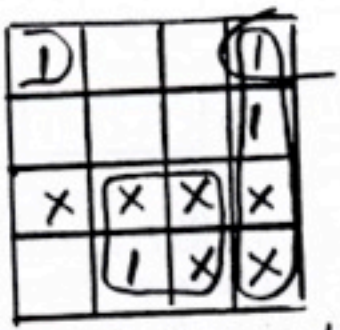
$d(A,B,C,x) = \Sigma(10,11,12,13,14,15)$



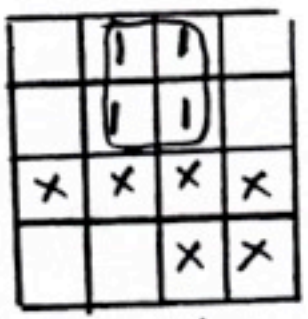
$DA = A'B'x$



$DB = A + C'x' + BCx$



$DC = Cx' + Ax + A'B'x'$



$y = A'x$

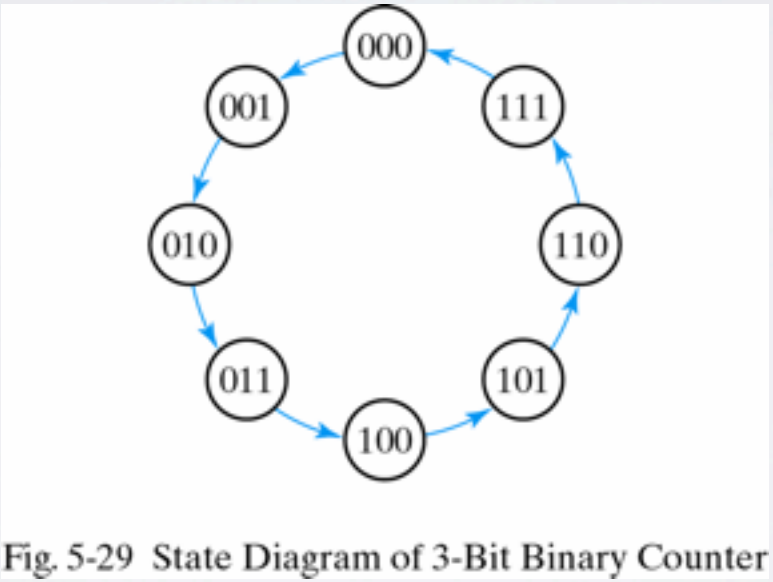


Fig. 5-29 State Diagram of 3-Bit Binary Counter

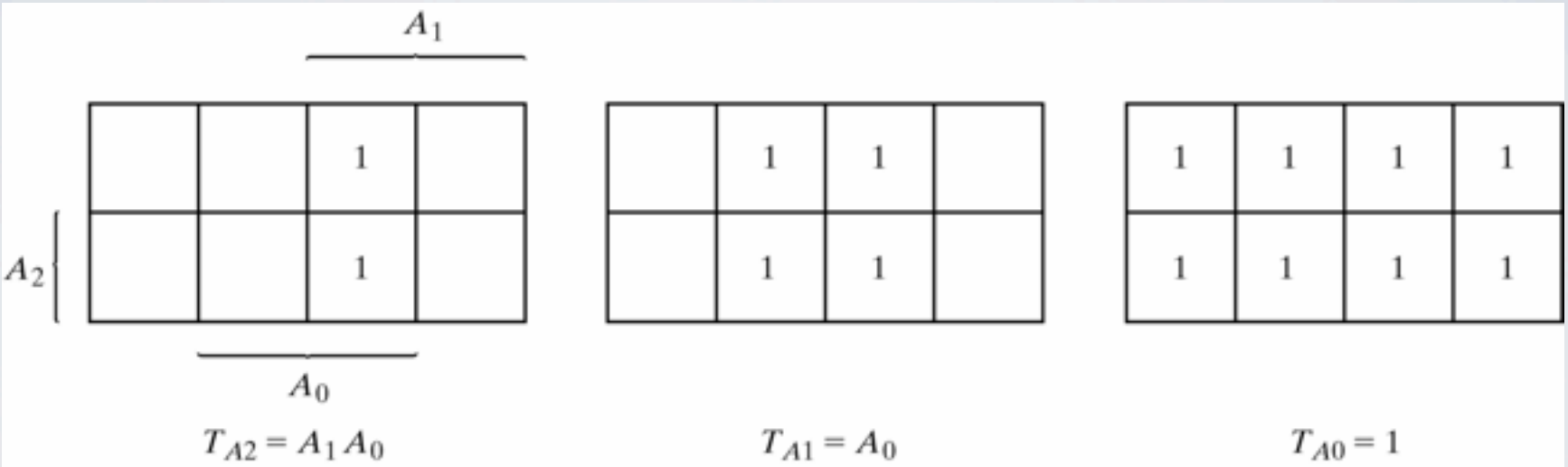


Fig. 5-30 Maps for 3-Bit Binary Counter

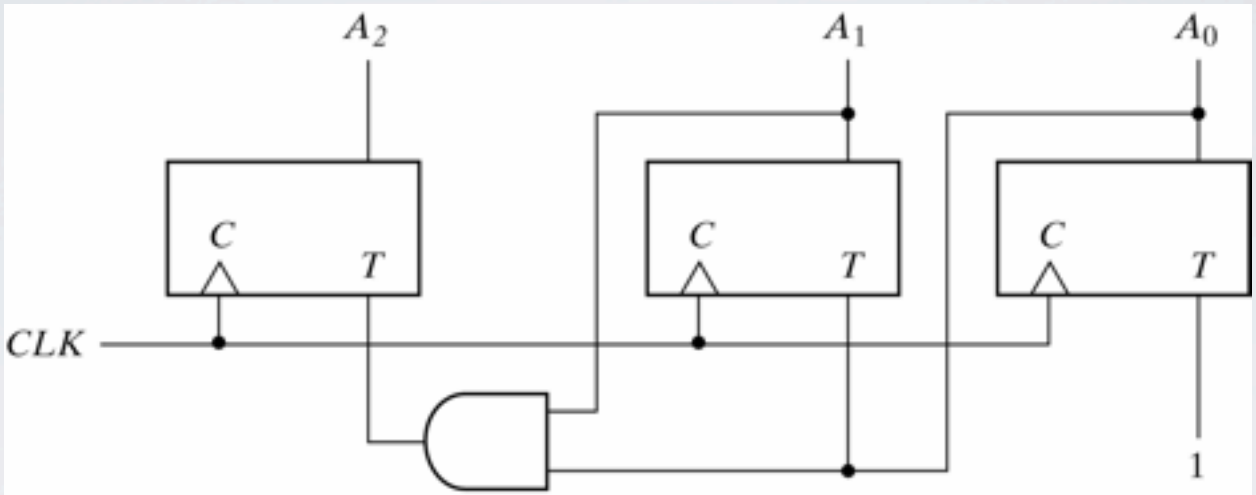


Fig. 5-31 Logic Diagram of 3-Bit Binary Counter