INEL 4205 Digital Logic Circuits

Practice Problem Set 1 for Exam 3

1. Design a sequence detector. The circuit has one 1-bit input **x** and one 1-bit output **z**. The output becomes a logic **1** for one clock cycle if the sequence **0010** (two **0**, followed by a **1** and then by a **0)** is detected in the input **x**. Overlapping sequences should be detected. Your solution should include:
    a. state diagram and state transition table. Use sequential state codes.
    b. K-maps to minimize the combinational part of the circuit <u>for the least-significant state bit only</u> using a JK flip flop. Show the resulting Boolean algebra equations for J and K.
    c. Repeat part b for the second bit using a T flip flop.
2. Design a 3-bit UP/DOWN counter. The device has a single-bit input UP/DOWN. It should repeatedly count from 0 to 7 if the UP/DOWN is logic-1, and from 7 to 0 otherwise. Use T flip flops.
3. Design a circuit that will repeatedly go through the following binary sequence: 0, 1, 2, 4, 6. Use D-type flip flops.
4. Show how to implement a JK flip flop using a 2 x 1 multiplexer, inverters, and a D flip flop. (Hint: Use the flip flop's Q as the multiplexer's select bit)
5. A circuit has two JK flip flops, one input **x** and one output **z**. Determine the output sequence for an input sequence of 01011011101111010 if the combinational part of the circuit is governed by the following logic equations:

    $J_A = B\mathbf{x}$ $\quad$ $K_A = B'\mathbf{x}$ $\quad$ $J_B = A'\mathbf{x}$ $\quad$ $K_B = A + \mathbf{x}$ $\quad$ $z = A\mathbf{x}' + B\mathbf{x}$
6. Find the state diagram for a circuit capable of detecting the following sequences: 010 or 1001. The circuit's output should become logic-1 when either 010 or 1001 are received in its 1-bit serial input. Perform a state reduction step to eliminate any states that are not needed. Draw the diagram for (a) a Moore FSM, and (b)a Mealy FSM. Overlapping sequences are allowed.

Table 5-1
Flip-Flop Characteristic Tables

***JK* Flip-Flop**

J	K	$Q(t+1)$	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

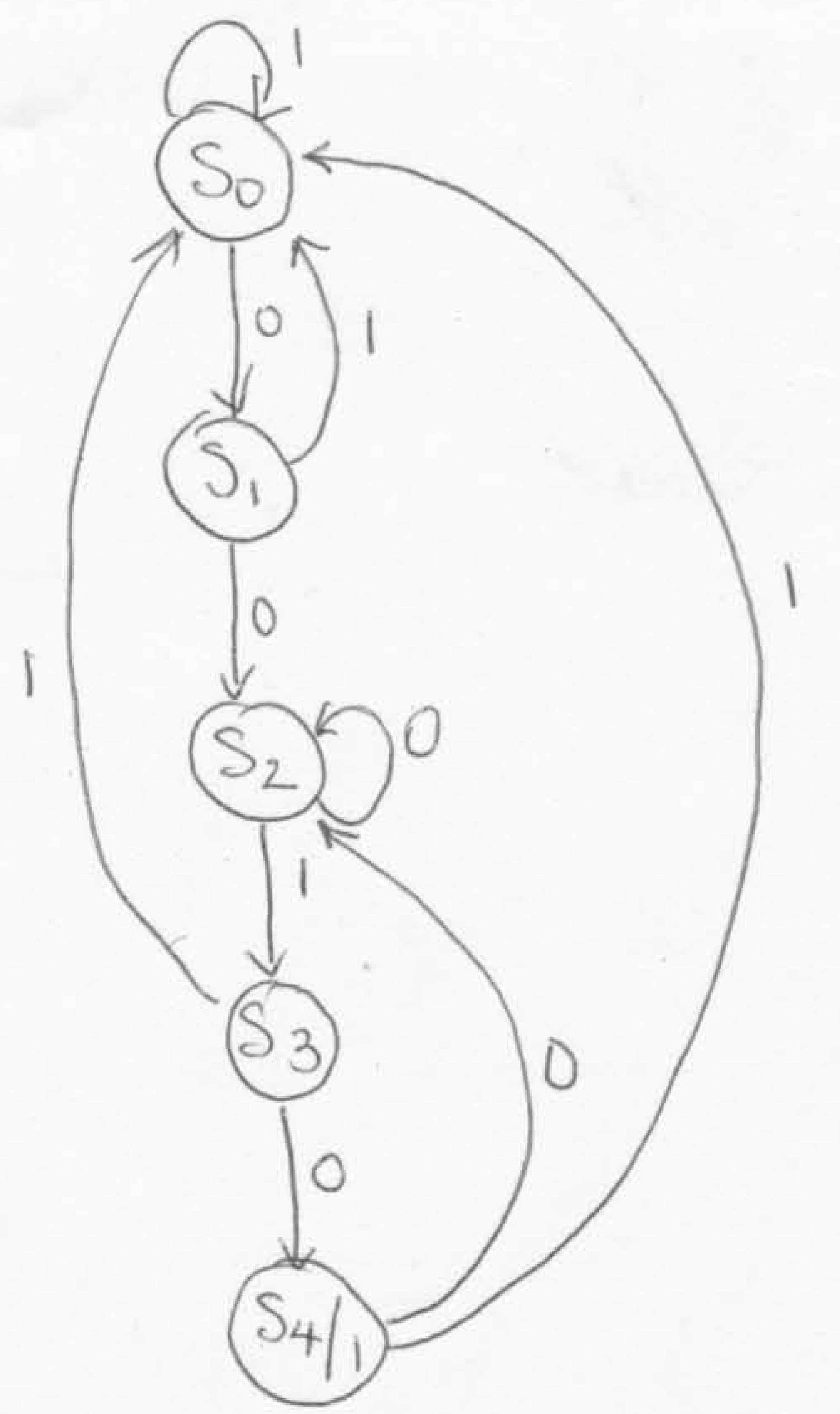
***D* Flip-Flop**

D	$Q(t+1)$	
0	0	Reset
1	1	Set

***T* Flip-Flop**

T	$Q(t+1)$	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

(1)



$S_0 = 000$

$S_1 = 001$

$S_2 = 010$

$S_3 = 011$

$S_4 = 100$

Q(t)	Q(t+1)	J K
0	0	0X
0	1	1X
1	0	X1
1	1	X0

pres. ABC	input xin	next ABC	J_C K_C	T_B	output Z
000	0	001	1 X	0	0
000	1	000	0 X	0	0
001	0	010	X 1	1	0
001	1	000	X 1	0	0
010	0	010	0 X	0	0
010	1	011	1 X	0	0
011	0	100	X 1	1	0
011	1	000	X 1	1	0
100	0	010	0 X	1	1
100	1	000	0 X	0	1

x ↓ not used

J_C

AB \ Cx	00	01	11	10
00	1	0	X	X
01	0	1	X	X
11	X	X	X	X
10	0	0	X	X

$\boxed{J_C = BX + A'B'X'}$

K_C

AB \ Cx	00	01	11	10
00	X	X	1	1
01	X	X	1	1
11	X	X	X	X
10	X	X	X	X

$\boxed{K_C = 1}$

T_B

AB \ Cx	00	01	11	10
00	0	0	0	1
01	0	0	1	1
11	X	X	X	X
10	1	0	X	X

$\boxed{T_B = Cx' + BC + Ax'}$

(2)

up/$\overline{down}$	pres ABC	next ABC	$T_A T_B T_C$
0	000	111	111
0	001	000	001
0	010	001	011
0	011	010	001
0	100	011	111
0	101	100	001
0	110	101	011
0	111	110	001

up/$\overline{down}$	pres ABC	next ABC	$T_A T_B T_C$
1	000	001	001
1	001	010	011
1	010	011	001
1	011	100	111
1	100	101	001
1	101	110	011
1	110	111	001
1	111	000	111

let xin be up/$\overline{down}$

(2) cont.

T_A

$x_{in}A \backslash BC$	00	01	11	10
00	1	0	0	0
01	1	0	0	0
11	0	0	1	0
10	0	0	1	0

$\boxed{T_A = \bar{x}_{in}\bar{B}\bar{C} + x_{in}BC}$

T_B

$x_{in}A \backslash BC$	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	0	1	1	0
10	0	1	1	0

$\boxed{T_B = \bar{x}_{in}\bar{C} + x_{in}C}$

$\boxed{T_C = 1}$

(3)

present ABC	next ABC
000	001
001	010
010	100
100	110
110	000

011, 101 & 111 → X

D_A

$A \backslash BC$	00	01	11	10
0			X	1
1	1	X	X	

$D_A = AB'C' + A'BC'$

$D_A = A\bar{B} + A'B$

D_B

$A \backslash BC$	00	01	11	10
0		1	X	
1	1	X	X	

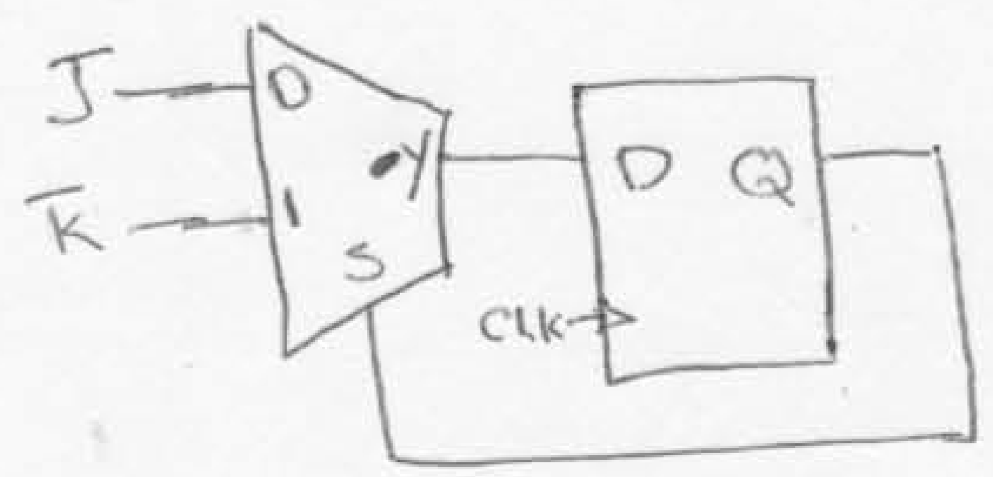
$D_B = AB'C' + A'B'$

$D_B = C + AB'$

$D_C = A'B'C'$

D_C → only a single 1
no reduction possible

(4)



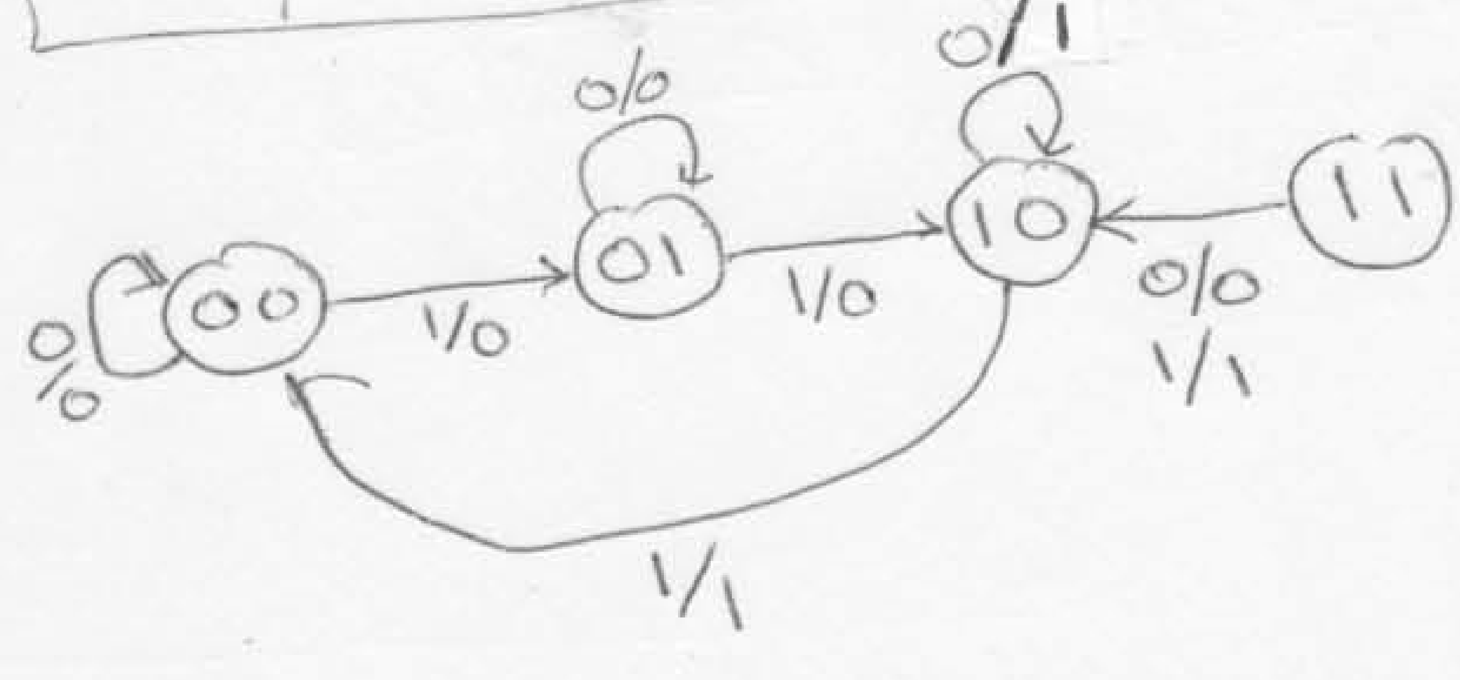
Q	J K	Q(t+1)
0	0 0	0
0	0 1	0
0	1 0	1
0	1 1	1
1	0 0	1
1	0 1	0
1	1 0	1
1	1 1	0

when $Q(t) = 0$
$D = J$

when $Q(t) = 1$
$D = \bar{K}$

(5)

$J_A K_A J_B K_B$	pres AB	input X	next AB	output Z
0 0 0 0	00	0	00	0
0 1 1 1	00	1	01	0
0 0 0 0	01	0	01	0
1 0 1 1	01	1	10	1
0 0 0 1	10	0	10	1
0 1 D 1	10	1	00	1
0 0 0 1	11	0	10	0
1 0 0 1	11	1	10	1

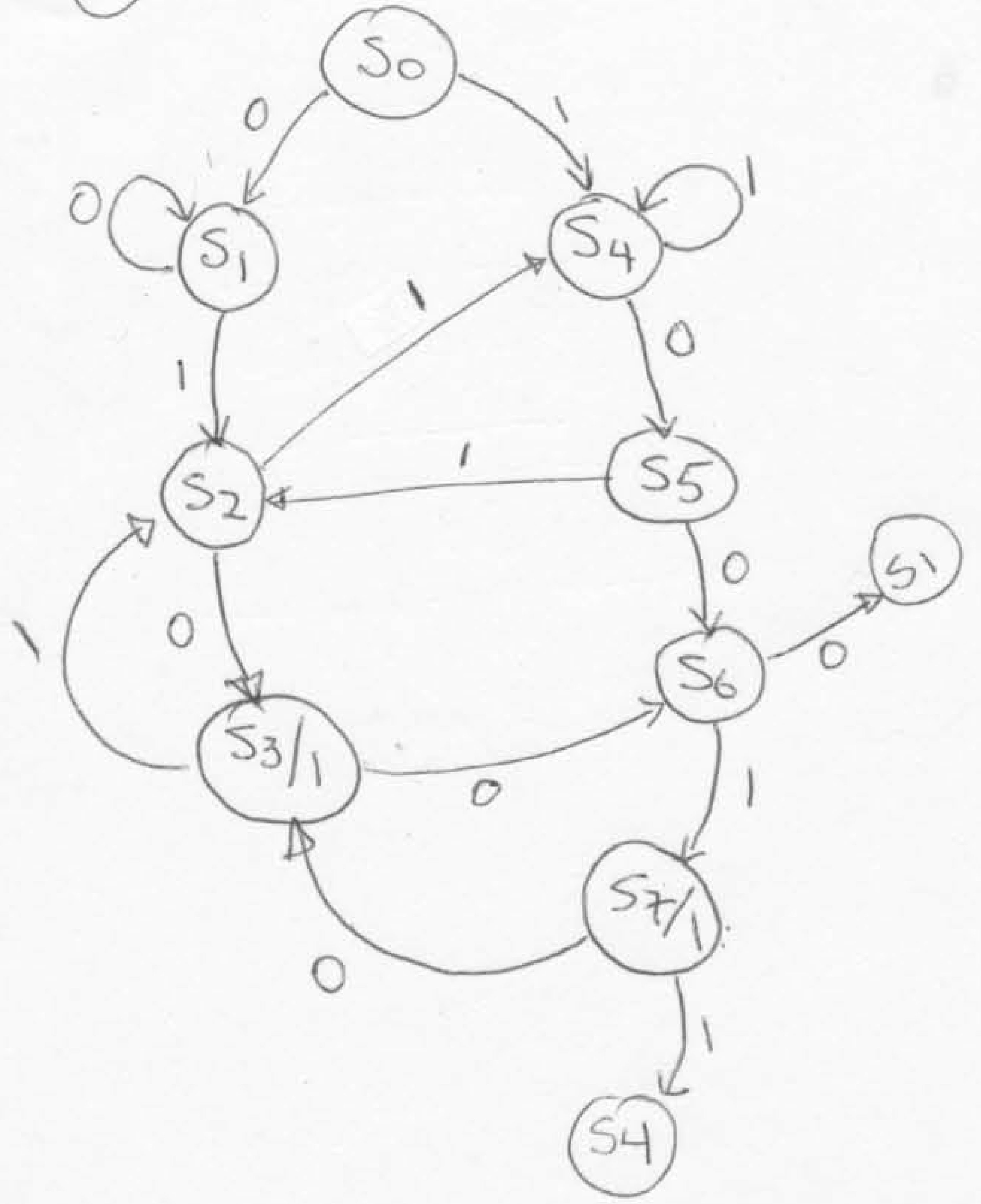


0101101110111010 ← input seq.
0000100010001000 1 ← output seq.
0000100010001000 1

Nota: la tabla tiene un error; las posiciones sexta y septima deberian estar intercambiadas

(6) (a)

010 or 1001

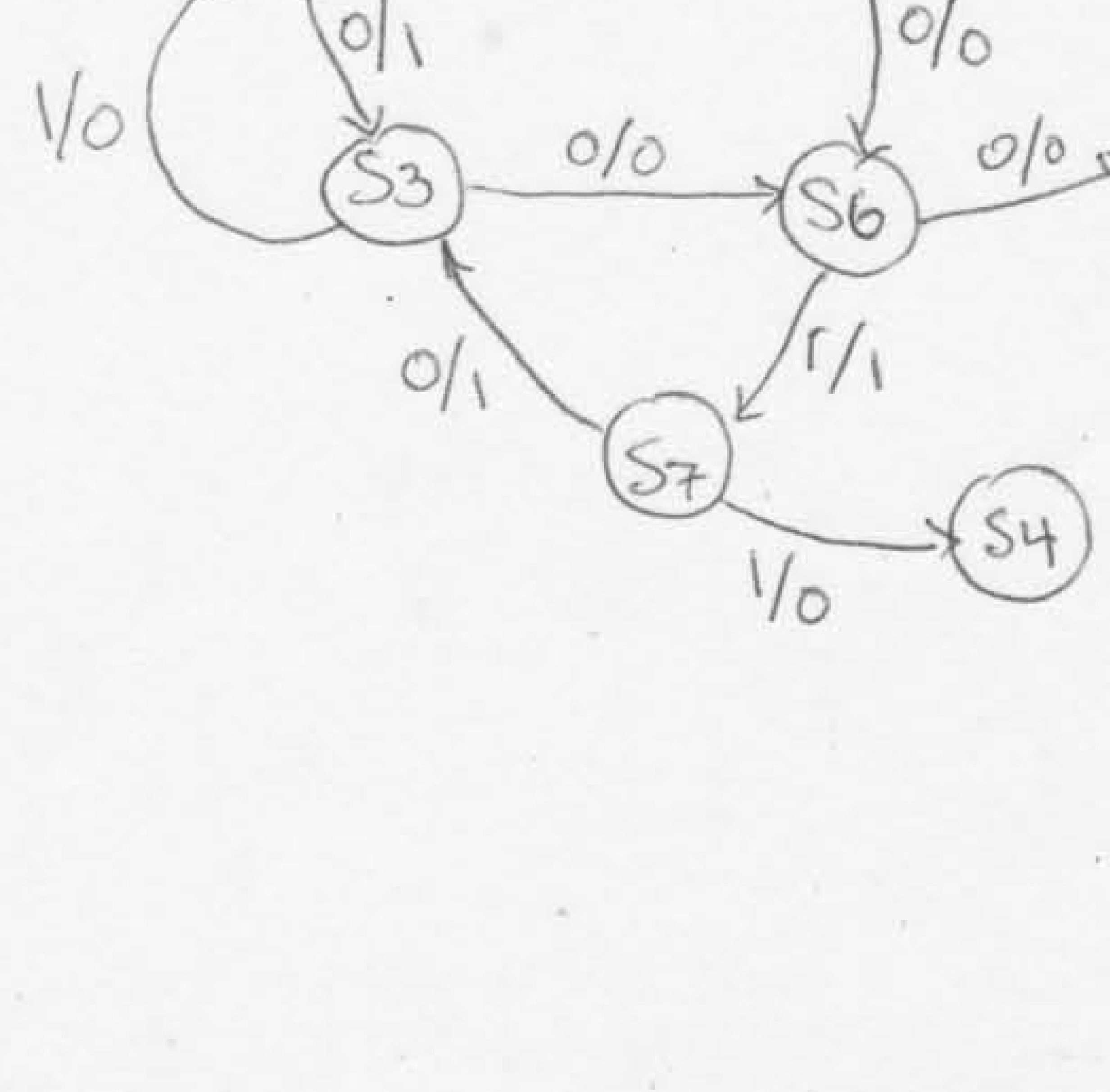


note: output ~~is~~ only indicated for states where it is 1. States without an output have it equal to $\emptyset$

	next x=0	next x=1	output	
S_0	S_1	S_4	0	
S_1	S_1	S_2	0	
S_2	S_3	S_4	0	
S_3	S_6	S_2	1	
S_4	S_5	S_4	0	
S_5	S_6	S_2	0	
S_6	S_1	S_7	0	
S_7	S_3	S_4	1	

the are no equivalent states

(b)

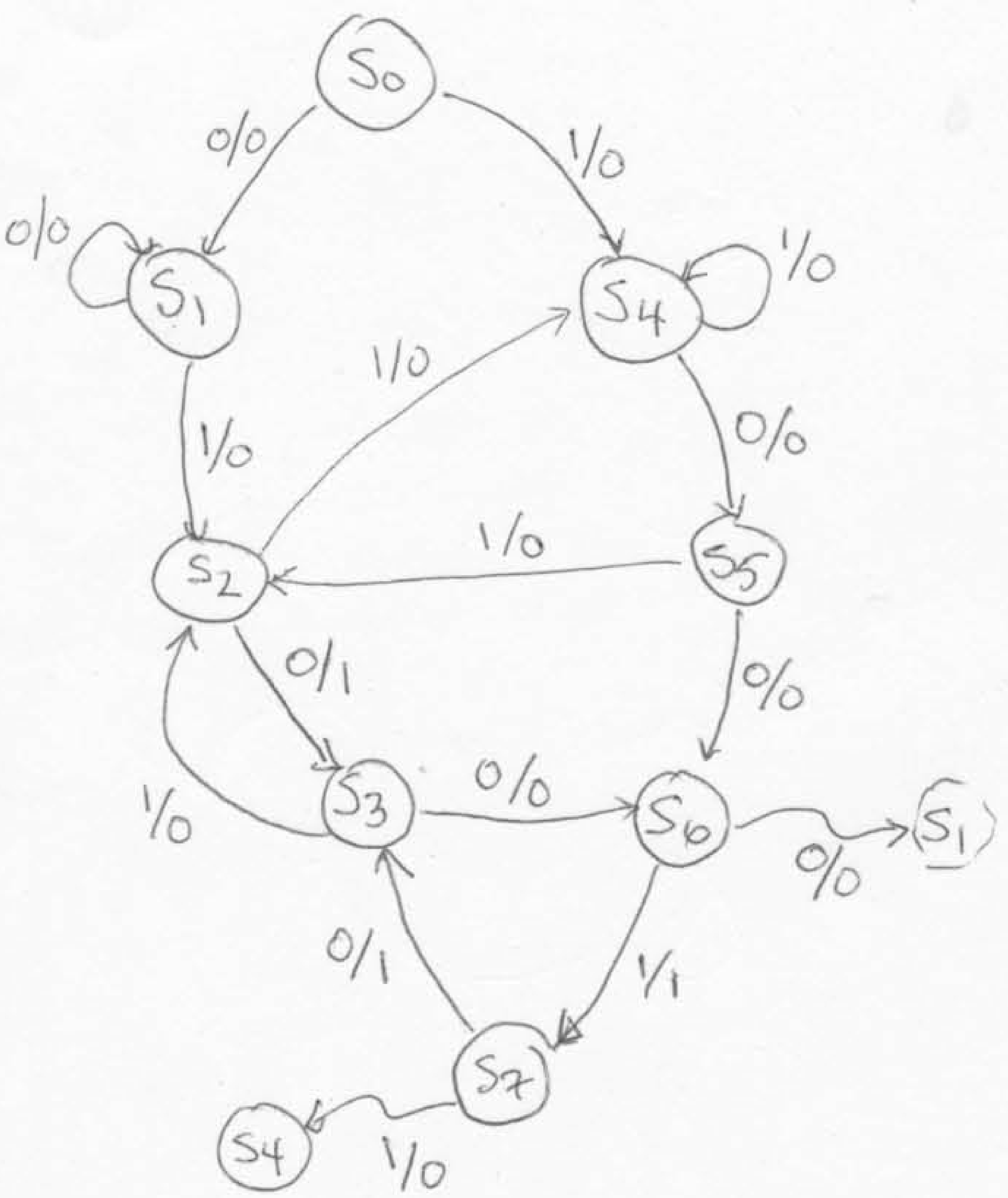


	next x=0	next x=1	output x=0	output x=1
S_0	S_1	S_2 ~~S_4~~	0	0
S_1	S_1	S_2	0	0
S_2	S_3	S_2 ~~S_4~~	1	0
S_3	S_6	S_2	0	0
~~S_4~~	S_3 ~~S_5~~	~~S_4~~	~~0~~	~~0~~
~~S_5~~	~~S_6~~	~~S_2~~	~~0~~	~~0~~
S_6	S_1	~~S_7~~ S_2	0	1
~~S_7~~	~~S_3~~	~~S_4~~	~~1~~	~~0~~

S_7 & S_2 are equivalent
S_5 & S_3 are equivalent
S_4 & S_2 are equivalent

	next x=0	next x=1	output x=0	output x=1
S_0	S_1	S_2		

6



	x = 0	x = 1	x = 0	x = 1
S_0	S_1	S_4	0	0
S_1	S_1	S_2	0	0
S_2	S_3	S_4	1	0
S_3	S_6	S_2	0	0
S_4	~~S_5~~ S_3	S_4	0	0
~~S_5~~	~~S_6~~	~~S_2~~	~~0~~	~~0~~
S_6	S_1	~~S_7~~ S_2	0	1
~~S_7~~	~~S_3~~	~~S_4~~	~~1~~	~~0~~

S_7 is equivalent to S_2

S_5 is " " S_3

re-label S_6 as S_5

	x=0	x=1	x=0	x=1
S_0	S_1	S_4	0	0
S_1	S_1	S_2	0	0
S_2	S_3	S_4	1	0
S_3	S_5	S_2	0	0
S_4	S_3	S_4	0	0
S_5	S_1	S_2	0	1

new state diagram