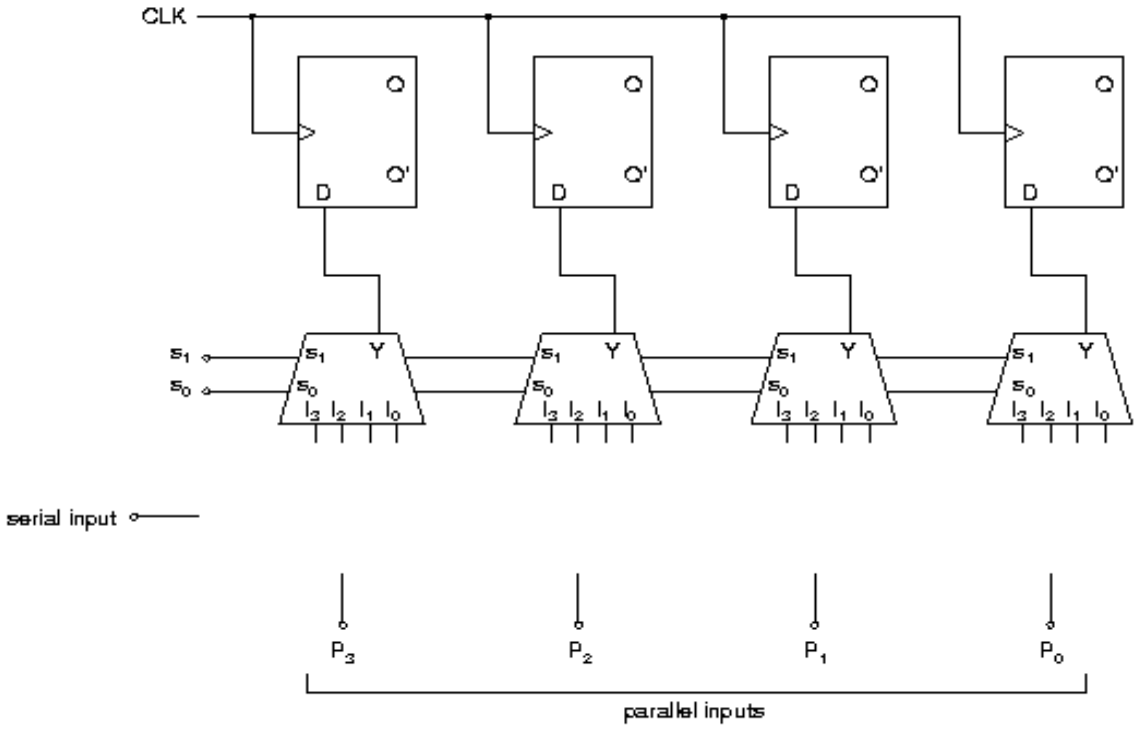
INEL 4205 - Extra Practice Problems - Exam 4 – Spring 2009

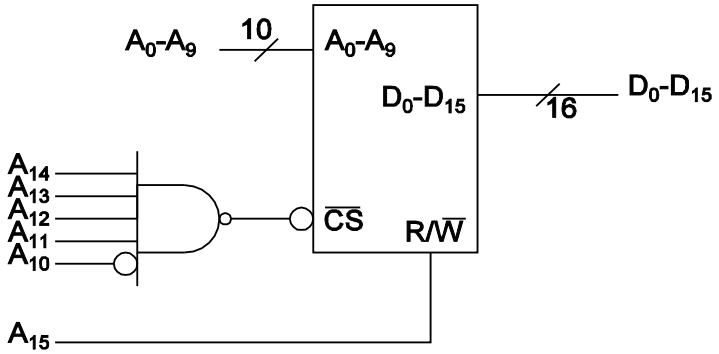
This problems are just examples and are not indicative of the exam that you will take.
You will prepare better for the exam by first reading the chapters 6 and 7 and working on the textbook problems.

1. The following diagram shows four D-flip flops and four 4×1 multiplexers. The multiplexer inputs, output and select terminals are indicated by the letters *I*, *Y*, and *s*, respectively. Notice that the select lines s_1s_0 are common to all multiplexers. Complete the diagram so that the circuit operates as follows:

s_1s_0	action
00	Parallel load – loads parallel inputs into register
01	Hold – keeps the register contents
10	Negate – complements the register contents
11	Shift right; serial input is inserted in first (left) flip flop



2. The following diagram shows how a RAM chip is connected to a CPU that have 16-bit data and address buses.



a. How many bytes of information can be stored in the RAM?

b. Determine the addresses that the CPU can use to read data from RAM. For each range, express the beginning and ending address in hex.

c. Repeat part b, but for the addresses that the CPU can use to write data into RAM.

3. Determine the PLA programming table needed to implement the following two boolean functions. Minimize the number of product terms. Show all your work, including the Karnaugh maps used in the minimization.

$F_1 (A,B,C,D) = \sum(1, 3, 4, 5, 7, 13, 15)$
$F_2 (A,B,C,D) = \sum(0, 2, 3, 6, 7, 8, 10, 11, 12, 14)$

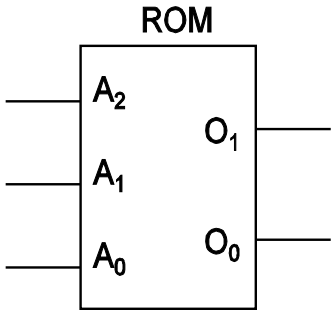
Write your result in the following table.

Product terms	Inputs A B C D	Outputs ( ) F_1	( ) F_2

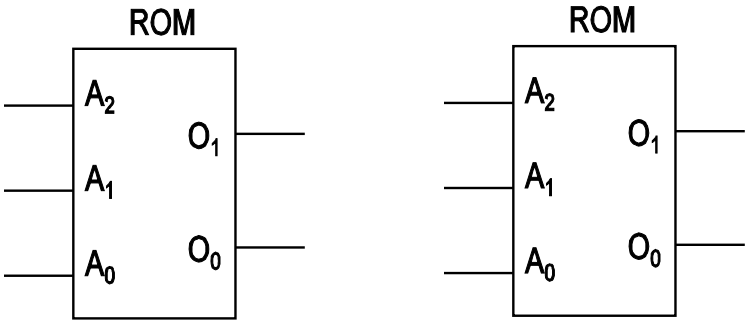
Note: not all rows need to be used

4. Show how to use a ROM to implement a full-subtractor that finds the difference x-y between the two 1-bit inputs x and y, and accepts a borrow input b_{in}. The output should be a 1-bit difference d and a 1-bit borrow b_{out}. Fill the following table with the contents of the ROM. Specify how do you connect the variables to the chip's inputs and outputs on the schematic diagram, shown on the right-hand-side.

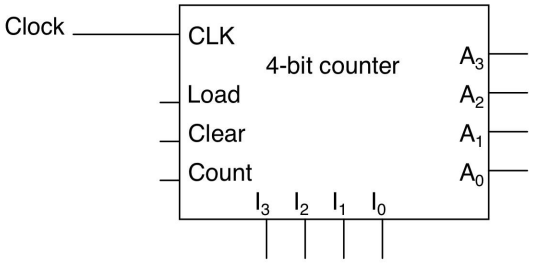
Address $A_2A_1A_0$	Content O_1O_0
000	
001	
010	
011	
100	
101	
110	
111	



5. On the diagram shown below, specify and label the external connections that you would use to construct a 2-bit subtractor using two ROMs like the one developed in problem 4. The new circuit should accept two 2-bit numbers x_1x_0 and y_1y_0 and a borrow input b_{in}. The output should be a 2-bit difference d_1d_0 and a 1-bit borrow b_{out}. You should write on the diagram where would the input and output bits are to be connected and also how to connect the first ROM borrow output to the second ROM.



6. The following sketch represents a 4-bit binary counter with parallel load and clear inputs. Applying a logic-1 in the "Load" input causes the signals in inputs $I_3I_2I_1I_0$ to be loaded into the counter. A logic-1 in the "Clear"input resets the count to 0000. A logic-1 at the "Count" input enables counting; a logic-0 at this input prevents counting. The device count appears in the outputs $A_3A_2A_1A_0$. Show how to construct a device that will count from 2 to 11 repetitively using this counter, by connecting inputs to logic-1, logic-0 or by adding external logic gates. Initially, your circuit might go through counts 0000 and 0001, but only the first time power is applied to the device.



7. The stimulus program shown below is used to simulate the binary counter with parallel load described in the module named "counter". Going over the program, predict what would be the output of the counter and the carry output from t=0 to t=155ns.

```
//Binary counter with parallel load
module counter (Count,Load,IN,CLK,Clr,A,CO);
  input Count,Load,CLK,Clr;
  input [3:0] IN;              //Data input
  output CO;                   //Output carry
  output [3:0] A;              //Data output
  reg [3:0] A;
  assign CO = Count & ~Load & (A == 4'b1111);
  always @ (posedge CLK or negedge Clr)
    if (~Clr) A = 4'b0000;
    else if (Load)  A = IN;
    else if (Count) A = A + 1'b1;
    else A = A;                // no change, default condition
endmodule

// Stimulus for testing counter
module testcounter;

   reg Count, Load, CLK, Clr;
   reg [3:0] IN ;
   wire C0 ;
   wire [3:0] A ;
   counter cnt (Count, Load, IN, CLK, Clr, A, C0)
   always
           #5 CLK = ~CLK ;
      initial
        begin
           Clr = 0;
           CLK = 1;
           Load = 0; Count = 1;
             #5 Clr = 1;
             #50 Load = 1; IN = 4'b1100;
             #10 Load = 0;
             #70 Count = 0;
             #20 $finish;
        end
endmodule
```

8. A 12-bit Hamming code word containing 8 bits of data and 4 parity bits is read from memory. What was the original 8-bit data word that was written into memory if the 12-bit word read out is as follows:

a. 101110000110
b. 101111110100

9. Draw the logic diagram of a 4-bit register with four D flip-flops and four 4×1 multiplexers with mode selection inputs s_1 and s_0. The register operates according to the following function table.

S1	S0	Register Operation
0	0	Complement the four outputs
0	1	Shift right
1	0	Shift left
1	1	Load parallel data

10. Mark the fuse map of the PAL, using the following sketch and indicating a connection with an X, to indicate how it should be programmed to implement the following Boolean functions, given in sum of minterms form:

F1(A,B,C,D) = Σ(7,8,9,10,11,12,13,14,15)
F2(A,B,C,D) = Σ(2,12,13)
F3(A,B,C,D) = Σ(0,2,3,4,5,6,7,8,10,11,15)
F4(A,B,C,D) = Σ(1,2,8,12,13)

Appropriately label the inputs and outputs. Show any other work in the next page.