

# BOOLEAN ALGEBRA

INEL4205 - Spring 2012

# OPERACIONES BÁSICAS

- AND - Salida es “1” si todas las entradas son “1”
- OR - salida es “1” si alguna entrada es “1”
- Not (complemento) - salida es “1” si la entrada es “0”, “0” si la entrada es “1”

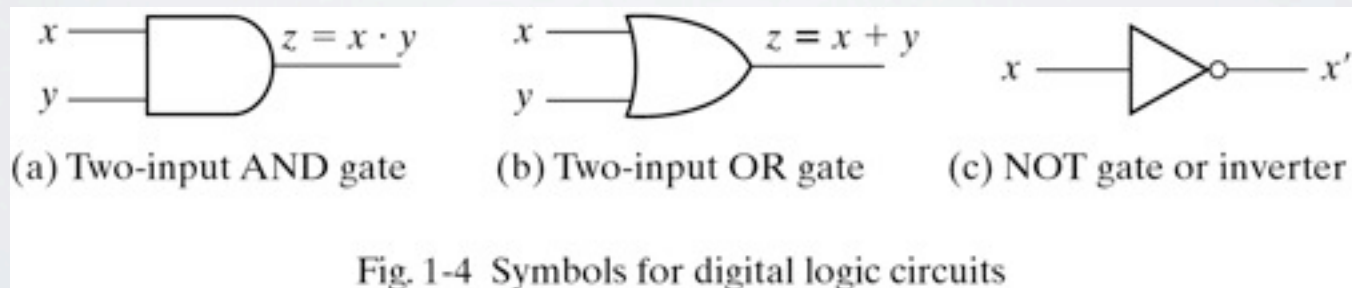


Fig. 1-4 Symbols for digital logic circuits

# TABLAS DE VERDAD

- la tala de verdad presenta la salida para todas las combinaciones posibles de las entradas
- si hay “n” entradas, el total de combinaciones únicas es  $2^N$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

AND

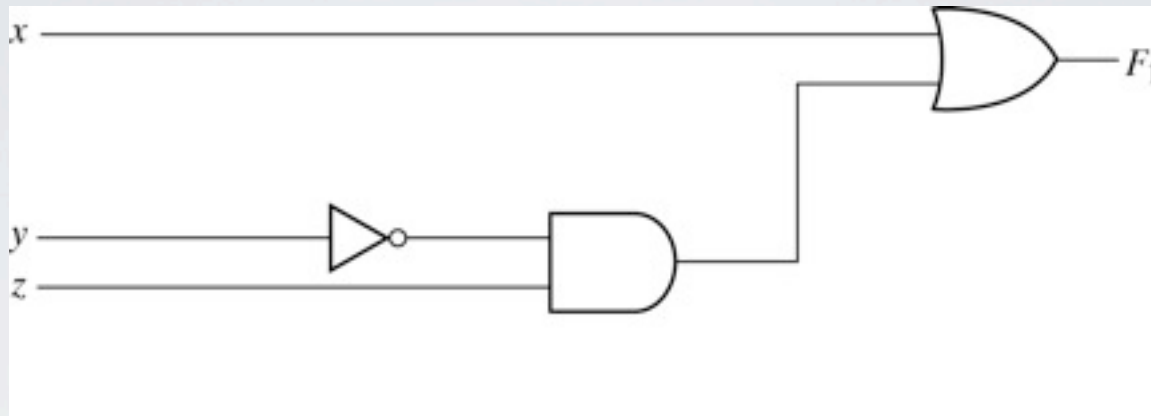
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

OR

A	Y
0	1
1	0

NOT

# EXPRESIÓN BOOLEANA



Escriba la tabla de verdad y la expresión booleana que representa la salida " $F_1$ " en términos de las entradas " $x$ ", " $y$ " y " $z$ "

**Table 2-1***Postulates and Theorems of Boolean Algebra*

Postulate 2	(a)	$x + 0 = x$	(b)	$x \cdot 1 = x$
Postulate 5	(a)	$x + x' = 1$	(b)	$x \cdot x' = 0$
Theorem 1	(a)	$x + x = x$	(b)	$x \cdot x = x$
Theorem 2	(a)	$x + 1 = 1$	(b)	$x \cdot 0 = 0$
Theorem 3, involution		$(x')' = x$		
Postulate 3, commutative	(a)	$x + y = y + x$	(b)	$xy = yx$
Theorem 4, associative	(a)	$x + (y + z) = (x + y) + z$	(b)	$x(yz) = (xy)z$
Postulate 4, distributive	(a)	$x(y + z) = xy + xz$	(b)	$x + yz = (x + y)(x + z)$
Theorem 5, DeMorgan	(a)	$(x + y)' = x'y'$	(b)	$(xy)' = x' + y'$
Theorem 6, absorption	(a)	$x + xy = x$	(b)	$x(x + y) = x$

postulado 4b forma 2

$$X + X'Y = X + Y$$

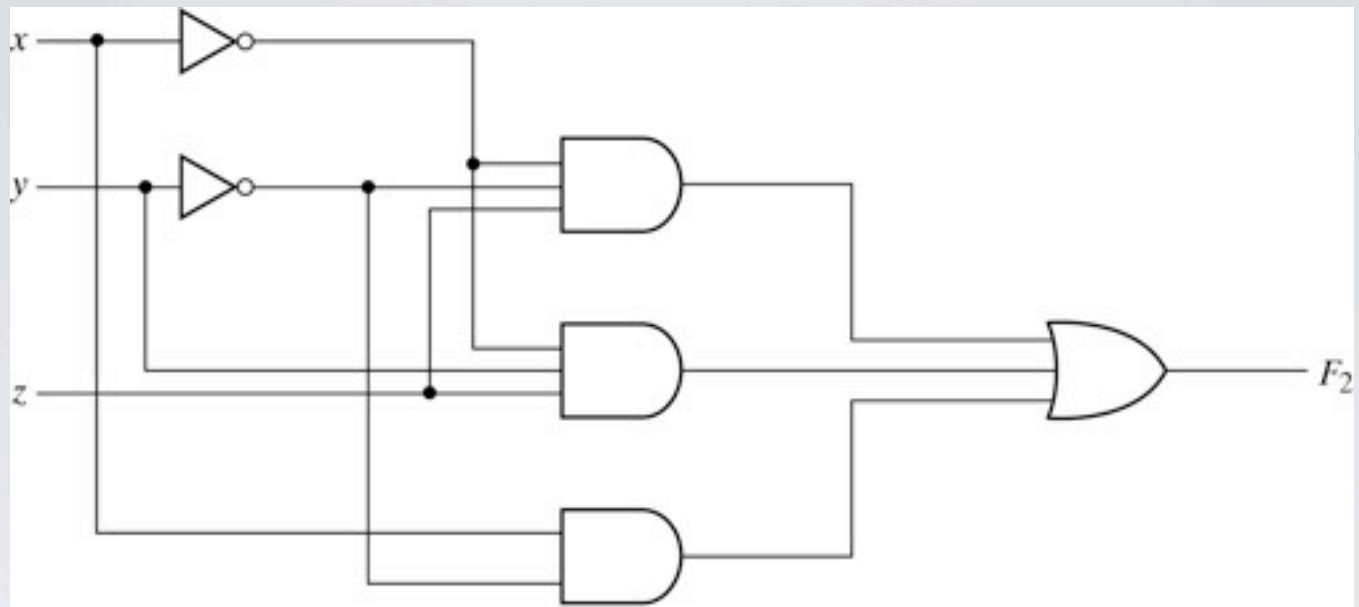
Teorema del Consenso

$$XY + X'Z + YZ = XY + X'Z$$

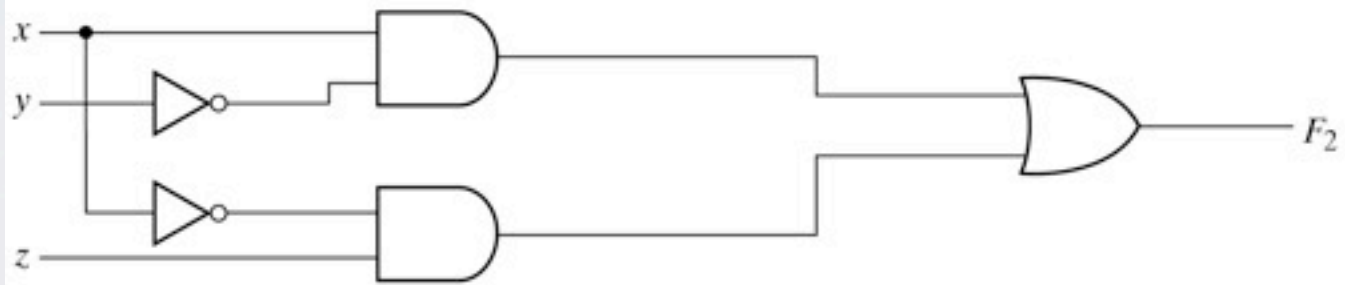
# SIMPLIFICACIÓN

- Simplifique la siguiente expresión booleana

$$F_2 = x'y'z + x'yz + xy'$$



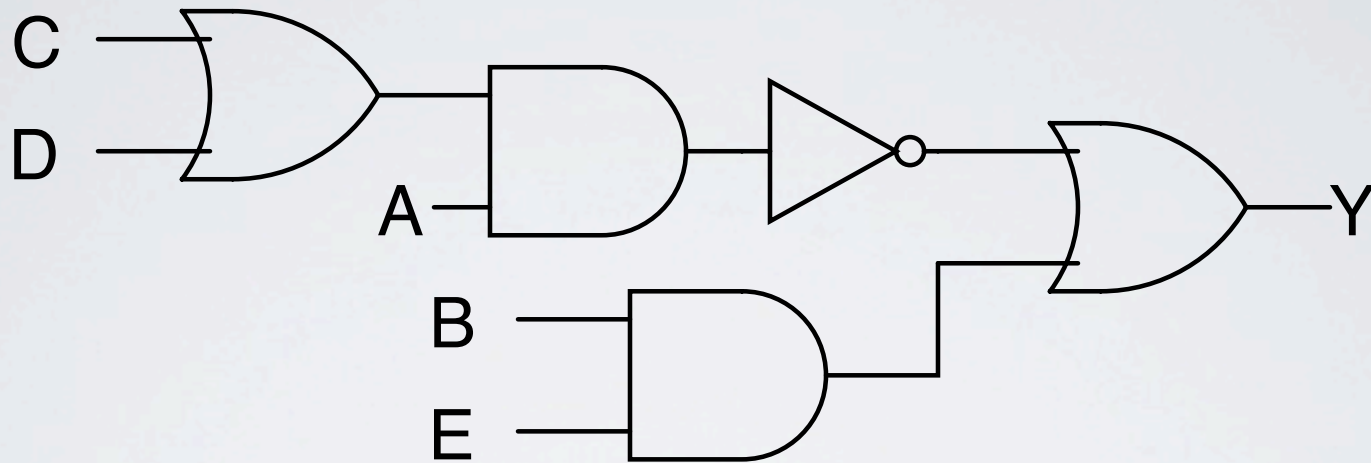
(a)  $F_2 = x'y'z + x'yz + xy'$



(b)  $F_2 = xy' + x'z$

Fig. 2-2 Implementation of Boolean function  $F_2$  with gates

# EJEMPLO



- Escriba la expresión booleana y la tabla de verdad para la “Y” del diagrama de arriba
- dibuje el diagrama para un circuito que produzca la siguiente salida

$$ACF + Dc'f'$$



# EJEMPLOS

1. determine el complemento de la siguiente expresión booleana:

$$(a'+b)c'$$

2. Demuestre que:

- $[(ab'+c)d'+e]' = [(a'+b)c'+d]e'$
- $x+xy=x$

# EJEMPLOS

simplifique:

- $x(x'+y)$
- $x+x'y$
- $(x+y)(x+y')$
- $xy+x'z+yz$
- $(x+y)(x'+z)(y+z)$

Práctica: probs. 2.2, 2.3 y 2.4

# TEOREMAS ADICIONALES

Aplicando el postulado 4b

$$X + X'Y = X + Y$$

llamemoslo postulado 4b forma 2

Teorema del Consenso

$$XY + X'Z + YZ = XY + X'Z + YZ(X + X')$$

$$XY + X'Z + YZ = XY(1 + Z) + X'Z(1 + Y)$$

$$XY + X'Z + YZ = XY + X'Z$$

Simplifiqu

$$abcd' + a'b'cd + cd'$$

$$\begin{aligned} &abcd' + a'b'cd + cd' \\ &(ab+1)cd' + a'b'CD \\ &c(d' + a'b'd) \end{aligned}$$

Por el postulado 4b forma 2

$$C(D' + A'B')$$

simplifique  
 $ab'c' + cd' + bc'd'$

$$ab'c + cd' + bc'd'$$
$$ab'c + (c + bc')d'$$

postulado 4b forma 2

$$ab'c + cd' + bd'$$

simplifiqué

$$(a + b')(a' + b' + d)(b' + c + d')$$



$$(a + b')(a' + b' + d)(b' + c + d')$$

dualidad

$$ab' + a'b'd + b'cd'$$

$$(a + a'd + cd')b'$$

$$(a + d + cd')b'$$

$$(a + d + c)b'$$

dualidad

$$acd + b'$$

$$xy + x'yz' + yz$$

$$\begin{aligned}
 & xy + x'yz' + yz \\
 & xy + x'yz' + yz(x + x') \\
 & xy(1 + z) + x'y(z' + z) \\
 & \quad xy + x'y \\
 & \quad Y
 \end{aligned}$$

$$(xy' + z)(x + y') z$$

$$\begin{aligned}
 & (xy' + z)(x + y') z \\
 & (xy' + zx + zy')z \\
 & xy'z + xz + y'z \\
 & (x + 1)y'z + xz \\
 & (x + y')z
 \end{aligned}$$

$$xy' + z + (x' + y)z'$$

$$xy' + z + (x' + y)z'$$

postulado 4b forma 2

$$xy' + x' + Y + z$$

postulado 4b forma 2

$$x' + Y' + Y + z$$

$$\boxed{1}$$

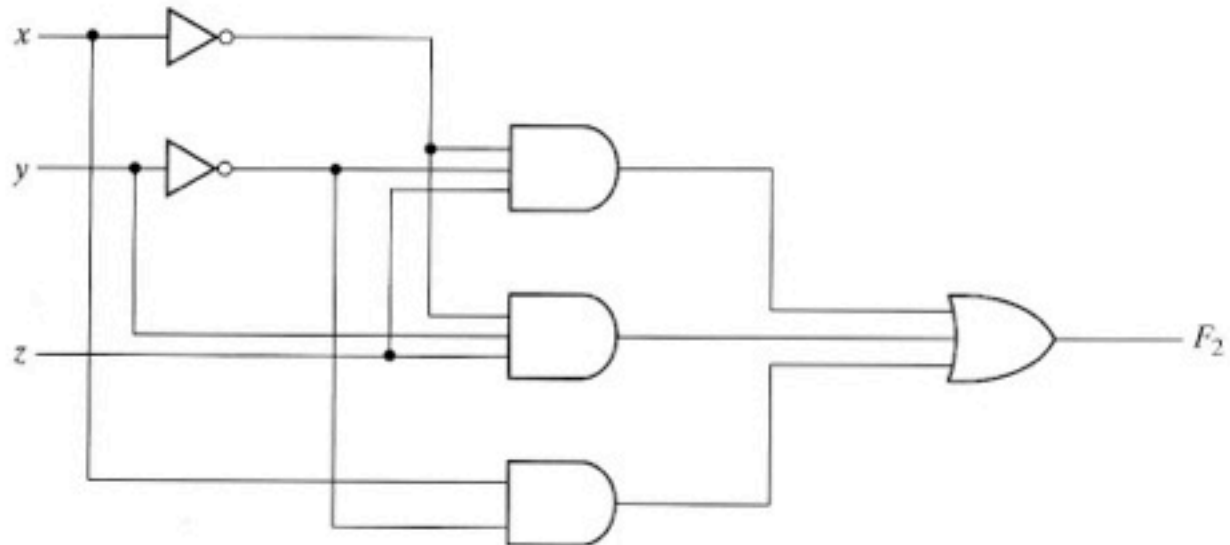
otra forma:

$$(xy' + z)' = (x' + y)z'$$

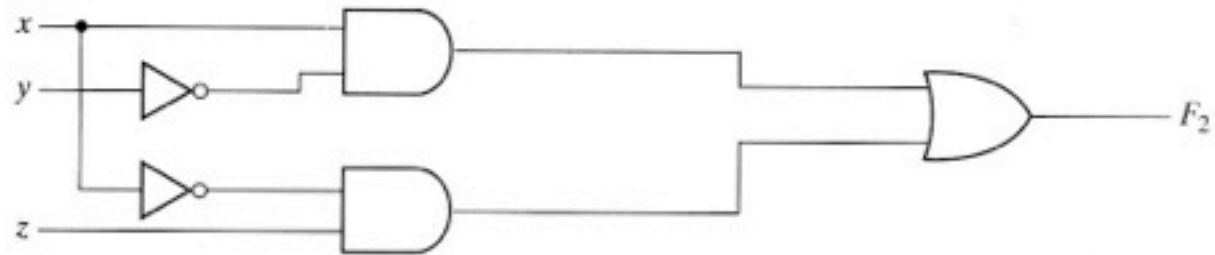
así que la expresión tiene la forma

$$A + A'$$

y por lo tanto siempre es 1



(a)  $F_2 = x'y'z + x'yz + xy'$  ← 3 términos; 8 literales



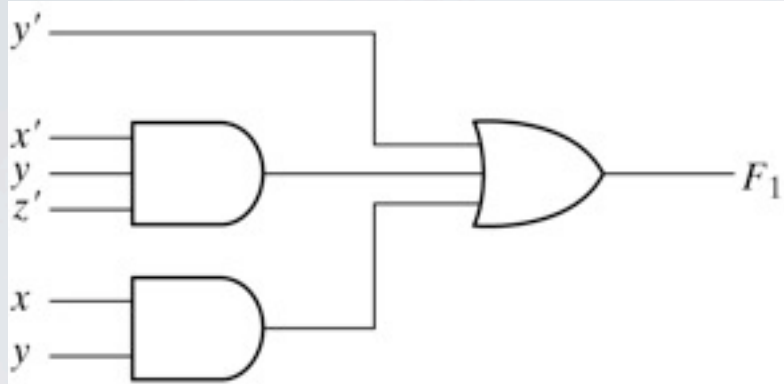
(b)  $F_2 = xy' + x'z$  ← 2 términos; 4 literales

**FIGURE 2-2**  
Implementation of Boolean function  $F_2$  with gates

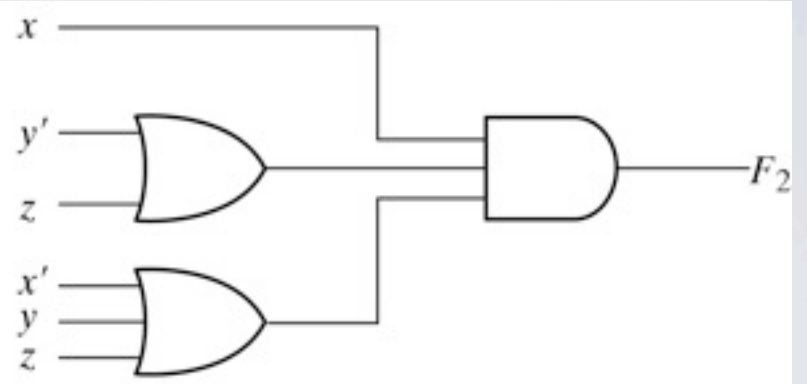


**Table 2-3**  
*Minterms and Maxterms for Three Binary Variables*

<b>x</b>	<b>y</b>	<b>z</b>	<b>Minterms</b>		<b>Maxterms</b>	
			<b>Term</b>	<b>Designation</b>	<b>Term</b>	<b>Designation</b>
0	0	0	$x'y'z'$	$m_0$	$x + y + z$	$M_0$
0	0	1	$x'y'z$	$m_1$	$x + y + z'$	$M_1$
0	1	0	$x'yz'$	$m_2$	$x + y' + z$	$M_2$
0	1	1	$x'yz$	$m_3$	$x + y' + z'$	$M_3$
1	0	0	$xy'z'$	$m_4$	$x' + y + z$	$M_4$
1	0	1	$xy'z$	$m_5$	$x' + y + z'$	$M_5$
1	1	0	$xyz'$	$m_6$	$x' + y' + z$	$M_6$
1	1	1	$xyz$	$m_7$	$x' + y' + z'$	$M_7$



(a) Sum of Products



(b) Product of Sums

Fig. 2-3 Two-level implementation

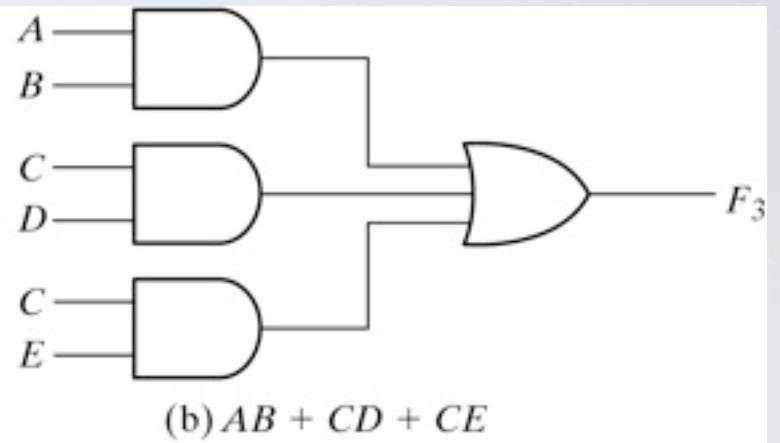
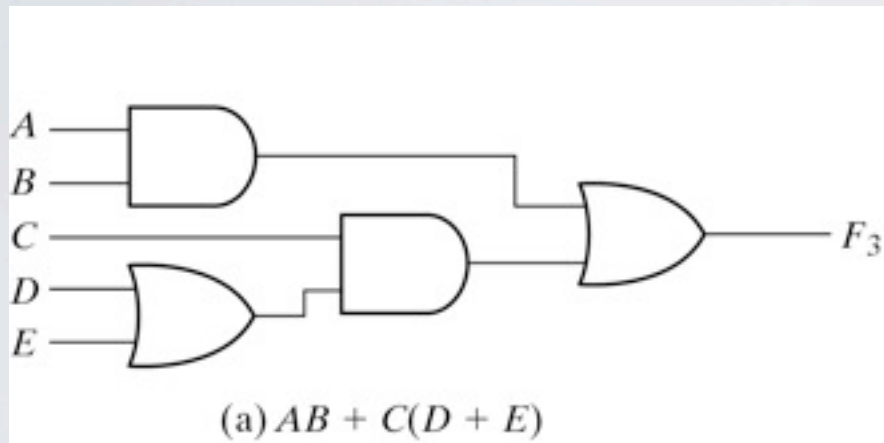


Fig. 2-4 Three- and Two-Level implementation









Name	Graphic symbol	Algebraic function	Truth table															
AND		$F = xy$	<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	x	y	F	0	0	0	0	1	0	1	0	0	1	1	1
x	y	F																
0	0	0																
0	1	0																
1	0	0																
1	1	1																
OR		$F = x + y$	<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	x	y	F	0	0	0	0	1	1	1	0	1	1	1	1
x	y	F																
0	0	0																
0	1	1																
1	0	1																
1	1	1																
Inverter		$F = x'$	<table border="1"> <thead> <tr> <th>x</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td></tr> </tbody> </table>	x	F	0	1	1	0									
x	F																	
0	1																	
1	0																	
Buffer		$F = x$	<table border="1"> <thead> <tr> <th>x</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td></tr> </tbody> </table>	x	F	0	0	1	1									
x	F																	
0	0																	
1	1																	
NAND		$F = (xy)'$	<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	x	y	F	0	0	1	0	1	1	1	0	1	1	1	0
x	y	F																
0	0	1																
0	1	1																
1	0	1																
1	1	0																
NOR		$F = (x + y)'$	<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	x	y	F	0	0	1	0	1	0	1	0	0	1	1	0
x	y	F																
0	0	1																
0	1	0																
1	0	0																
1	1	0																
Exclusive-OR (XOR)		$F = xy' + x'y$ $= x \oplus y$	<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	x	y	F	0	0	0	0	1	1	1	0	1	1	1	0
x	y	F																
0	0	0																
0	1	1																
1	0	1																
1	1	0																
Exclusive-NOR or equivalence		$F = xy + x'y'$ $= (x \oplus y)'$	<table border="1"> <thead> <tr> <th>x</th> <th>y</th> <th>F</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	x	y	F	0	0	1	0	1	0	1	0	0	1	1	1
x	y	F																
0	0	1																
0	1	0																
1	0	0																
1	1	1																

Fig. 2-5 Digital logic gates

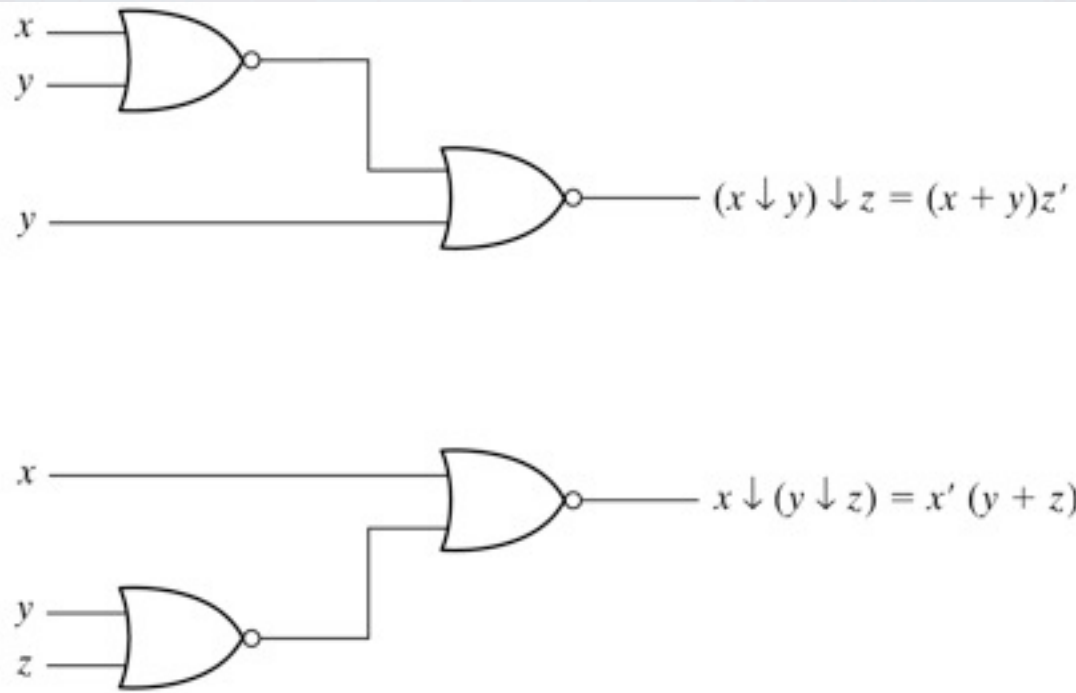
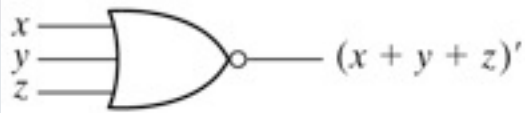
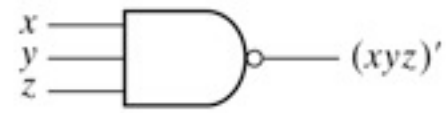


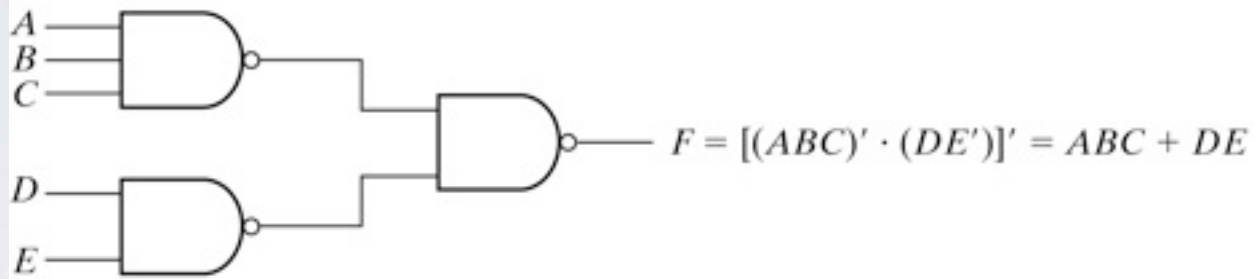
Fig. 2-6 Demonstrating the nonassociativity of the NOR operator;  $(x \downarrow y) \downarrow z \neq x \downarrow (y \downarrow z)$



(a) 3-input NOR gate



(b) 3-input NAND gate

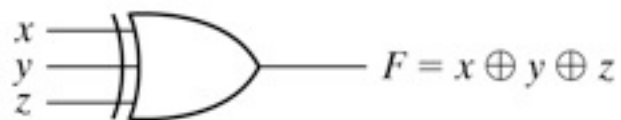


(c) Cascaded NAND gates

Fig. 2-7 Multiple-input and cascaded NOR and NAND gates



(a) Using 2-input gates



(b) 3-input gate

$x$	$y$	$z$	$F$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(c) Truth table

Fig. 2-8 3-input exclusive-OR gate

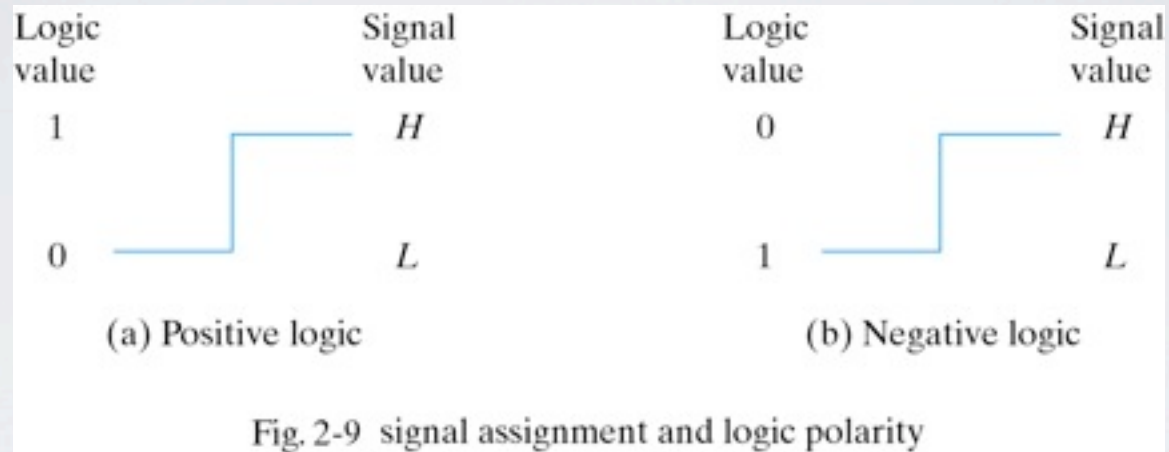
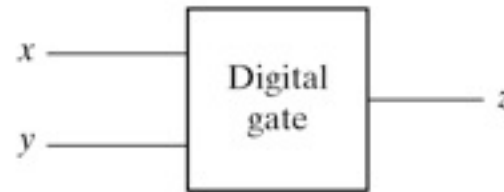


Fig. 2-9 signal assignment and logic polarity



$x$	$y$	$F$
$L$	$L$	$L$
$L$	$H$	$L$
$H$	$L$	$L$
$H$	$H$	$H$

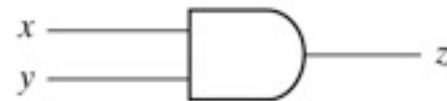
(a) Truth table with  $H$  and  $L$



(b) Gate block diagram

$x$	$y$	$z$
0	0	0
0	1	0
1	0	0
1	1	1

(c) Truth table for positive logic



(d) Positive logic AND gate

$x$	$y$	$z$
1	1	1
1	0	1
0	1	1
0	0	0

(e) Truth table for negative logic



(f) Negative logic OR gate

Fig. 2-10 Demonstration of positive and negative logic