ARITHMETIC CIRCUITS

INEL 4205 - Ch. 4 - Set 1

Spring 2012

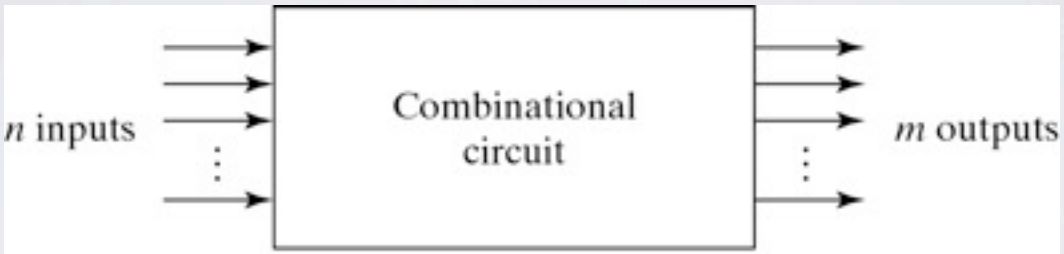


Fig. 4-1 Block Diagram of Combinational Circuit

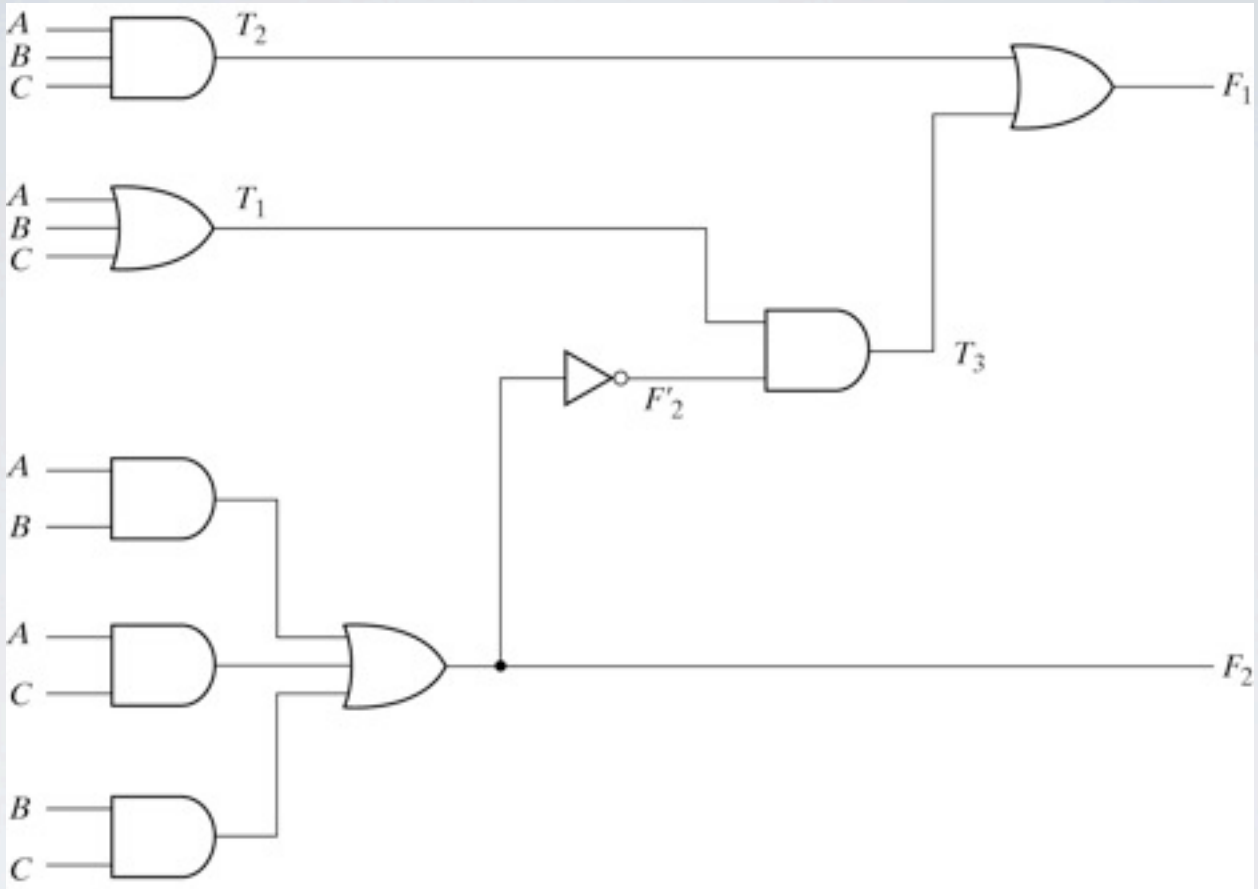


Fig. 4-2 Logic Diagram for Analysis Example

You can use intermediate variables to construct the boolean Functions from a complex logic diagram.

Table 4-2
Truth Table for Code-Conversion Example

Input BCD				Output Excess-3 Code			
A	*B*	*C*	*D*	*w*	*x*	*y*	*z*
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Table 4-2 BCD to Excess-3 Code

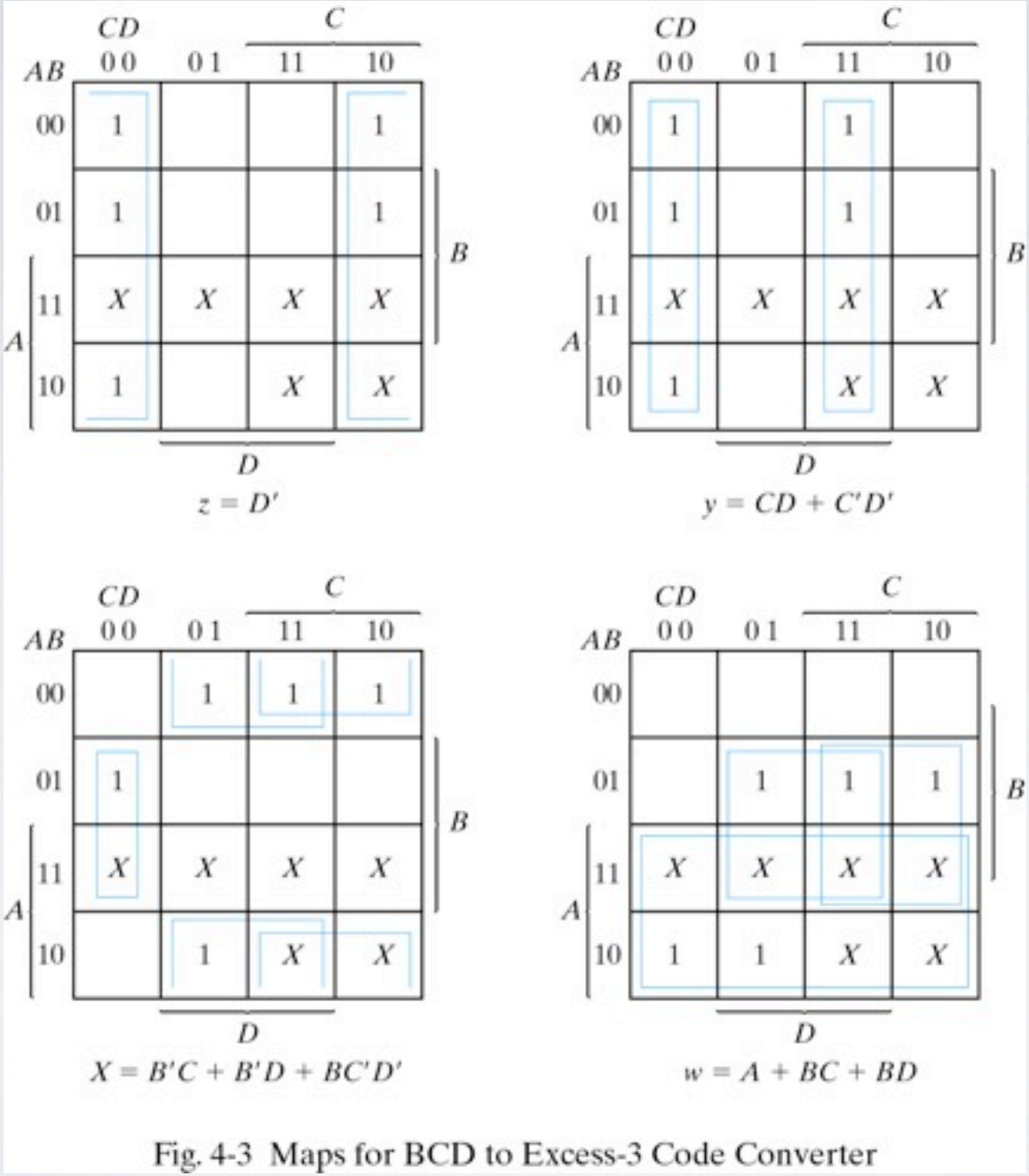


Fig. 4-3 Maps for BCD to Excess-3 Code Converter

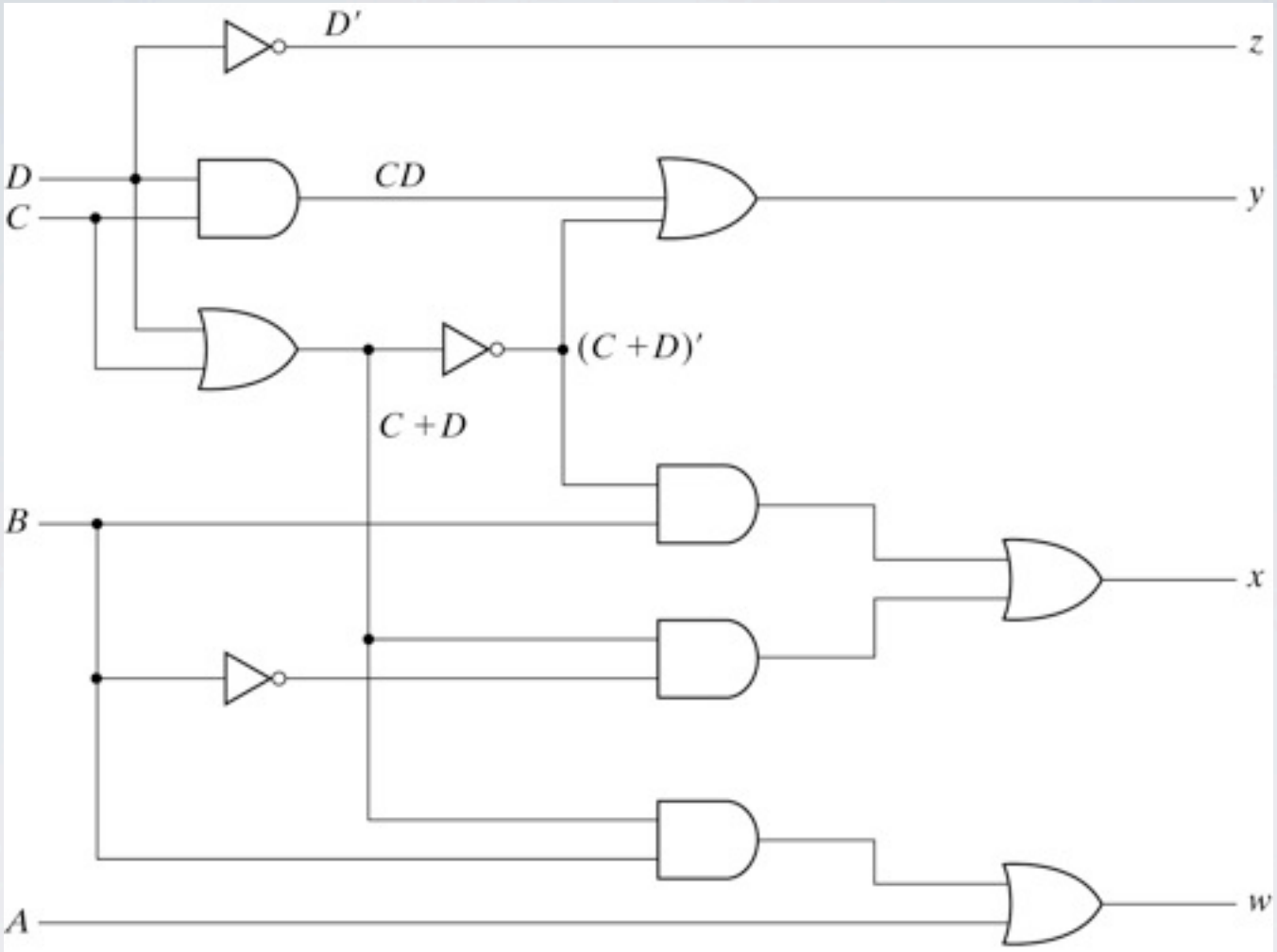
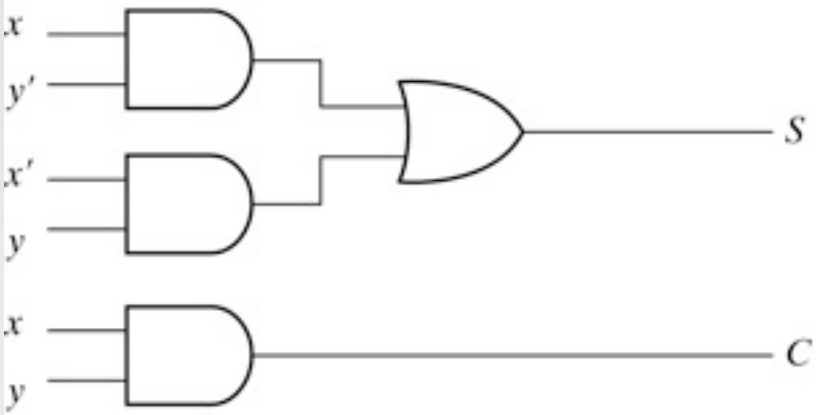


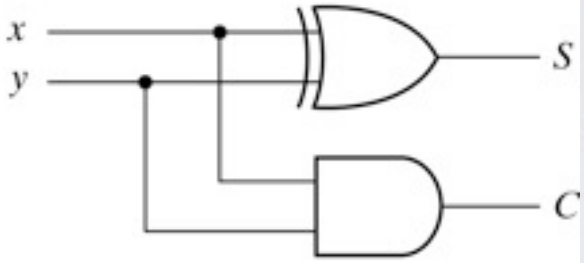
Fig. 4-4 Logic Diagram for BCD to Excess-3 Code Converter

Table 4-3
Half Adder

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



(a) $S = xy' + x'y$
$C = xy$

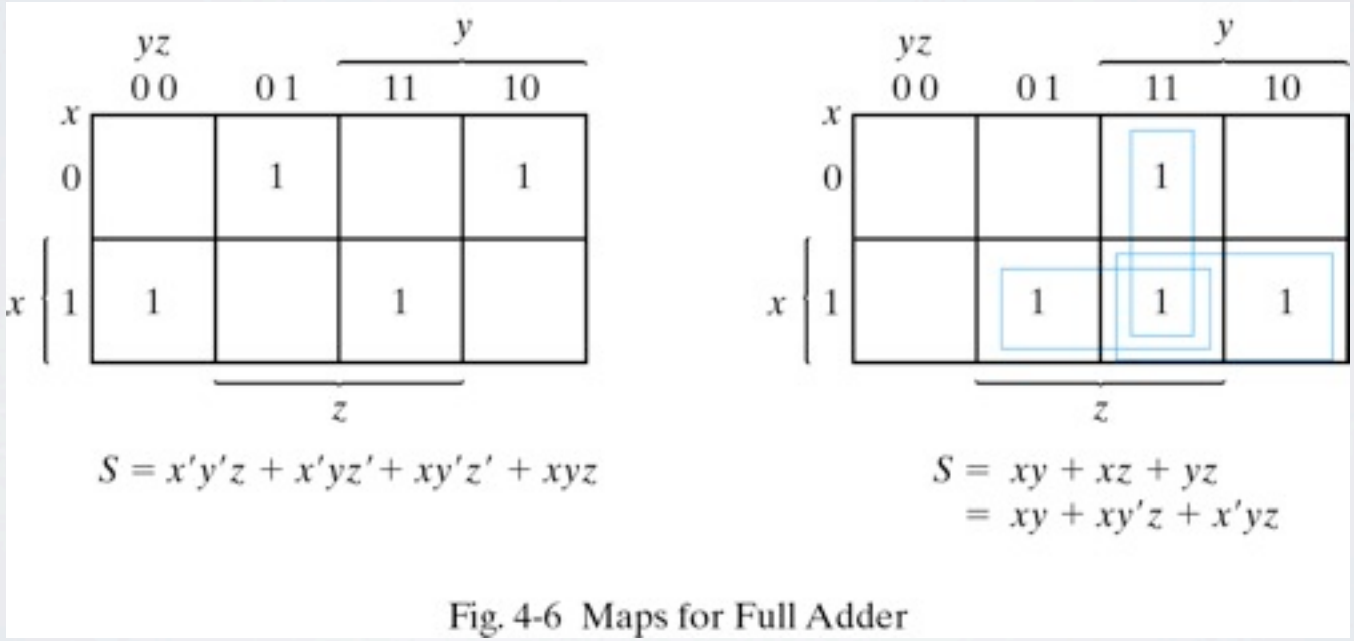


(b) $S = x \oplus y$
$C = xy$

Fig. 4-5 Implementation of Half-Adder

Table 4-4
Full Adder

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



$S = x'y'z + x'yz' + xy'z' + xyz$

$S = xy + xz + yz$
$= xy + xy'z + x'yz$

Fig. 4-6 Maps for Full Adder

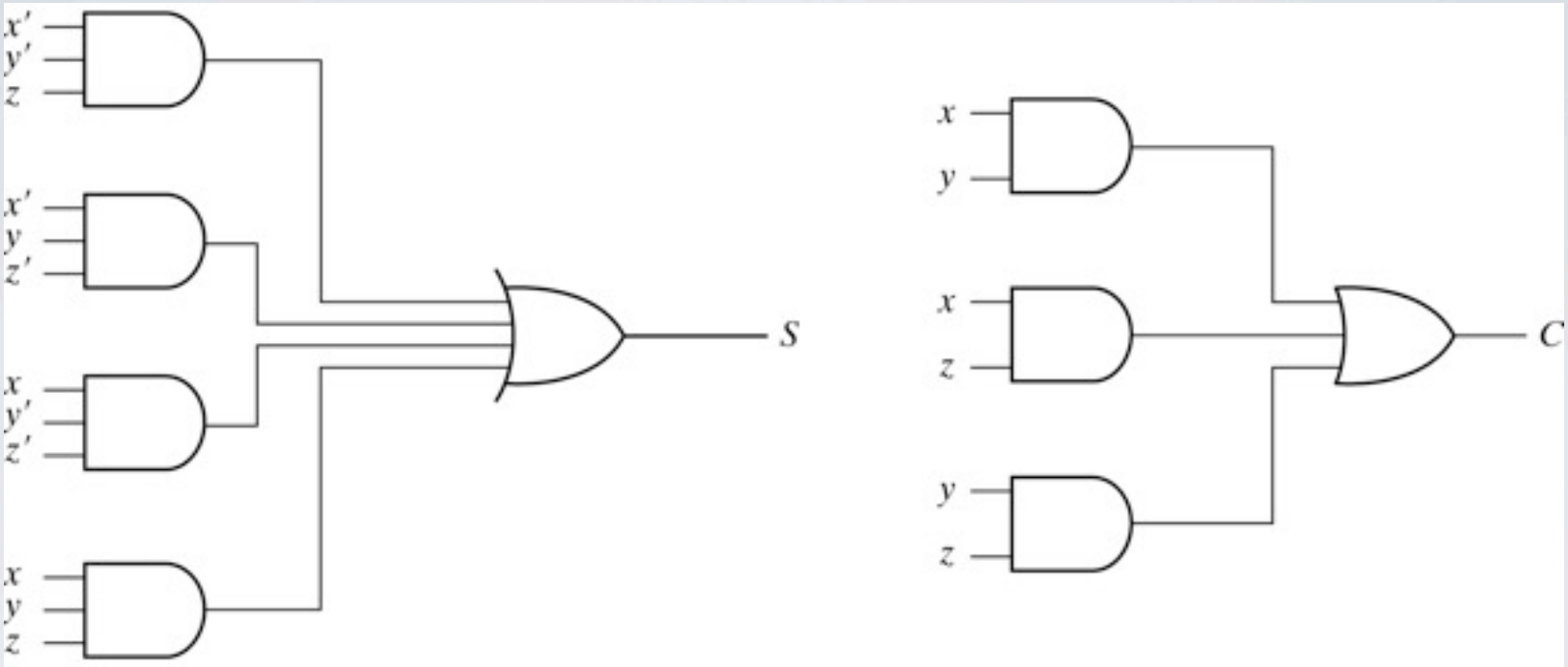


Fig. 4-7 Implementation of Full Adder in Sum of Products

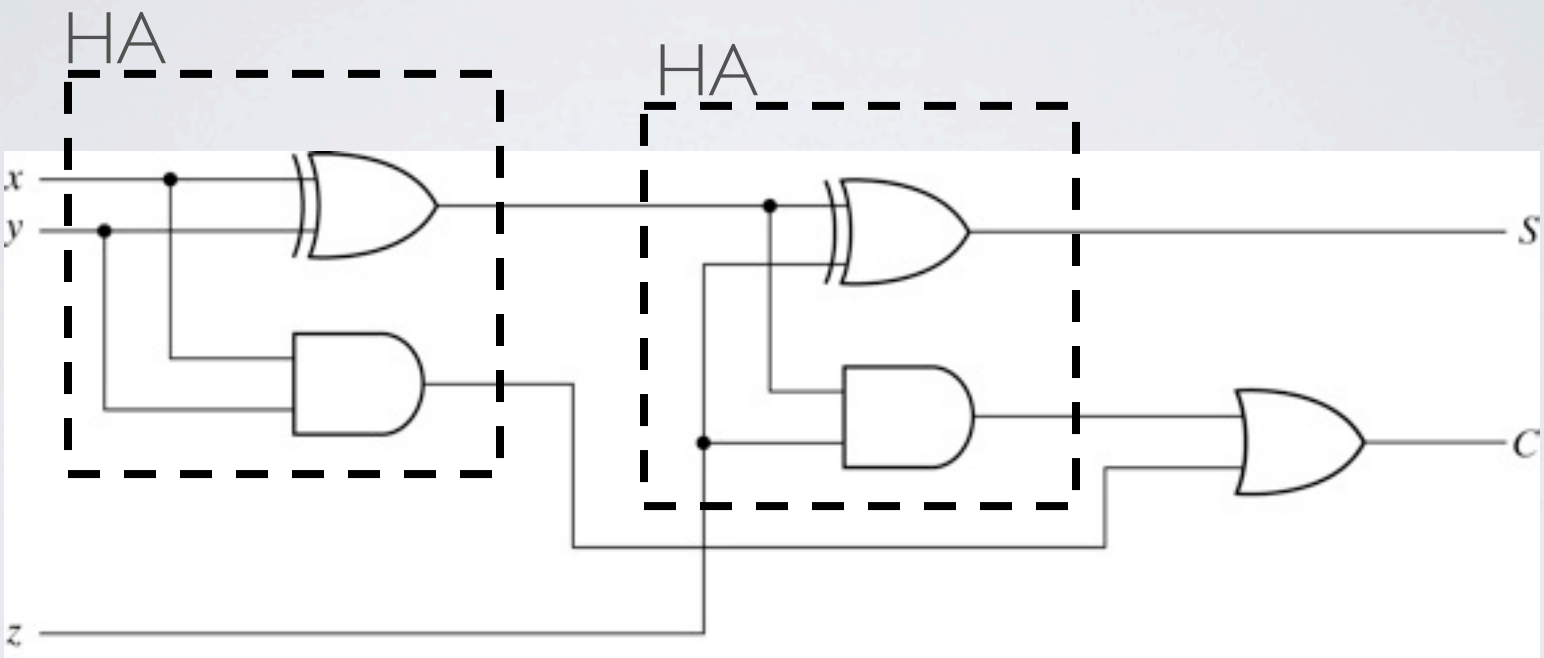


Fig. 4-8 Implementation of Full Adder with Two Half Adders and an OR Gate

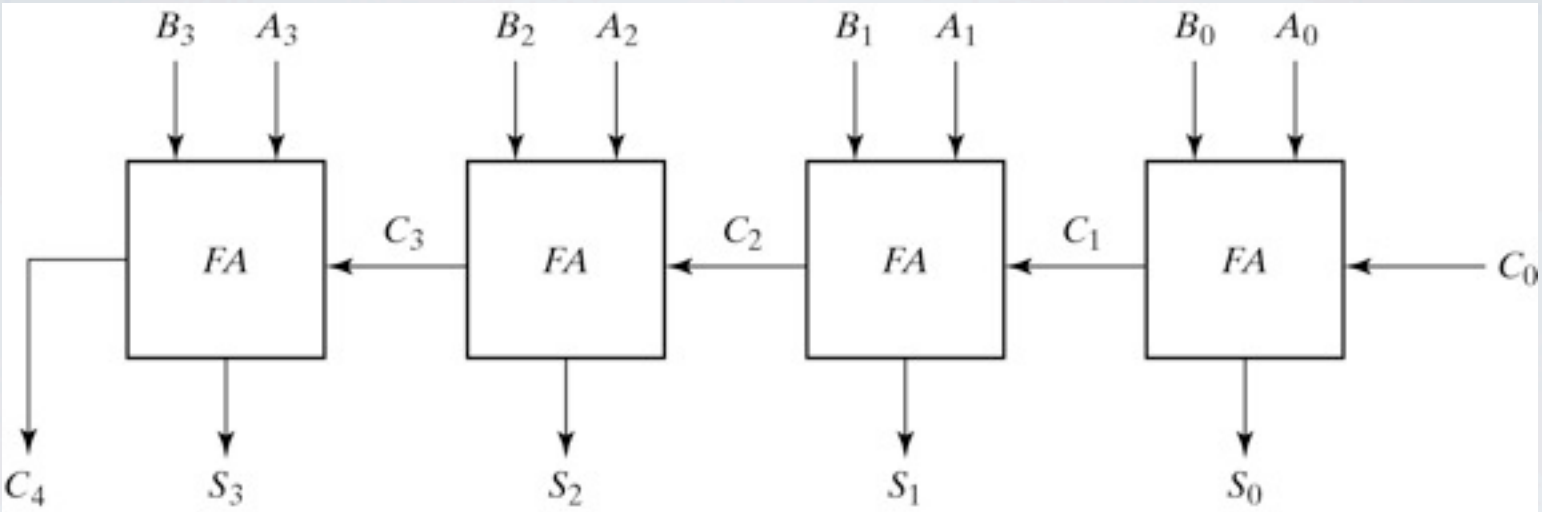


Fig. 4-9 4-Bit Adder

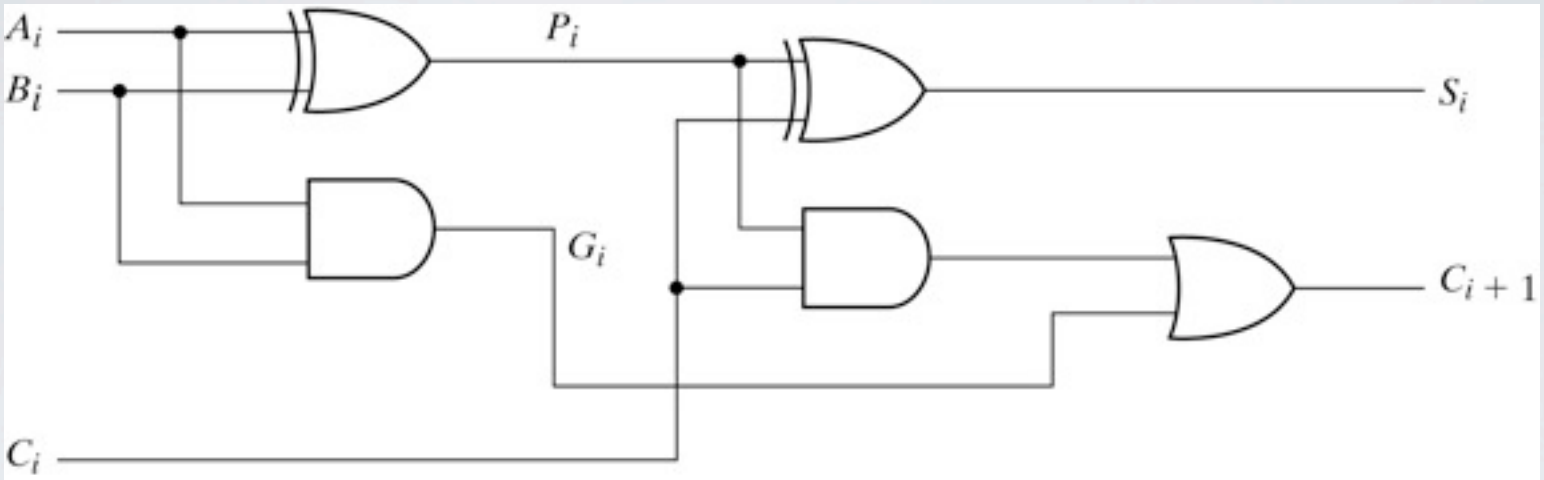


Fig. 4-10 Full Adder with P and G Shown

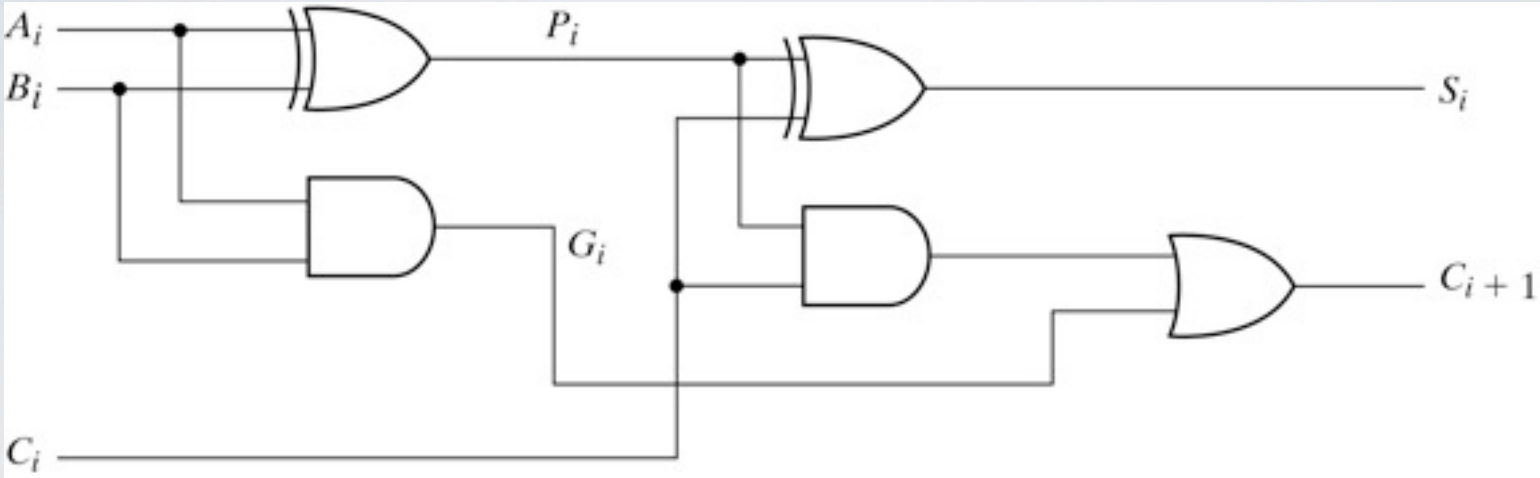


Fig. 4-10 Full Adder with P and G Shown

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + P_i C_i$$

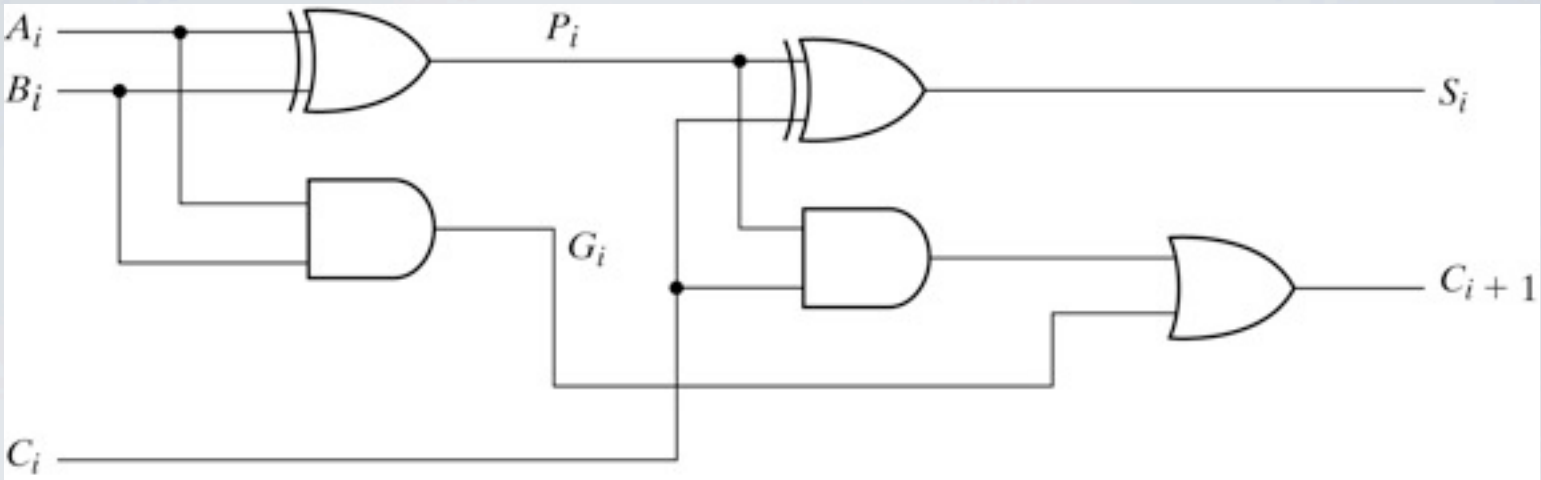


Fig. 4-10 Full Adder with P and G Shown

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + P_i C_i$$

C_0 = input carry

$$C_1 = G_0 + P_0 C_0$$

$$C_2 = G_1 + P_1 C_1 = G_1 + P_1(G_0 + P_0 C_0) = G_1 + P_1 G_0 + P_1 P_0 C_0$$

$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$$

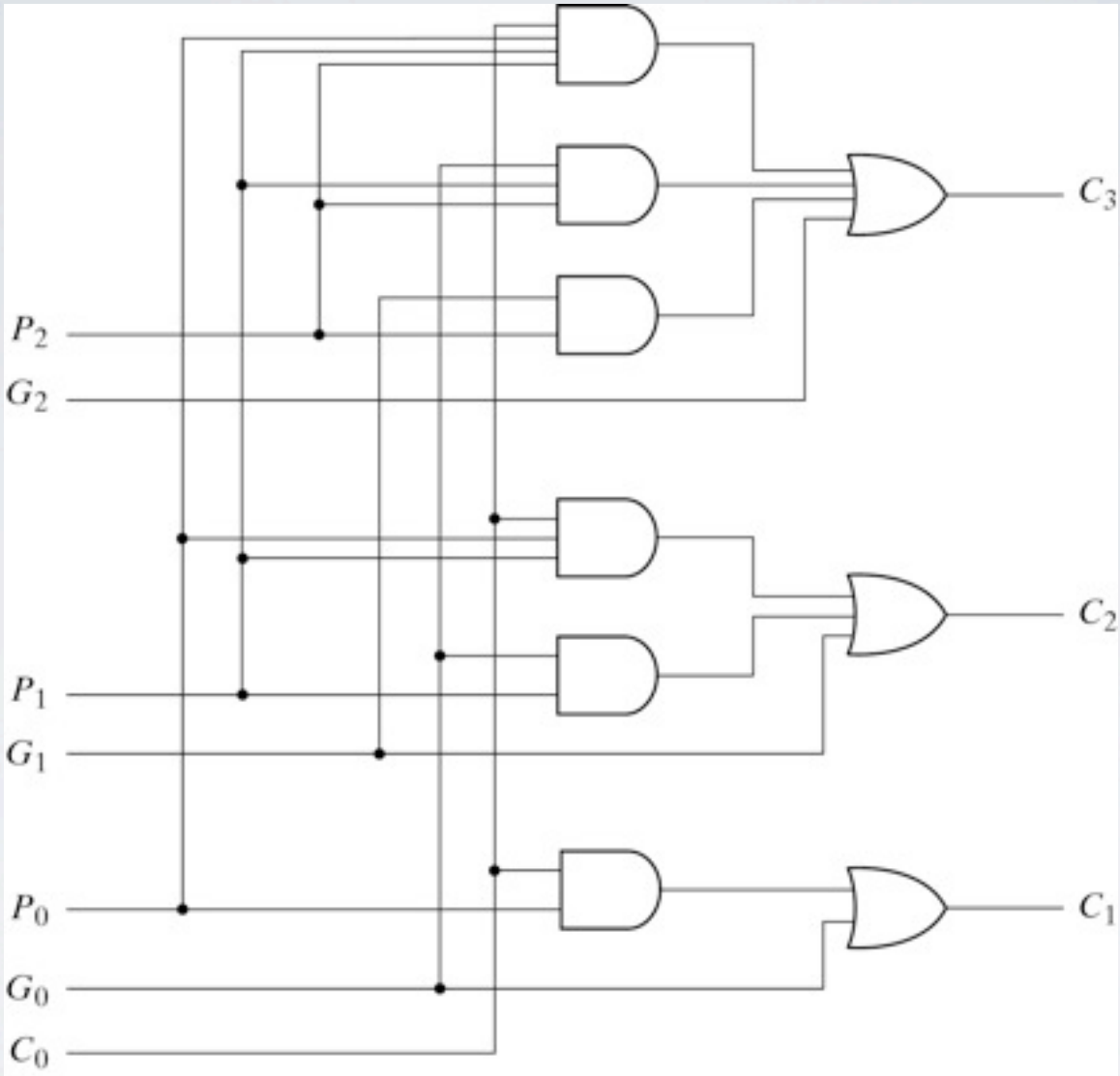


Fig. 4-11 Logic Diagram of Carry Lookahead Generator

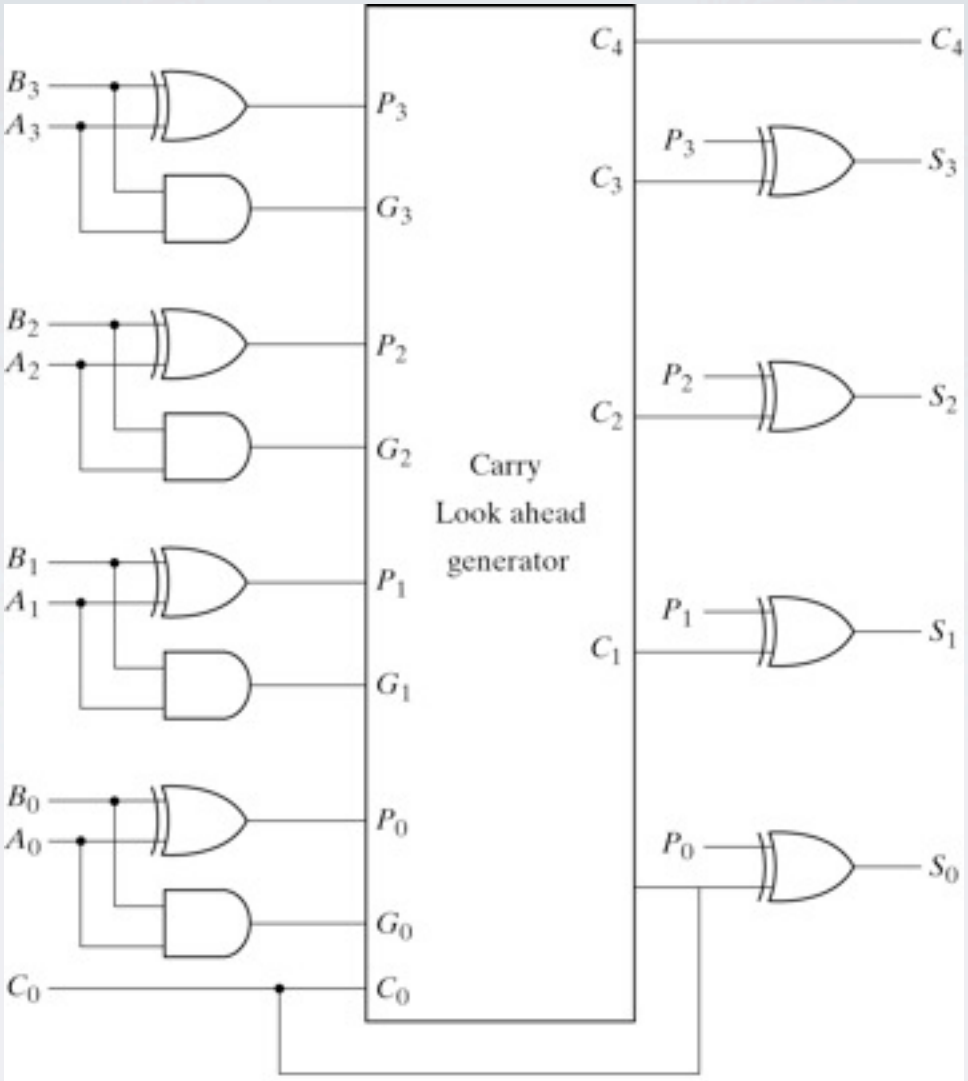


Fig. 4-12 4-Bit Adder with Carry Lookahead

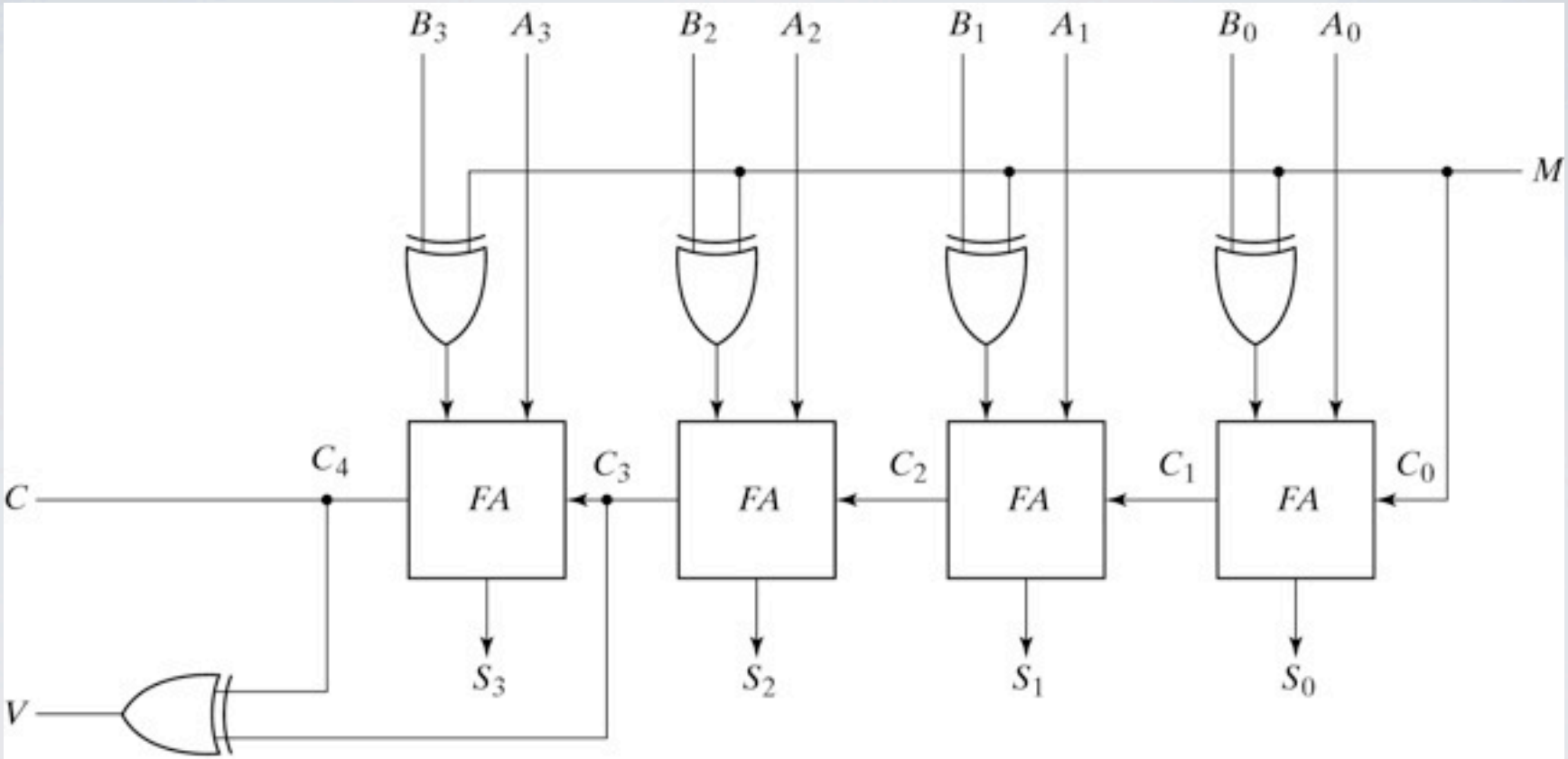


Fig. 4-13 4-Bit Adder Subtractor

M=1 complements the B-bits and adds 1, thus forming the 2's complement of B

carries:	0	1		carries:	1	0	
+70		0	1000110	−70		1	0111010
+80		0	1010000	−80		1	0110000
+150		1	0010110	−150		0	1101010

overflow occurs if:

For unsigned numbers: carry out of msb

for Signed numbers: if carry into sign bit is different than carry out of sign bit

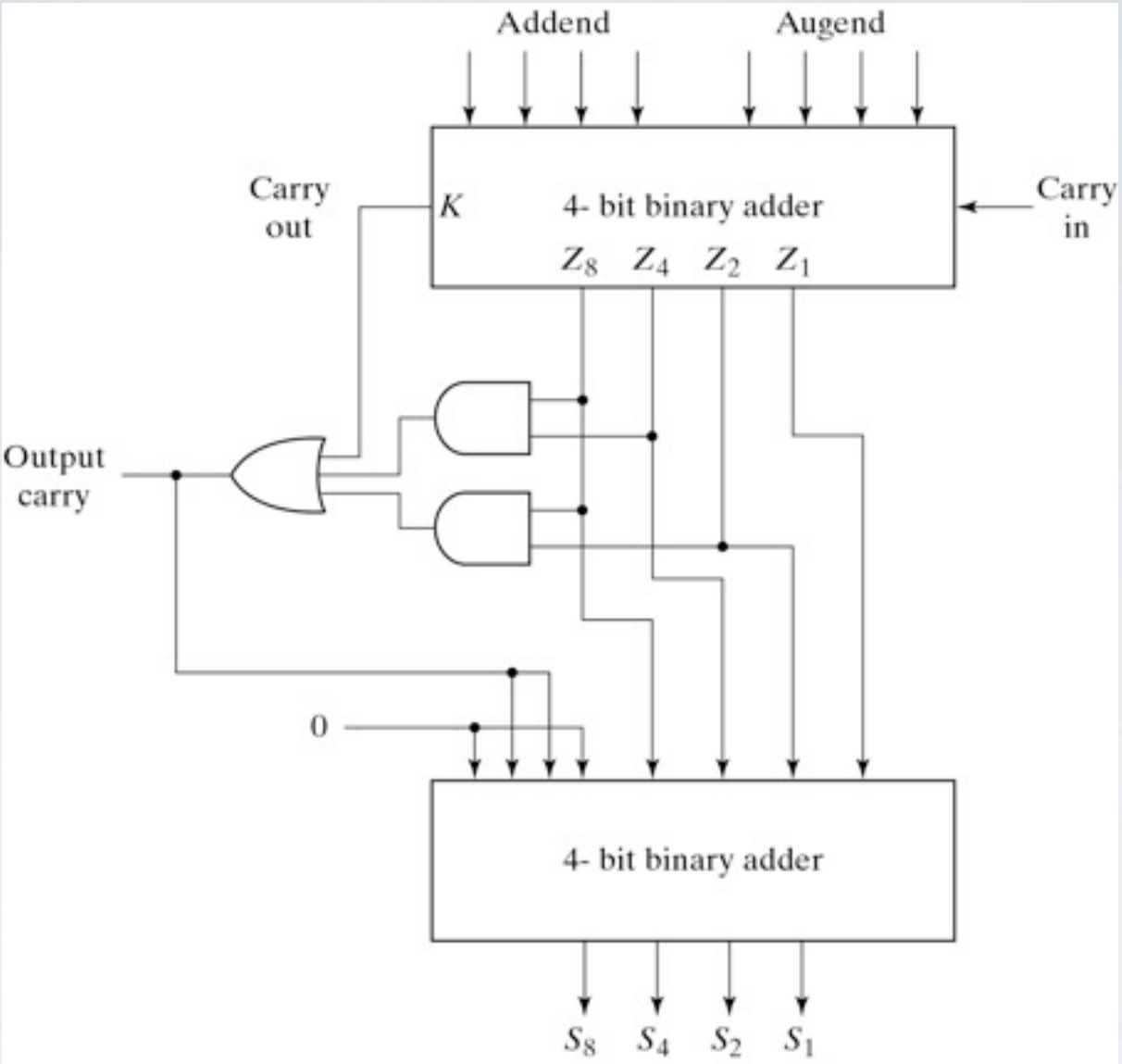


Fig. 4-14 Block Diagram of a BCD Adder

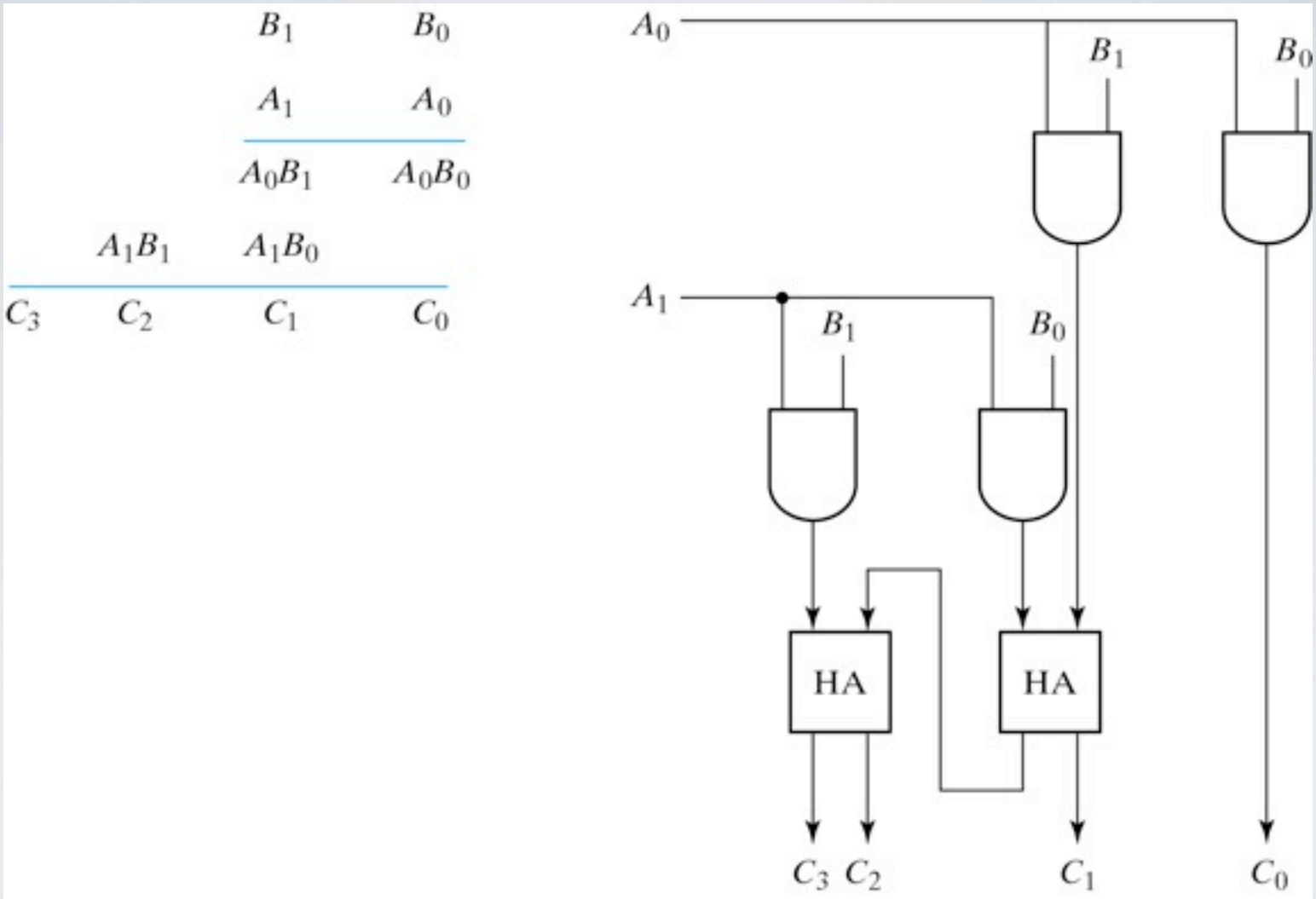


Fig. 4-15 2-Bit by 2-Bit Binary Multiplier

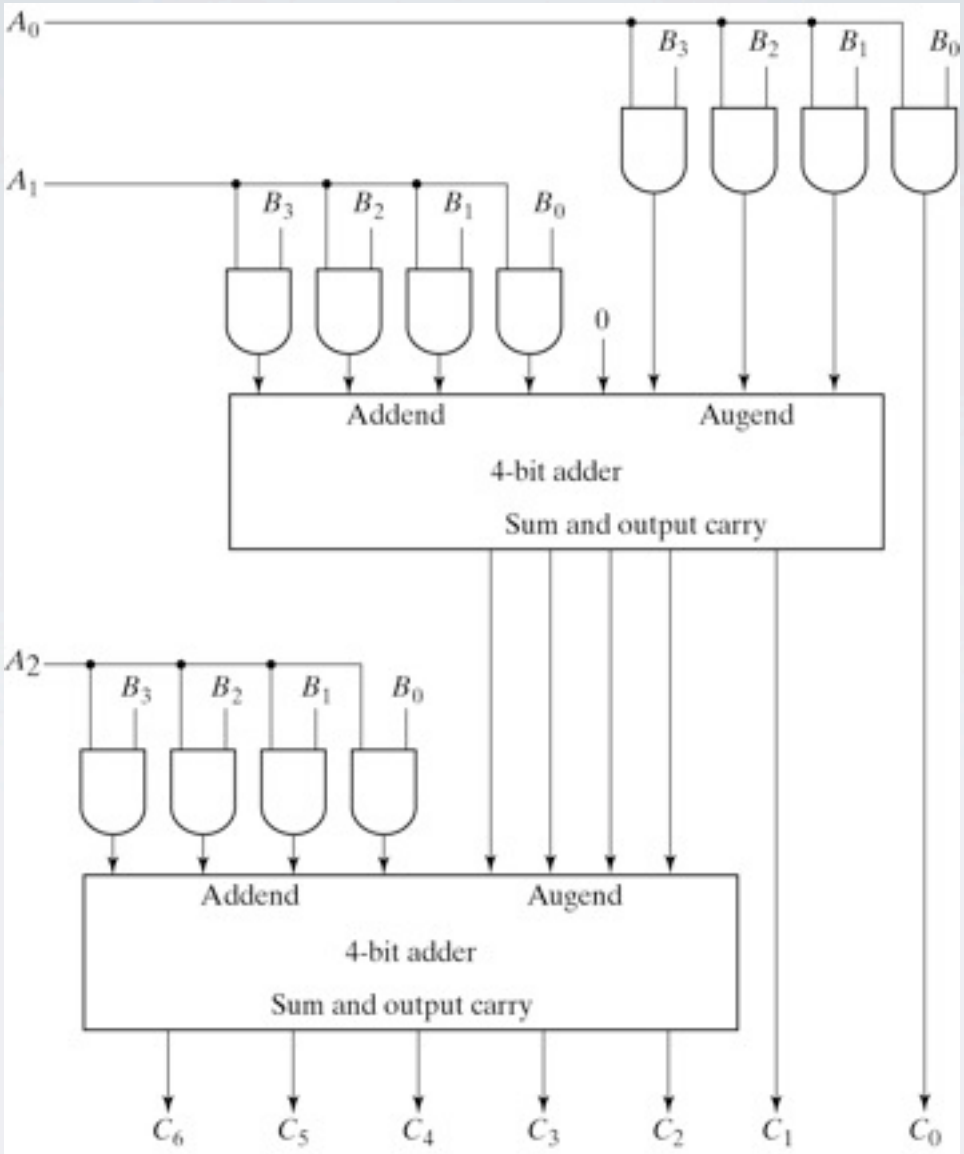


Fig. 4-16 4-Bit by 3-Bit Binary Multiplier

MAGNITUDE COMPARATOR

$$A = A_3A_2A_1A_0$$
$$B = B_3B_2B_1B_0$$

$$x_i = A_iB_i + A_i'B_i' \qquad \text{for } i = 0, 1, 2, 3$$
$$(A = B) = x_3x_2x_1x_0$$

$$(A > B) = A_3B_3' + x_3A_2B_2' + x_3x_2A_1B_1' + x_3x_2x_1A_0B_0'$$
$$(A < B) = A_3'B_3 + x_3A_2'B_2 + x_3x_2A_1'B_1 + x_3x_2x_1A_0'B_0$$

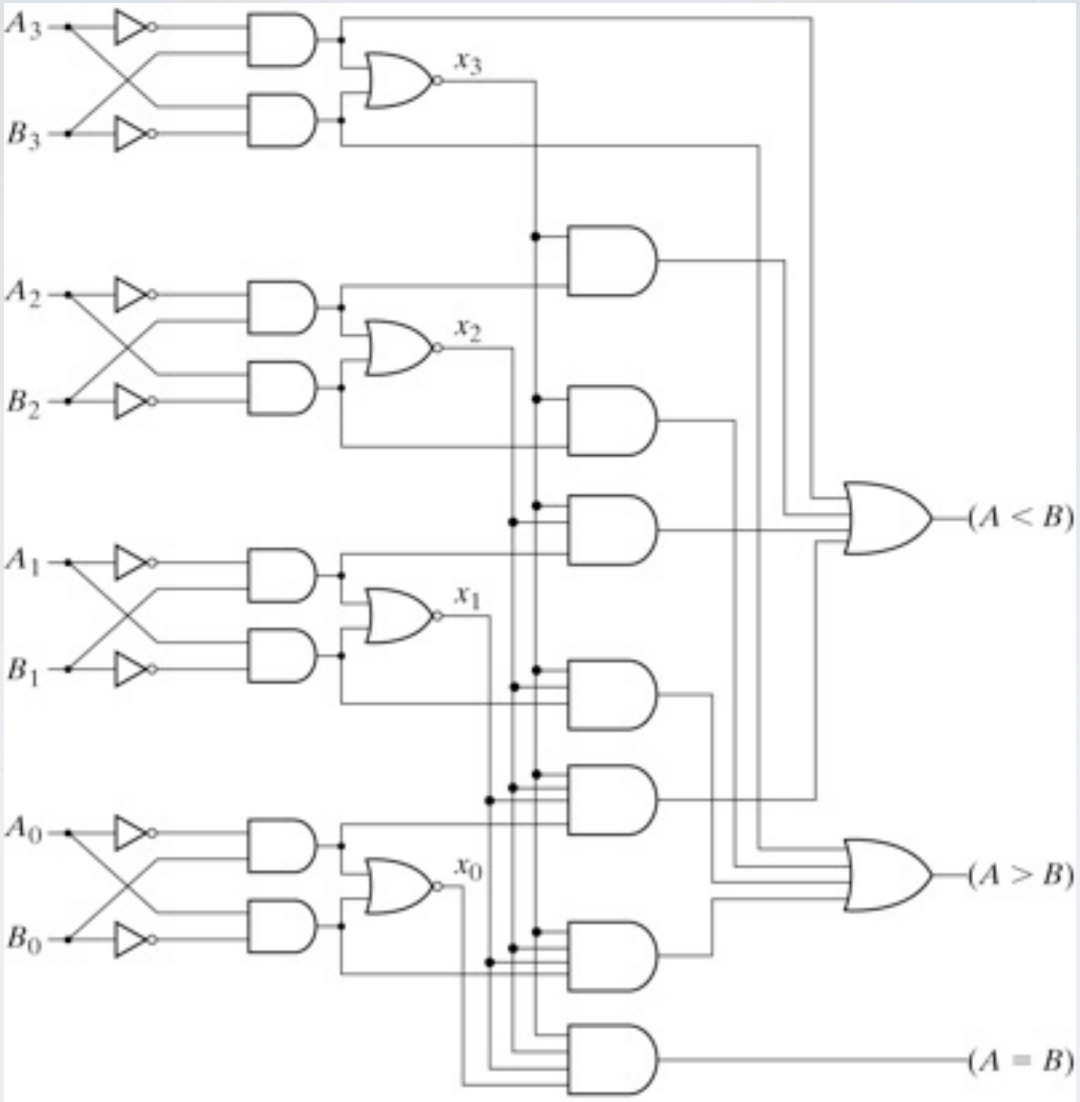


Fig. 4-17 4-Bit Magnitude Comparator