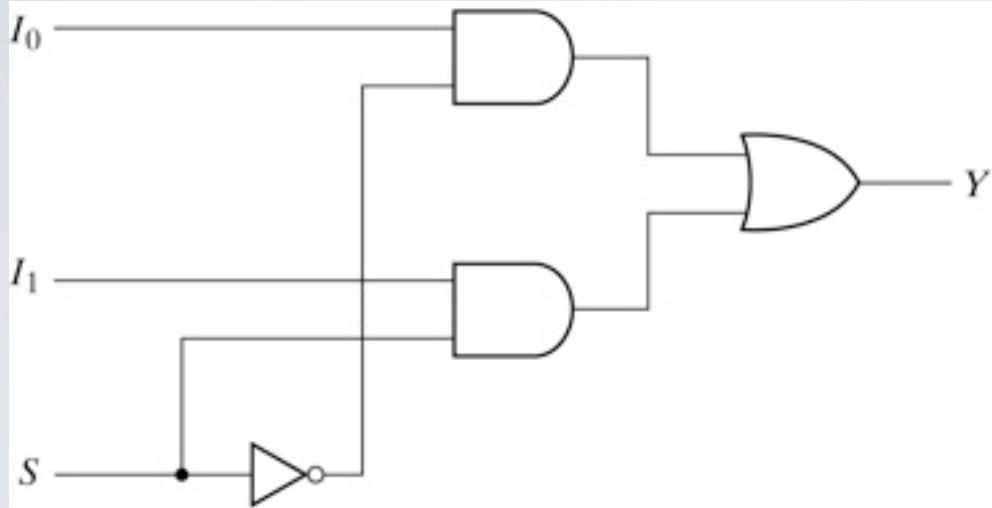# Multiplexers and Decoders
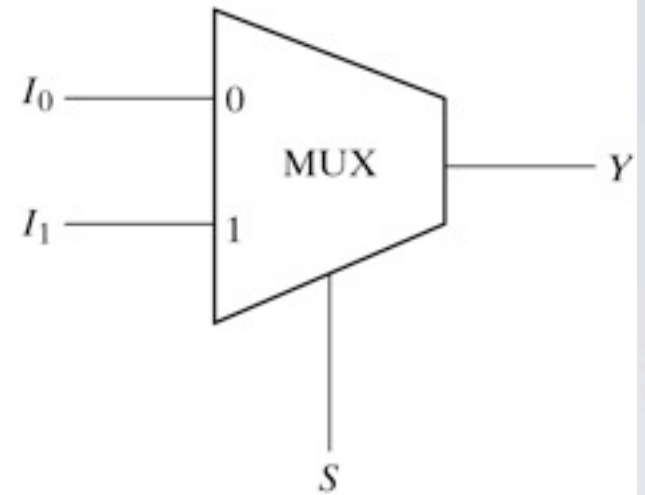
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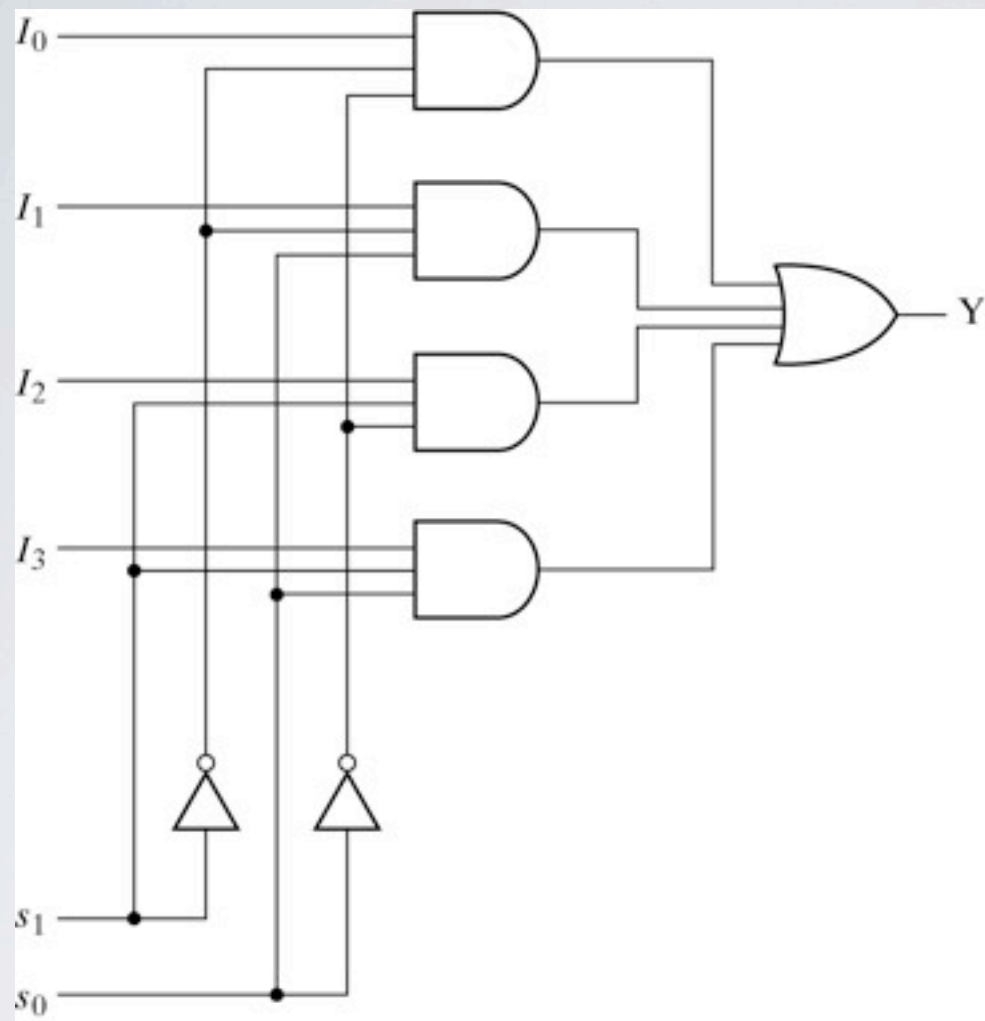
(a) Logic diagram

(b) Block diagram

Fig. 4-24 2-to-1-Line Multiplexer

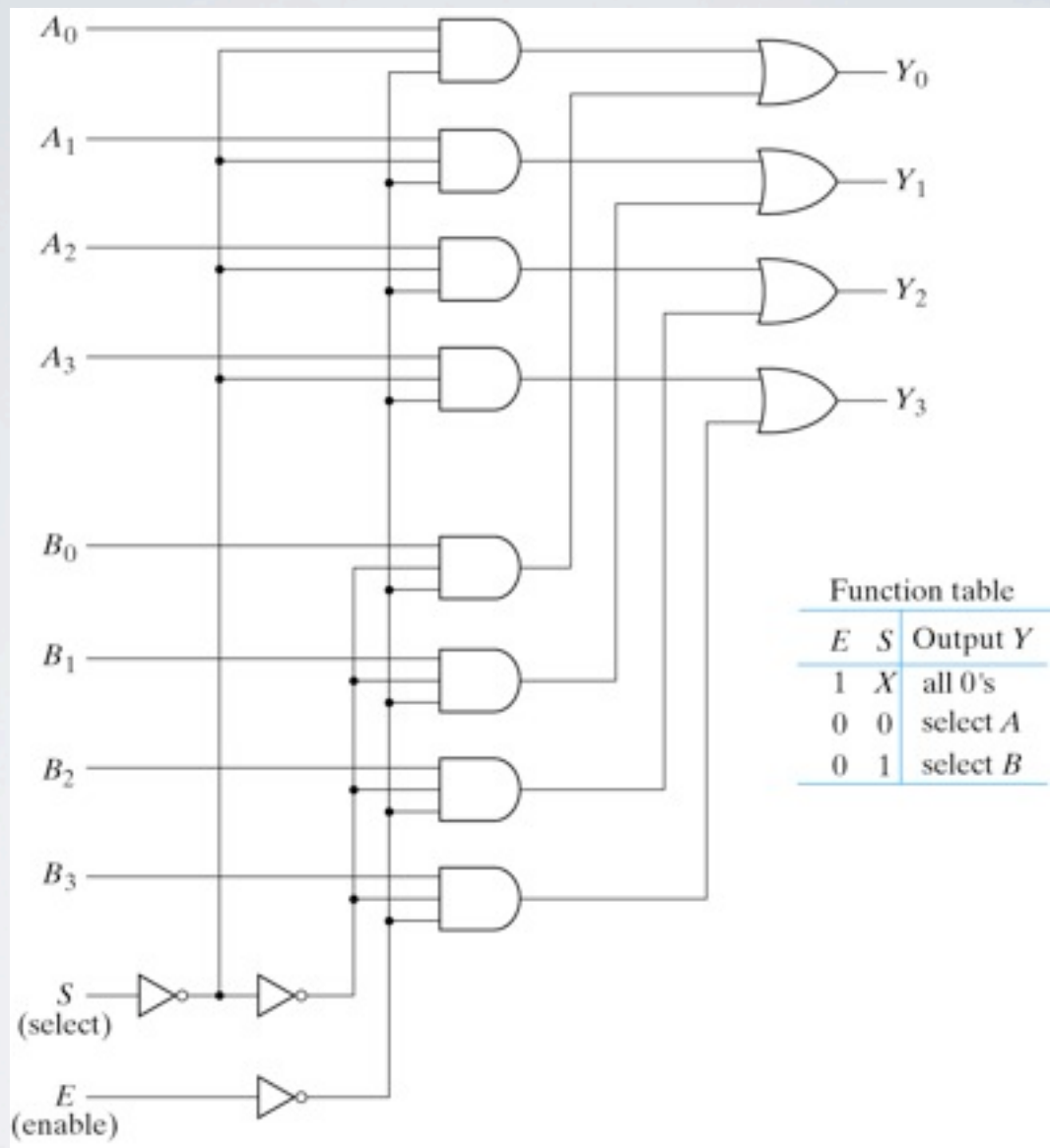| s_1	s_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

(b) Function table

(a) Logic diagram

Fig. 4-25 4-to-1-Line Multiplexer

Fig. 4-26 Quadruple 2-to-1-Line Multiplexer

Function table

E	S	Output Y
1	X	all 0's
0	0	select A
0	1	select B

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x	y	z	F	
0	0	0	0	
0	0	1	1	$F = z$
0	1	0	1	
0	1	1	0	$F = z'$
1	0	0	0	
1	0	1	0	$F = 0$
1	1	0	1	
1	1	1	1	$F = 1$

(a) Truth table

4×1 MUX

y —— S_0
x —— S_1

z —— 0
z' —— 1
0 —— 2
1 —— 3

—— F
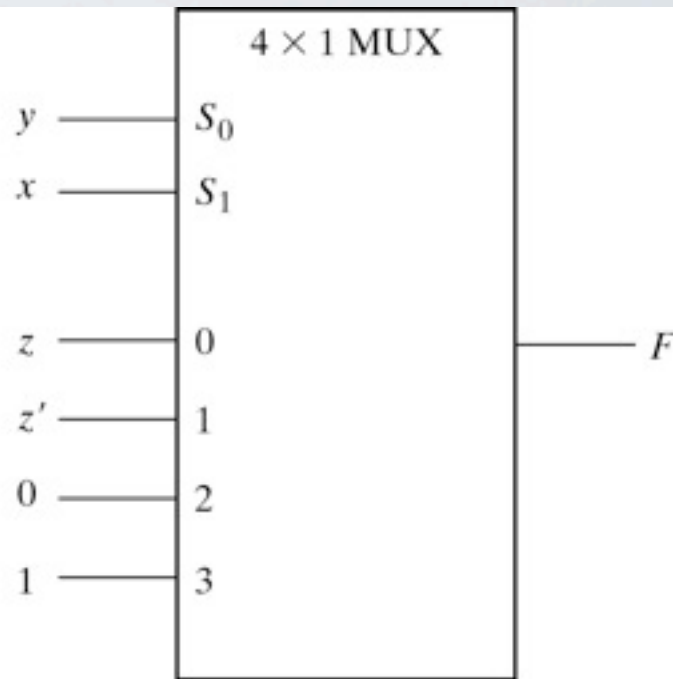
(b) Multiplexer implementation

Fig. 4-27 Implementing a Boolean Function with a Multiplexer

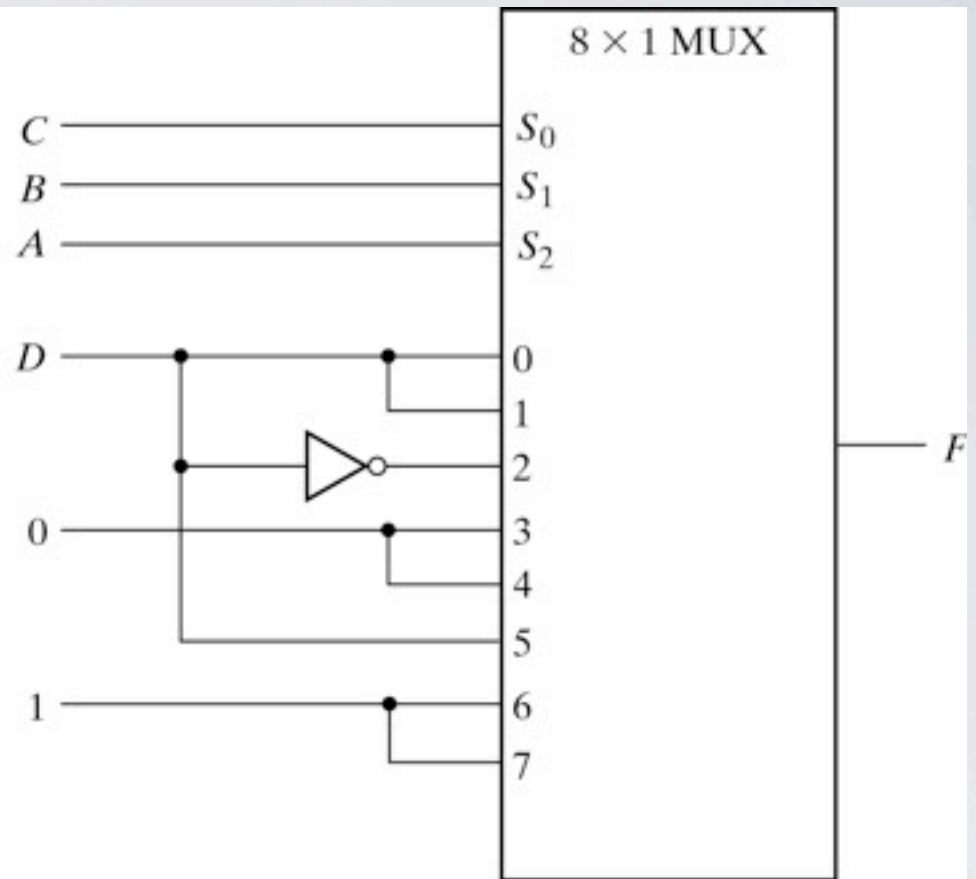| A	B	C	D	F	
0	0	0	0	0	F = D
0	0	0	1	1	
0	0	1	0	0	F = D
0	0	1	1	1	
0	1	0	0	1	F = D'
0	1	0	1	0	
0	1	1	0	0	F = 0
0	1	1	1	0	
1	0	0	0	0	F = 0
1	0	0	1	0	
1	0	1	0	0	F = D
1	0	1	1	1	
1	1	0	0	1	F = 1
1	1	0	1	1	
1	1	1	0	1	F = 1
1	1	1	1	1	

Fig. 4-28 Implementing a 4-Input Function with a Multiplexer

Table 4-6
Truth Table of a 3-to-8-Line Decoder

Inputs			Outputs							
x	y	z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1
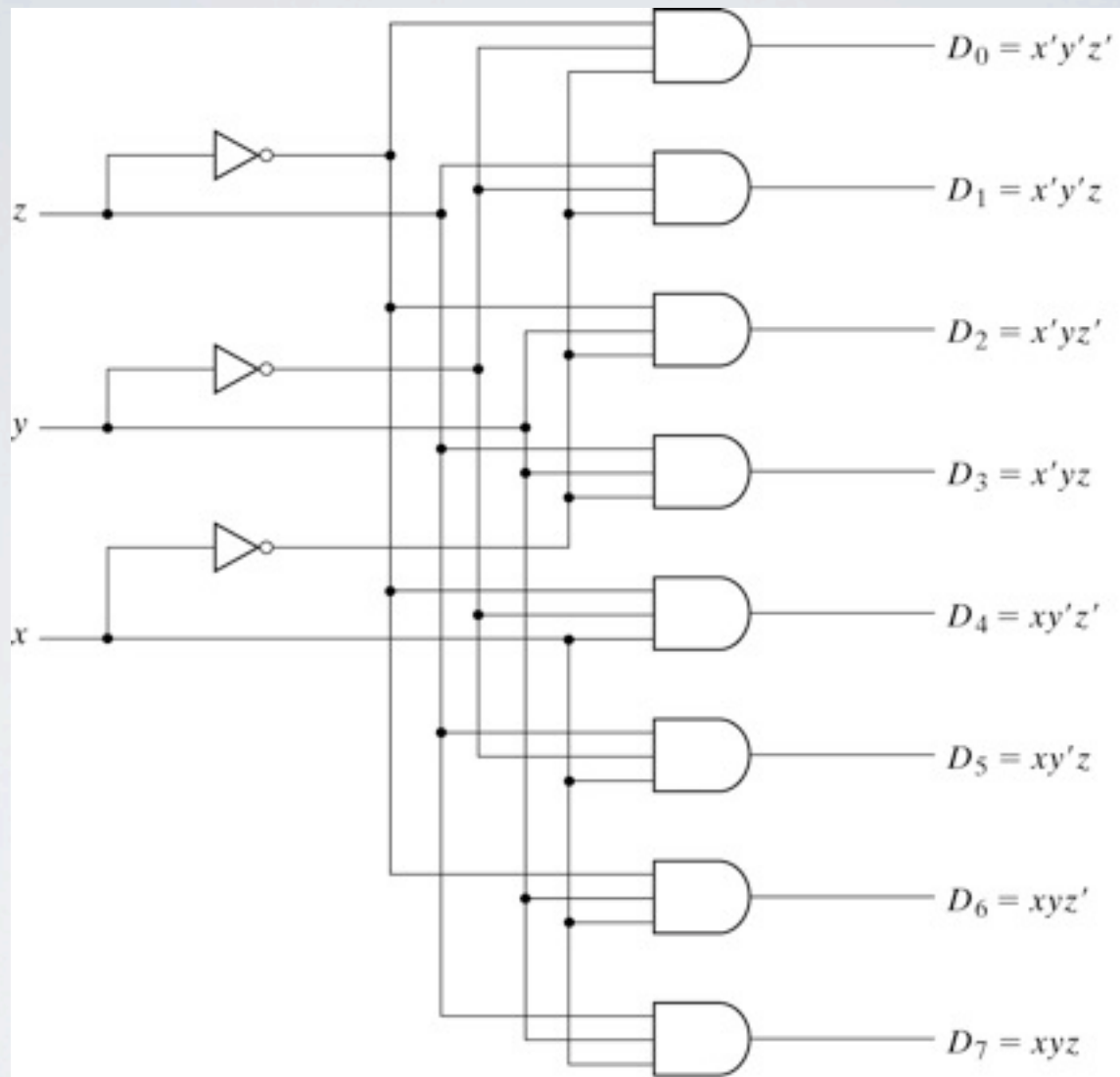
Fig. 4-18 3-to-8-Line Decoder

The labeled outputs of the decoder are:

$$D_0 = x'y'z'$$
$$D_1 = x'y'z$$
$$D_2 = x'yz'$$
$$D_3 = x'yz$$
$$D_4 = xy'z'$$
$$D_5 = xy'z$$
$$D_6 = xyz'$$
$$D_7 = xyz$$
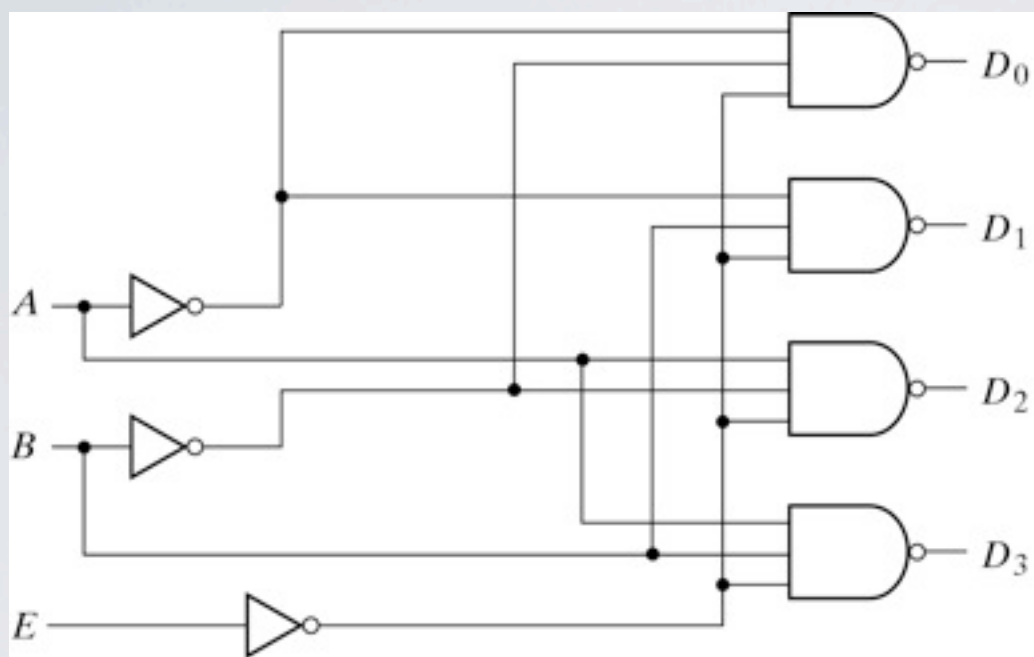
E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

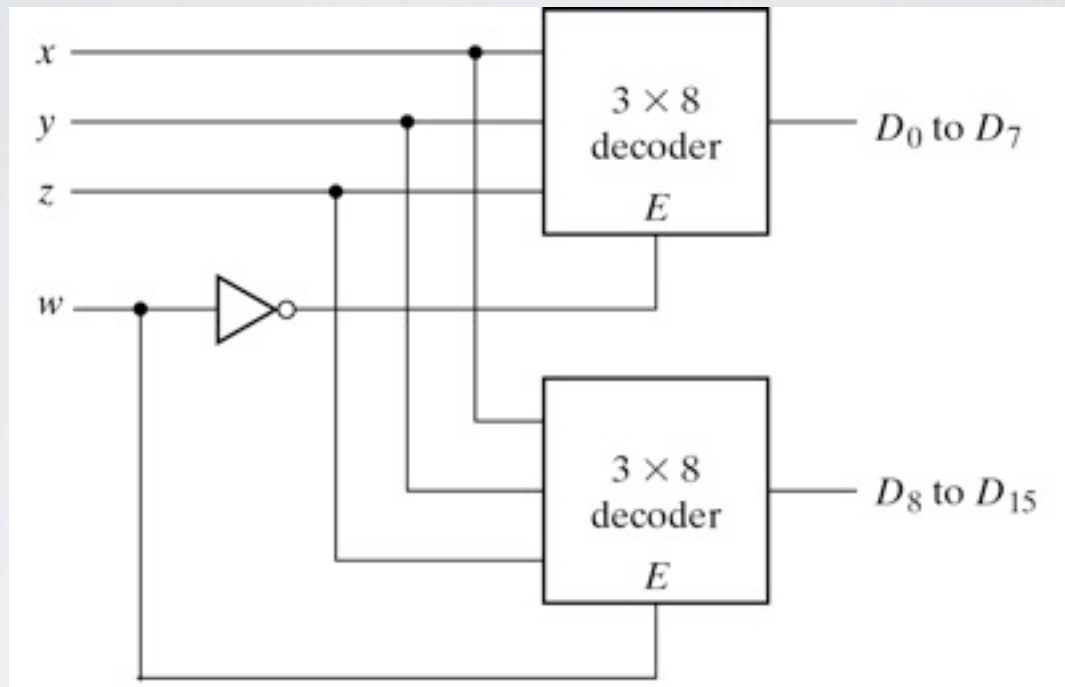(a) Logic diagram   (b) Truth table

Fig. 4-19 2-to-4-Line Decoder with Enable Input

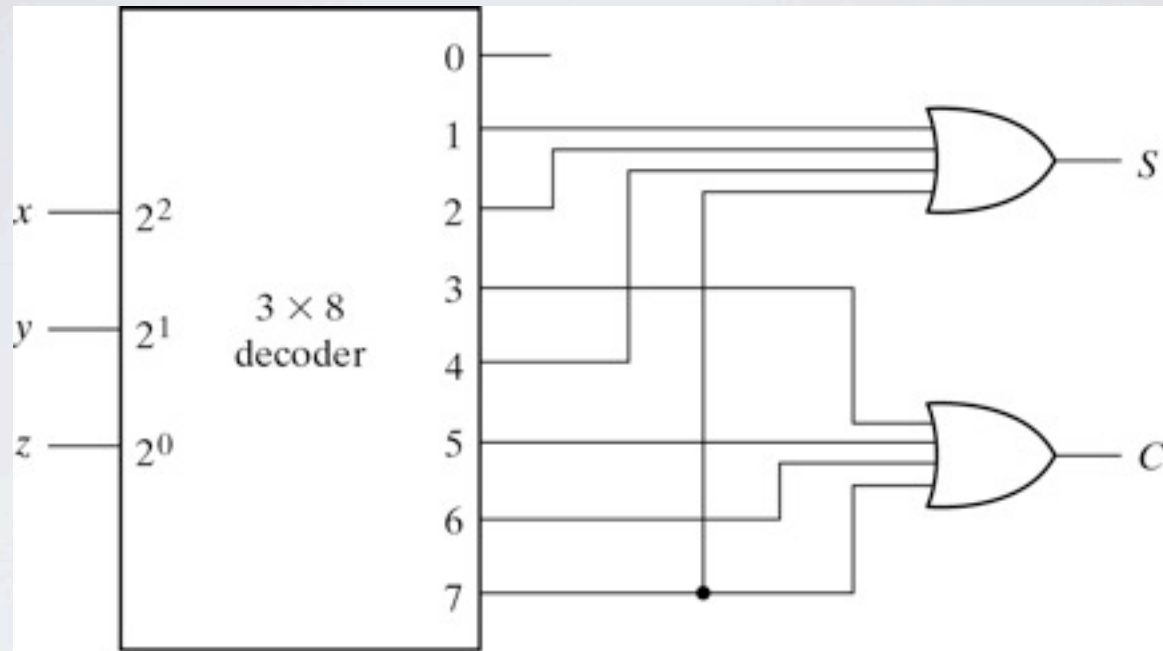Fig. 4-20 4 × 16 Decoder Constructed with Two 3 × 8 Decoders

Fig. 4-21 Implementation of a Full Adder with a Decoder

Table 4-7
Truth Table of Octal-to-Binary Encoder

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

D_0	D_1	D_2	D_3	x	y	V
0	0	0	0	X	X	0
1	0	0	0	0	0	1
X	1	0	0	0	1	1
X	X	1	0	1	0	1
X	X	X	1	1	1	1

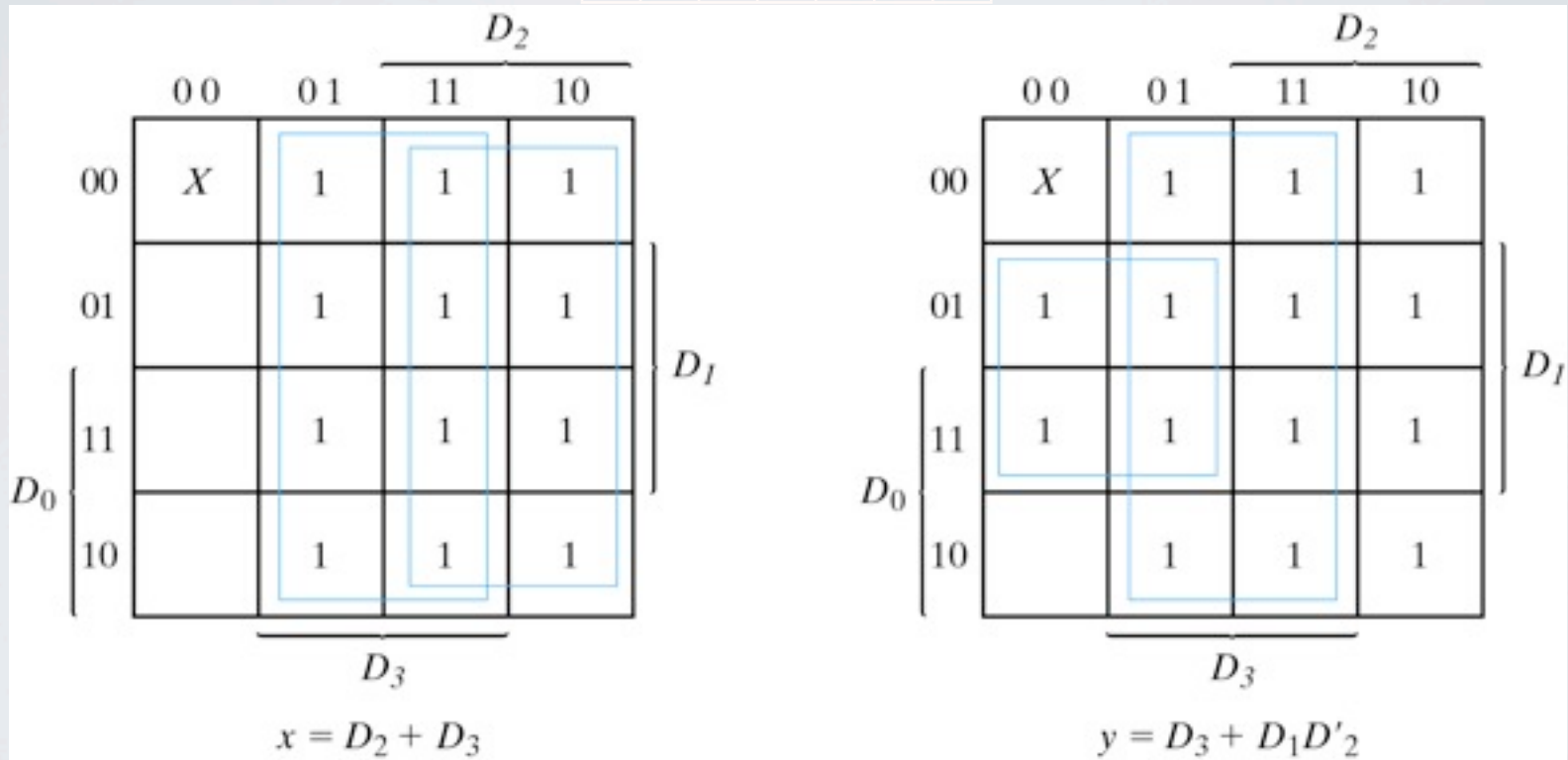$$x = D_2 + D_3$$

$$y = D_3 + D_1 D'_2$$
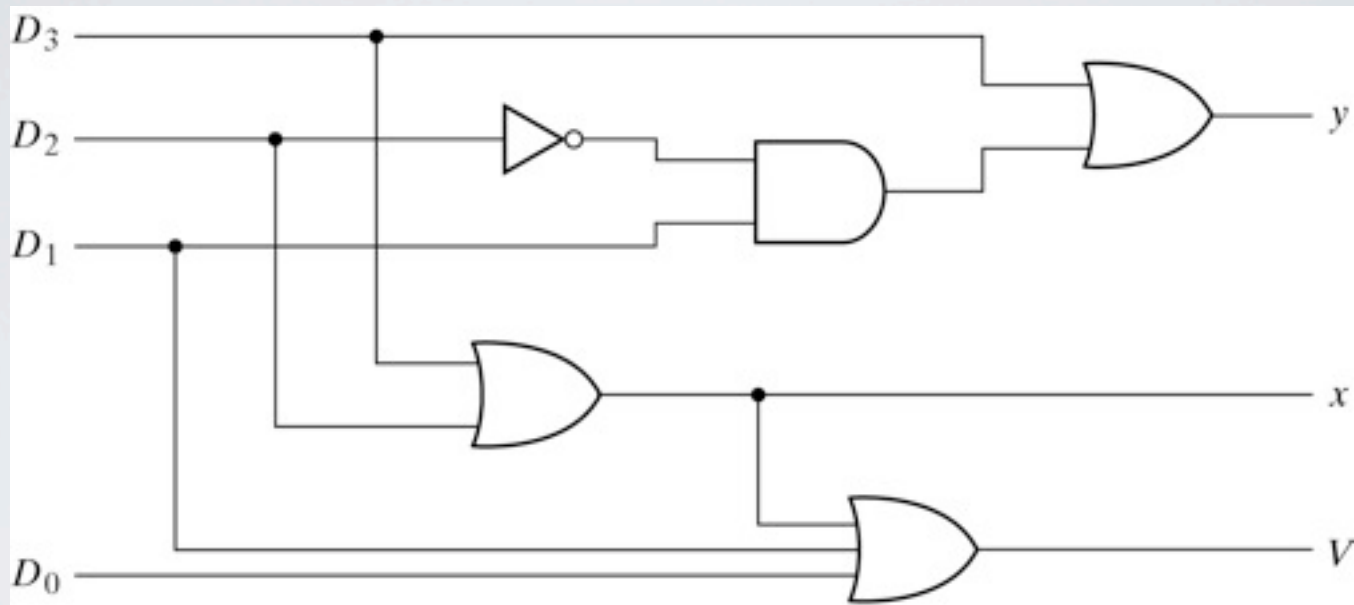
Fig. 4-22 Maps for a Priority Encoder

Fig. 4-23 4-Input Priority Encoder
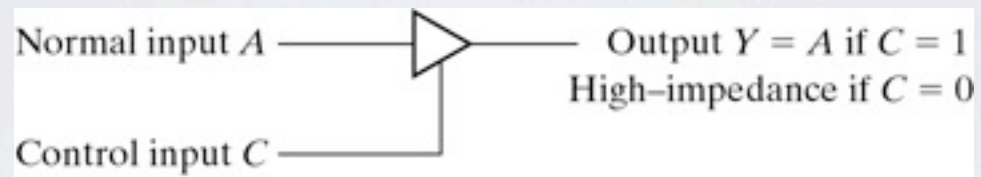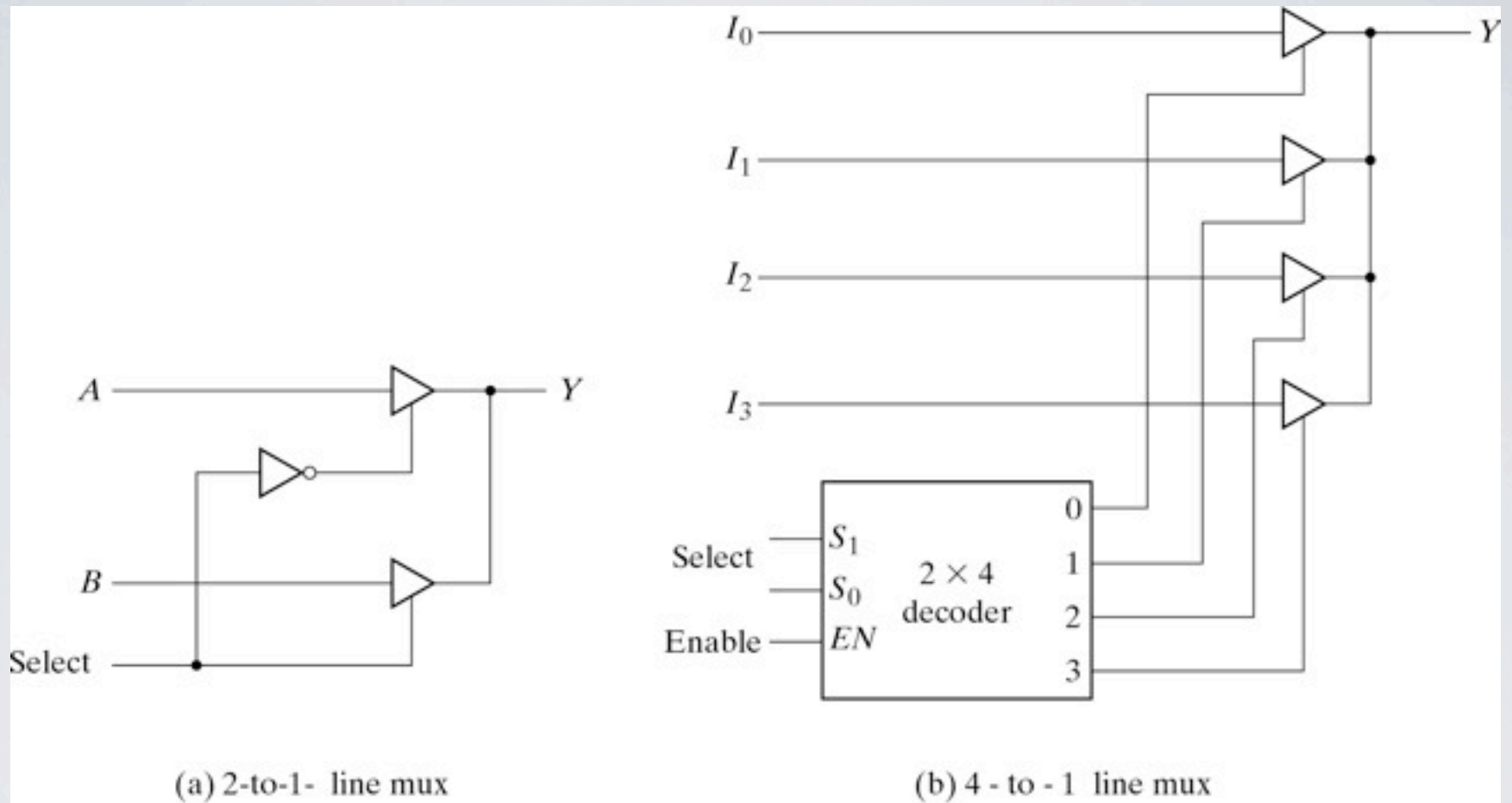
Fig. 4-29 Graphic Symbol for a Three-State Buffer

Normal input A → Output $Y = A$ if $C = 1$; High-impedance if $C = 0$

Control input C

(a) 2-to-1- line mux

(b) 4 - to - 1 line mux
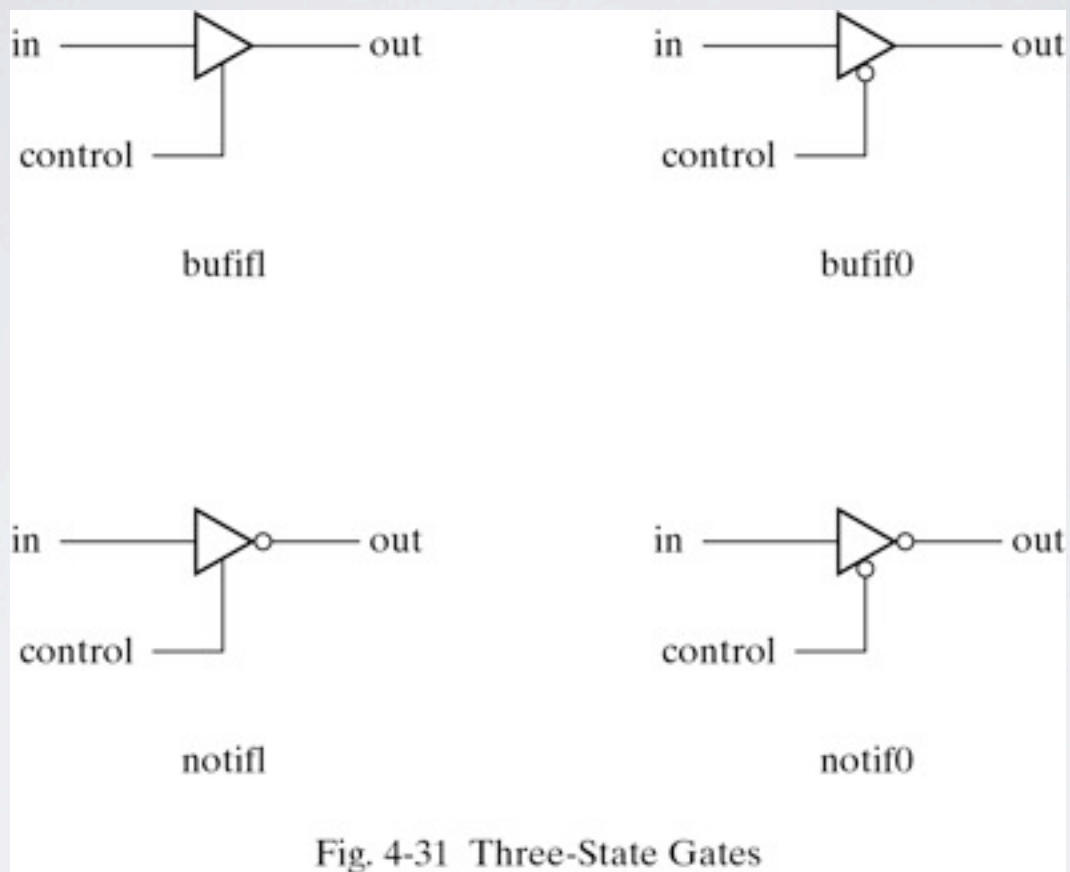
Fig. 4-30 Multiplexers with Three-State Gates

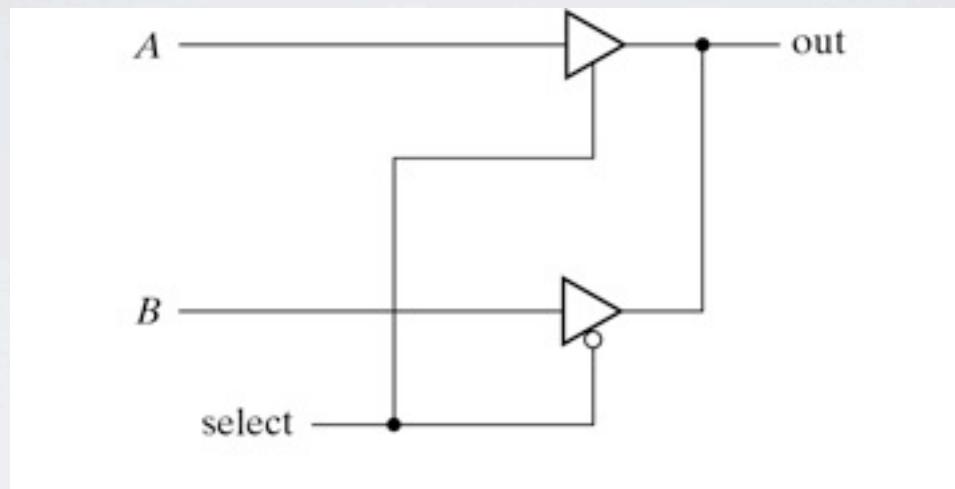Monday, March 5, 12

Fig. 4-31 Three-State Gates

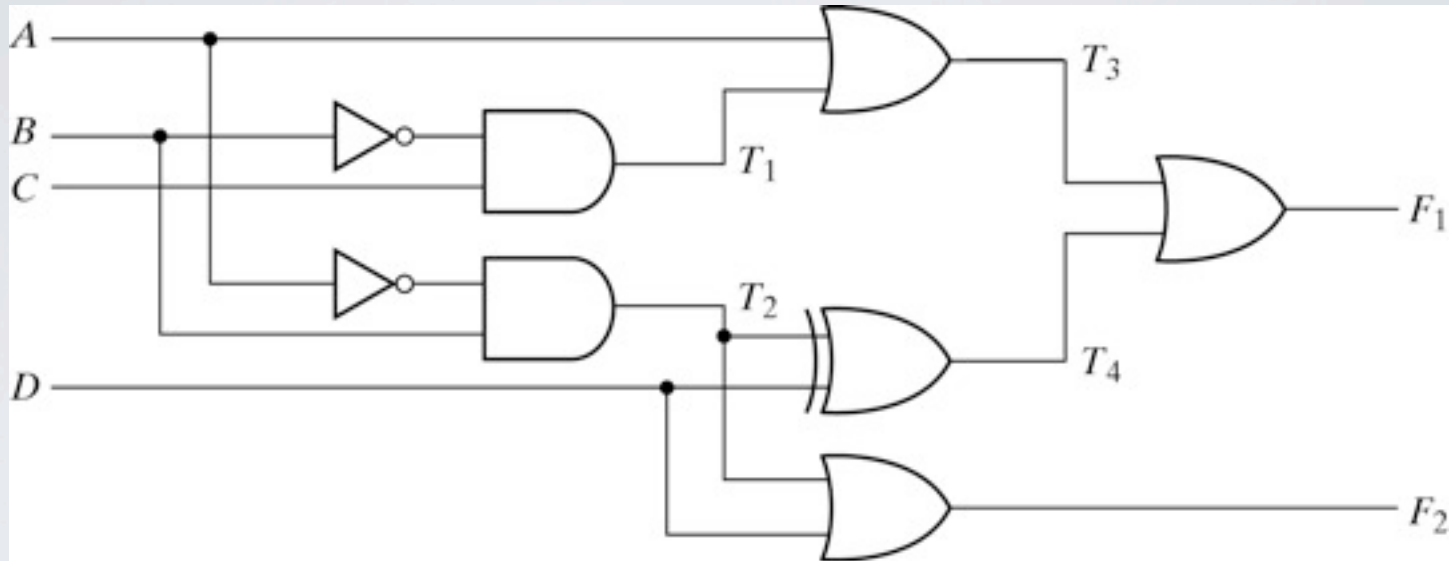Fig. 4-32 2-to-1-Line Multiplexer with Three-State Buffers
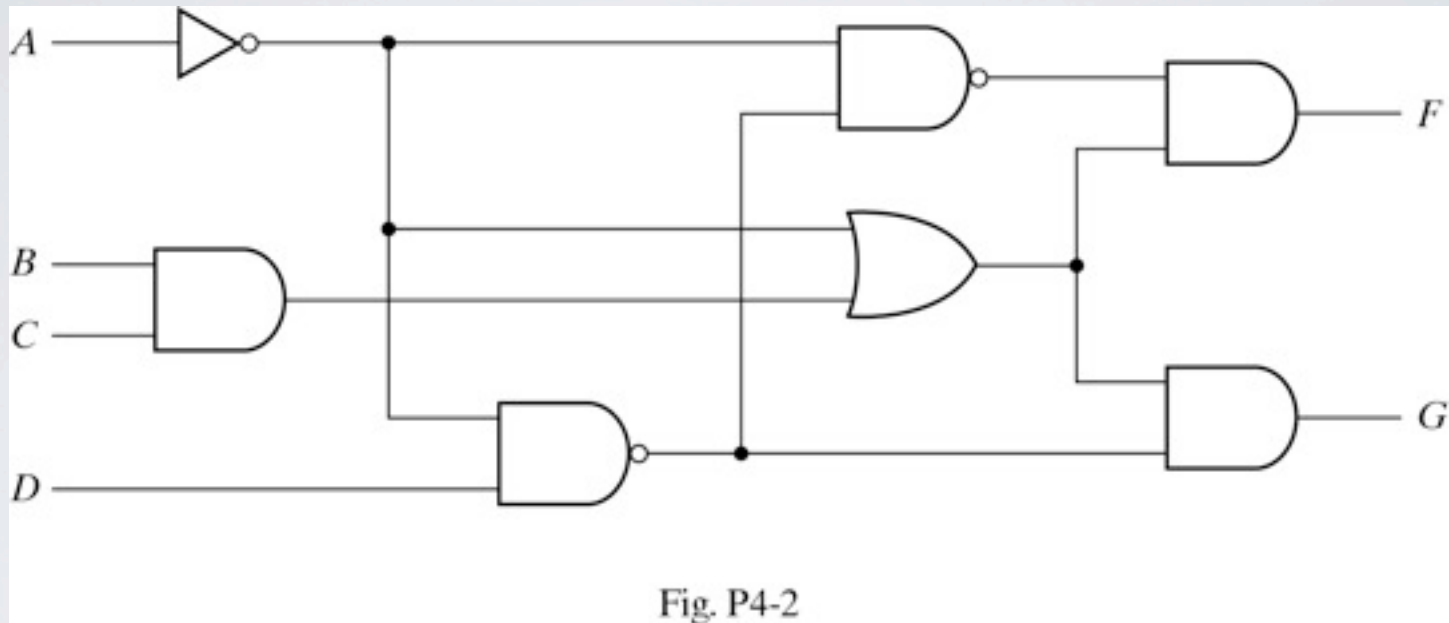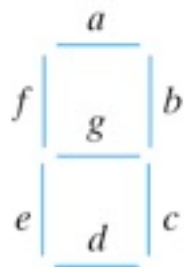
Fig. P4-1

Fig. P4-2

(a) Segment designation

(b) Numerical designation for display

Fig. P4-9