REGISTERS AND COUNTERS

INEL 4205 - LOGIC CIRCUITS - CHAPTER 6

SPRING 2008 - M. TOLEDO

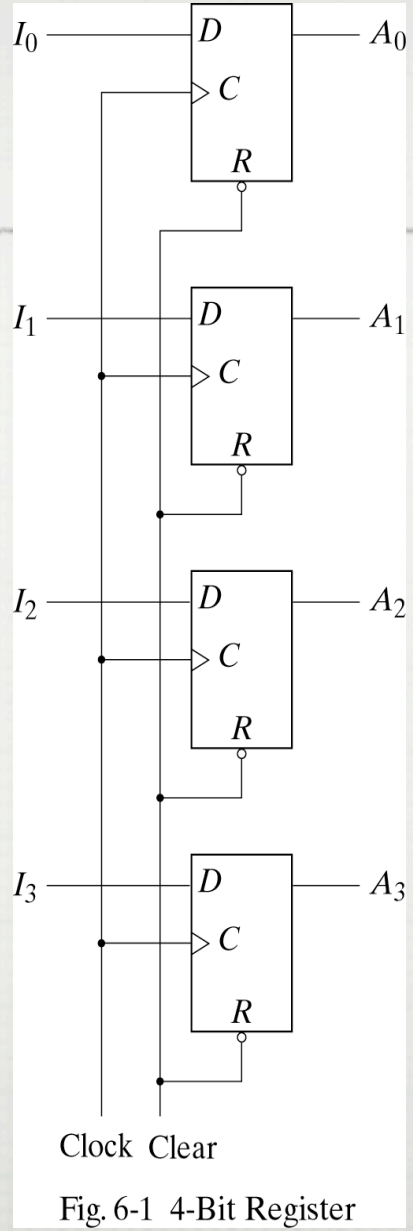


Fig. 6-1 4-Bit Register

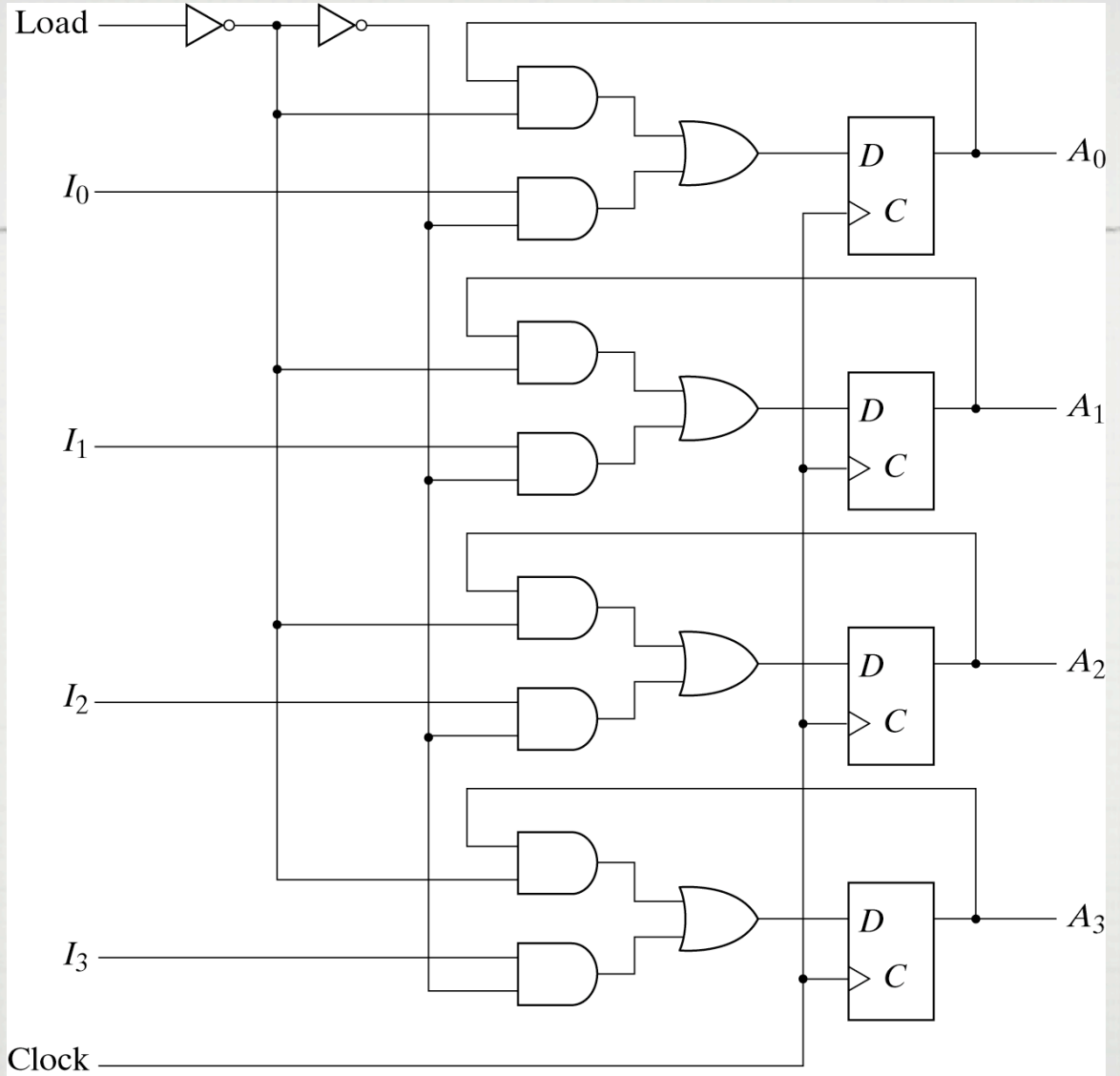


Fig. 6-2 4-Bit Register with Parallel Load

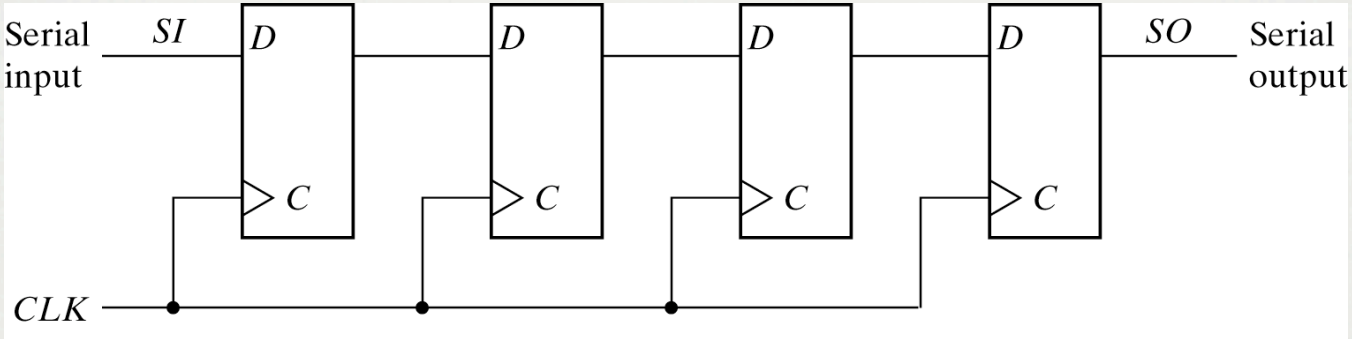


Fig. 6-3 4-Bit Shift Register

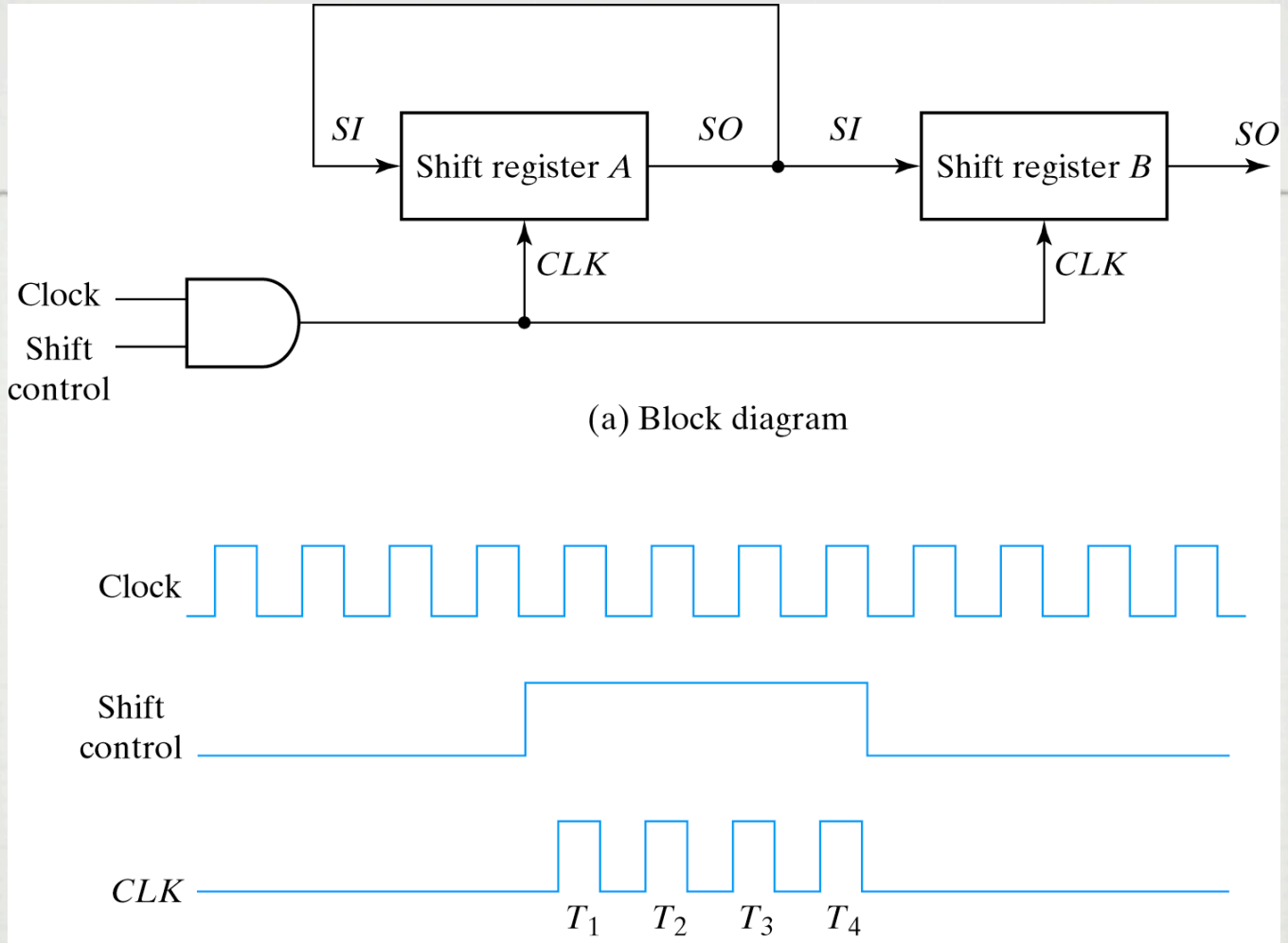


Fig. 6-4 Serial Transfer from Register *A* to register *B*

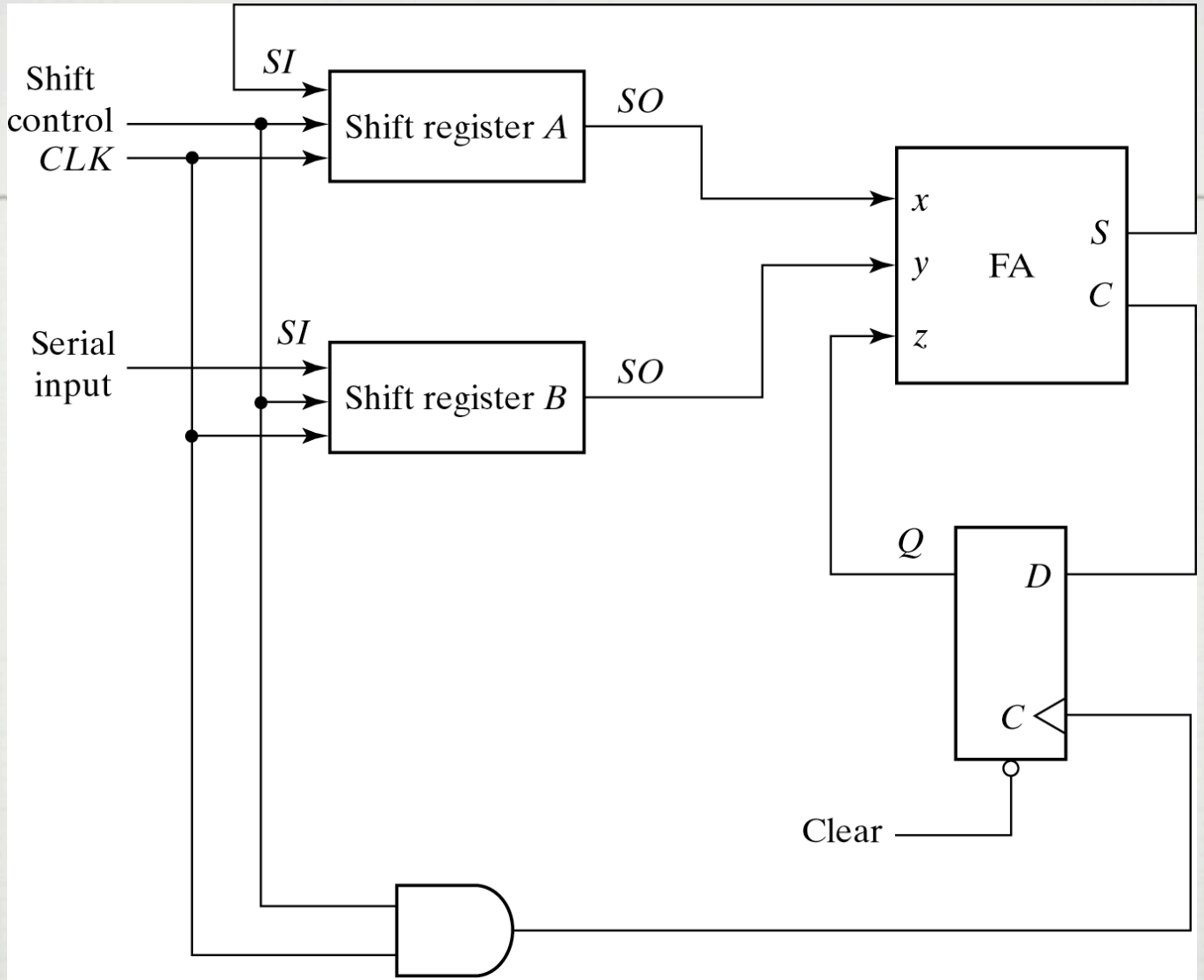


Fig. 6-5 Serial Adder

Table 6-2
State Table for Serial Adder

Present State	Inputs		Next State (Carry)	Output	Flip-Flop Inputs	
Q	X	y	Q	S	J_Q	K_Q
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

SERIAL-ADDER DESIGN:

SHIFT REGS WERE LEFT OUT OF THE TABLE

OUTPUT Q REFERS TO THE CARRY BIT.

AFTER MINIMIZATION ->

$$J_Q = xy$$
$$K_Q = x'y' = (x + y)'$$
$$S = x \oplus y \oplus Q$$

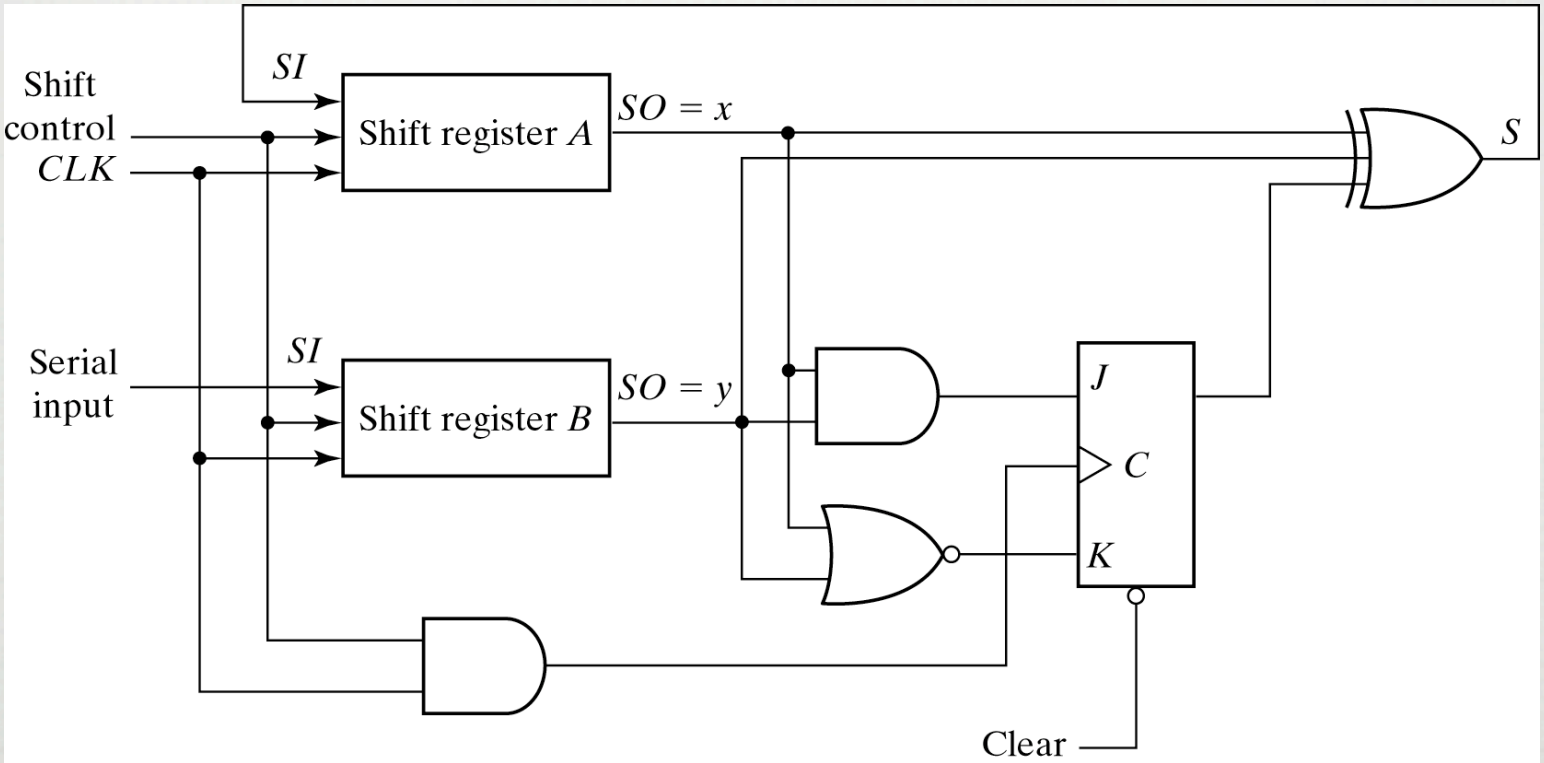


Fig. 6-6 Second form of Serial Adder

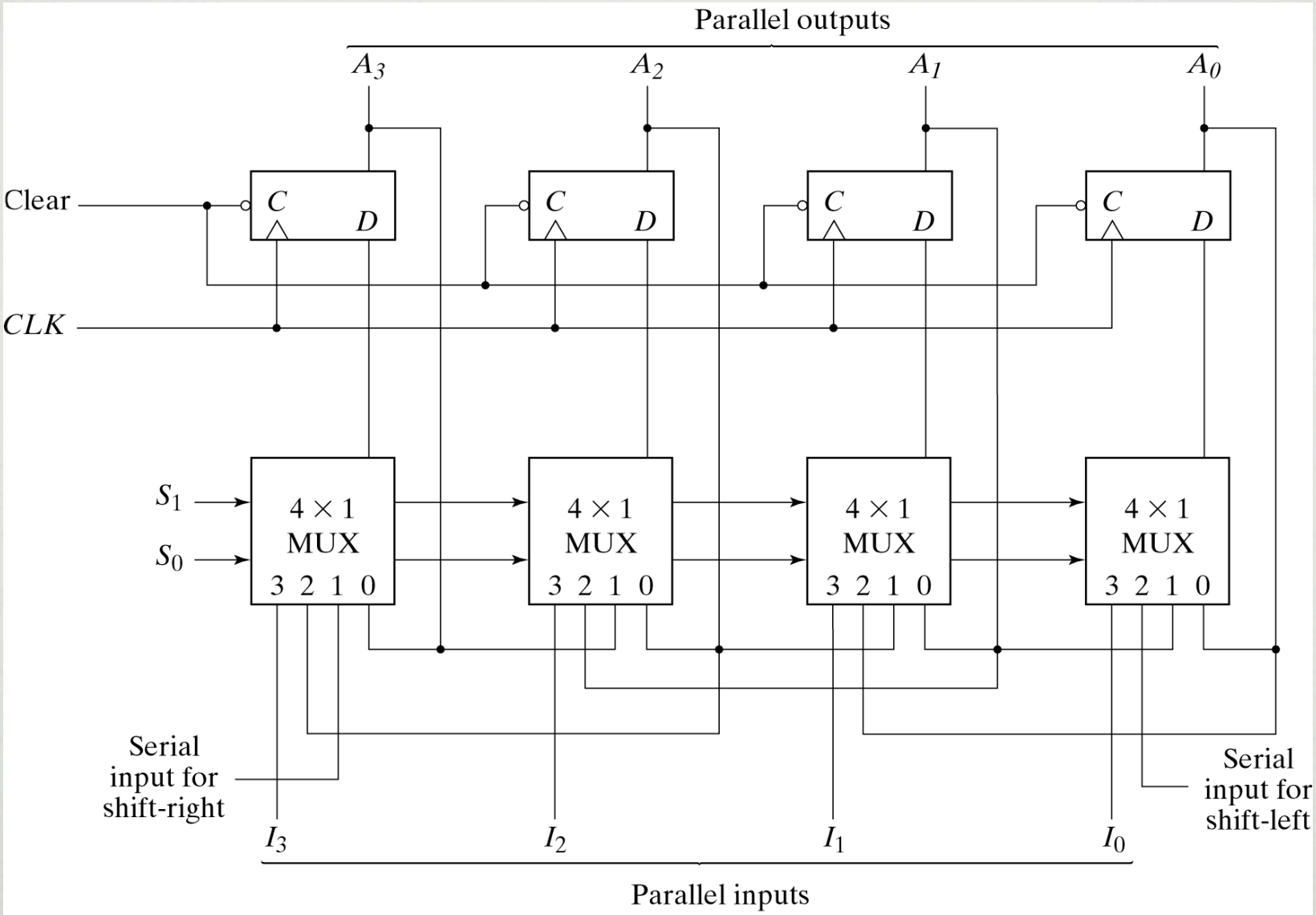


Fig. 6-7 4-Bit Universal Shift Register

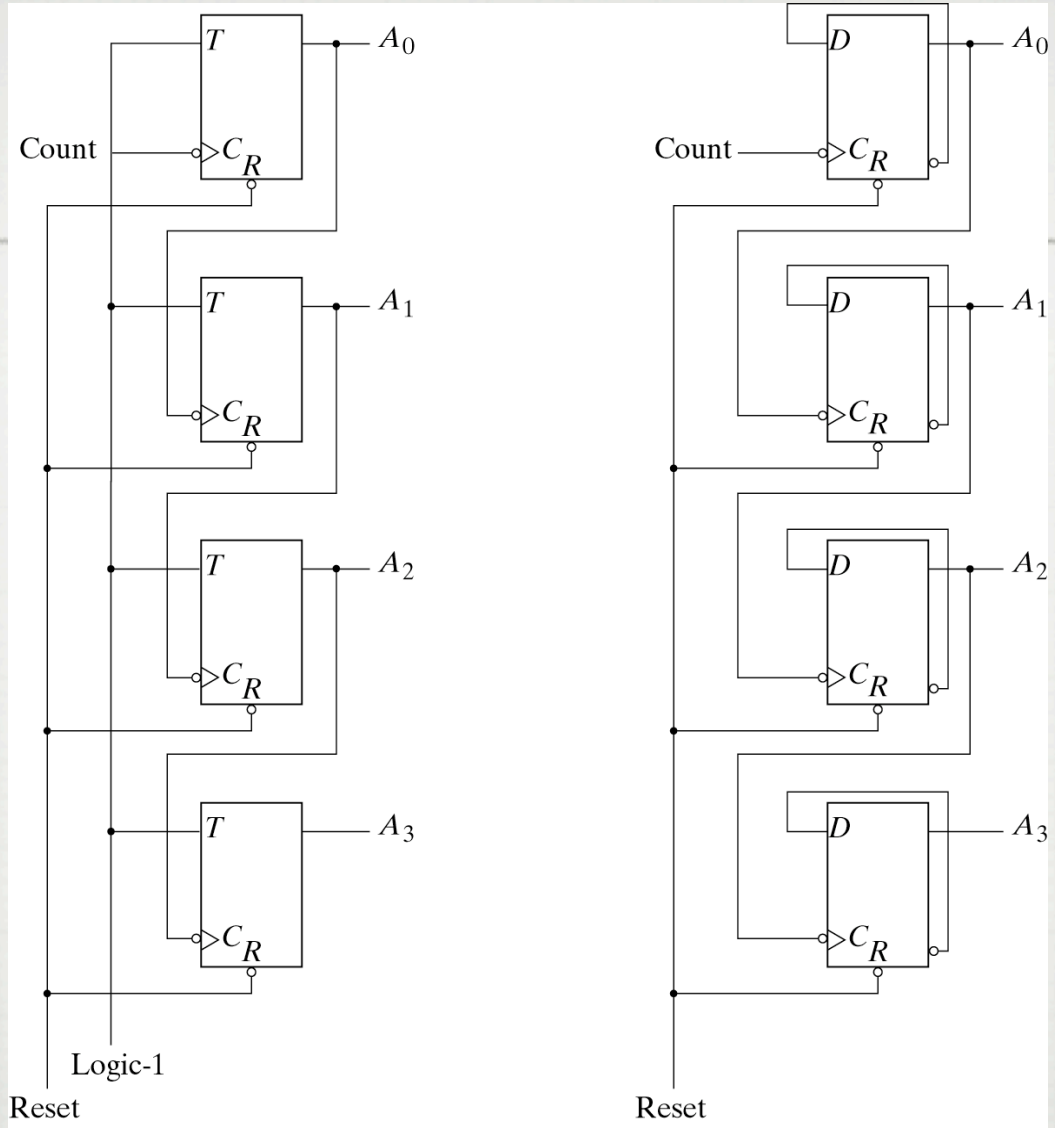


Fig. 6-8 4-Bit Binary Ripple Counter

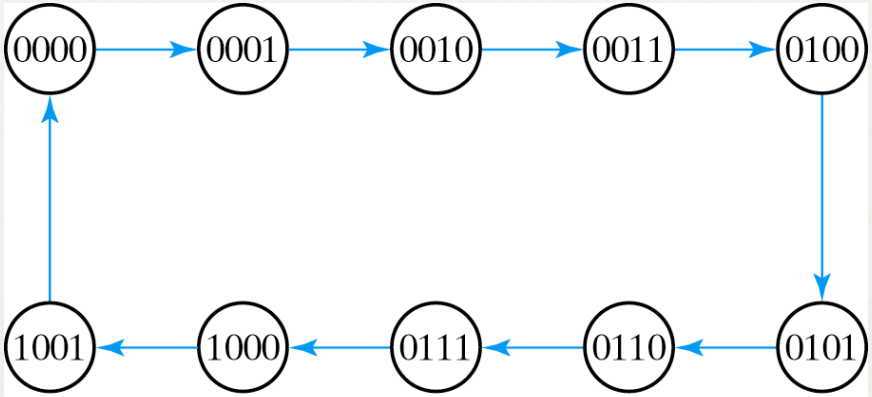


Fig. 6-9 State Diagram of a Decimal BCD-Counter

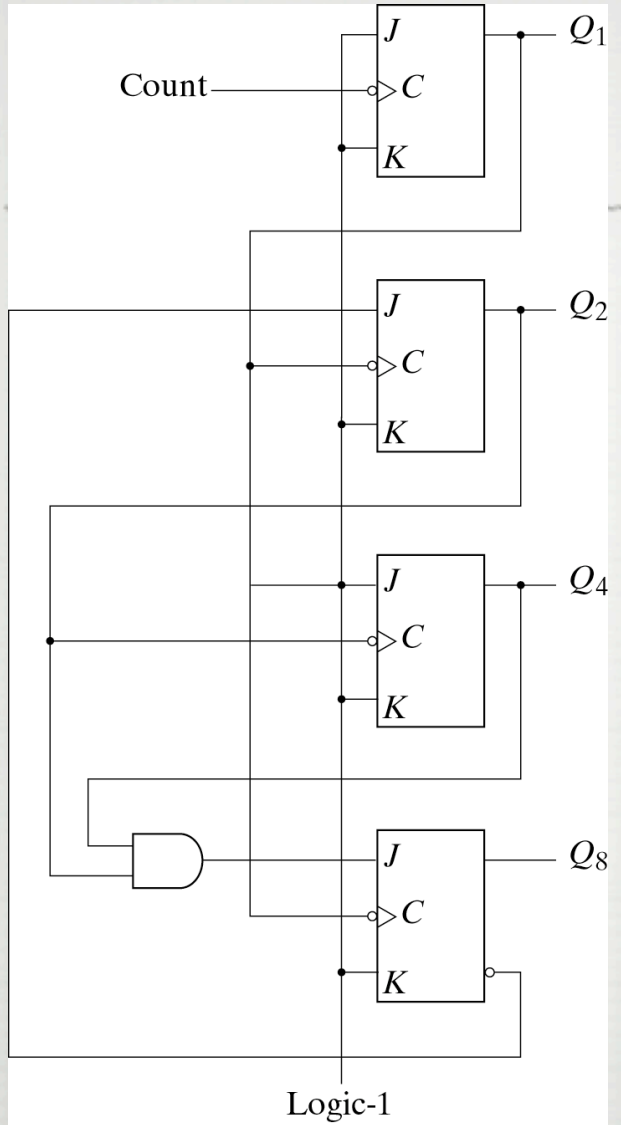


Fig. 6-10 BCD Ripple Counter

FF	Trigger	Signals
Q_1	Count↓	$J_1=K_1=1$: TOGGLE
Q_2	Q_1↓	$J2=Q_8'=1$; $K_2=1$ if Q8=1 RESET else TOGGLE
Q_4	Q_2↓	$J_4=K_4=1$: TOGGLE
Q_8	Q_1↓	$J_8=Q_2Q_4$; $K_8=1$ if Q_2 and Q_4=1 TOGGLE else RESET

ASYNCHRONOUS BCD COUNTER WITH JK FLIP FLOPS

Q_1 IS USED AS CLOCK (NEG EDGE)

PS	NS	J_2K_2	J_4K_4	J_8K_8
0000	0001			
0001	0010	1X	0X	0X
0010	0011			
0011	0100	X1	1X	0X
0100	0101			
0101	0110	1X	X0	0X
0110	0111			
0111	1000	X1	X1	1X
1000	1001			
1001	0000	0X	0X	X1
1010	XXXX			
1011	XXXX	XX	XX	XX
1100	XXXX			
1101	XXXX	XX	XX	XX
1110	XXXX			
1111	XXXX	XX	XX	XX

Q_1 ALWAYS TOGGLE
USE K-MAPS TO GET
DESIGN SIMILAR TO THE
ONE SHOWN IN
PREVIOUS SLIDE (BUT
USING Q_1 AS THE
CLOCK)

NOT USED IN BCD

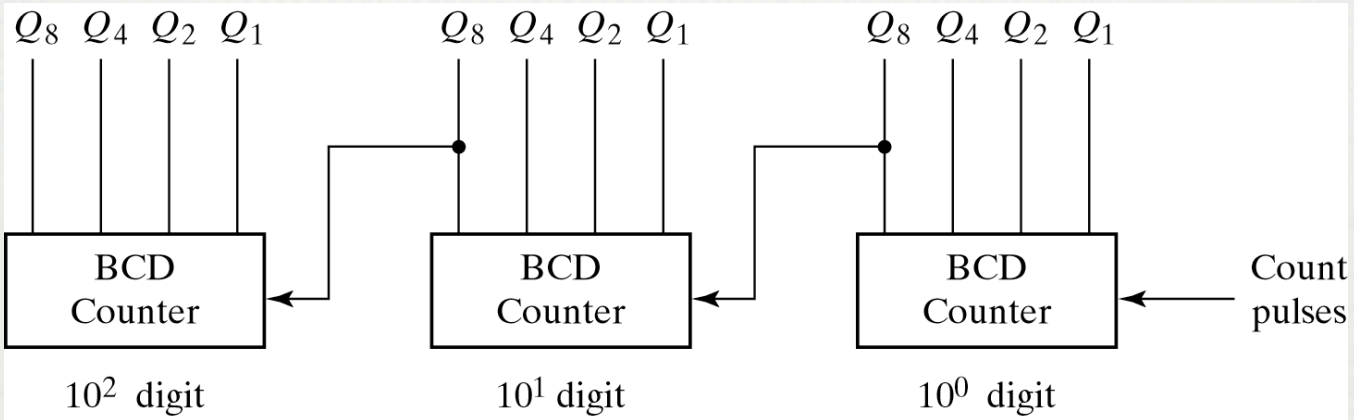


Fig. 6-11 Block Diagram of a Three-Decade Decimal BCD Counter

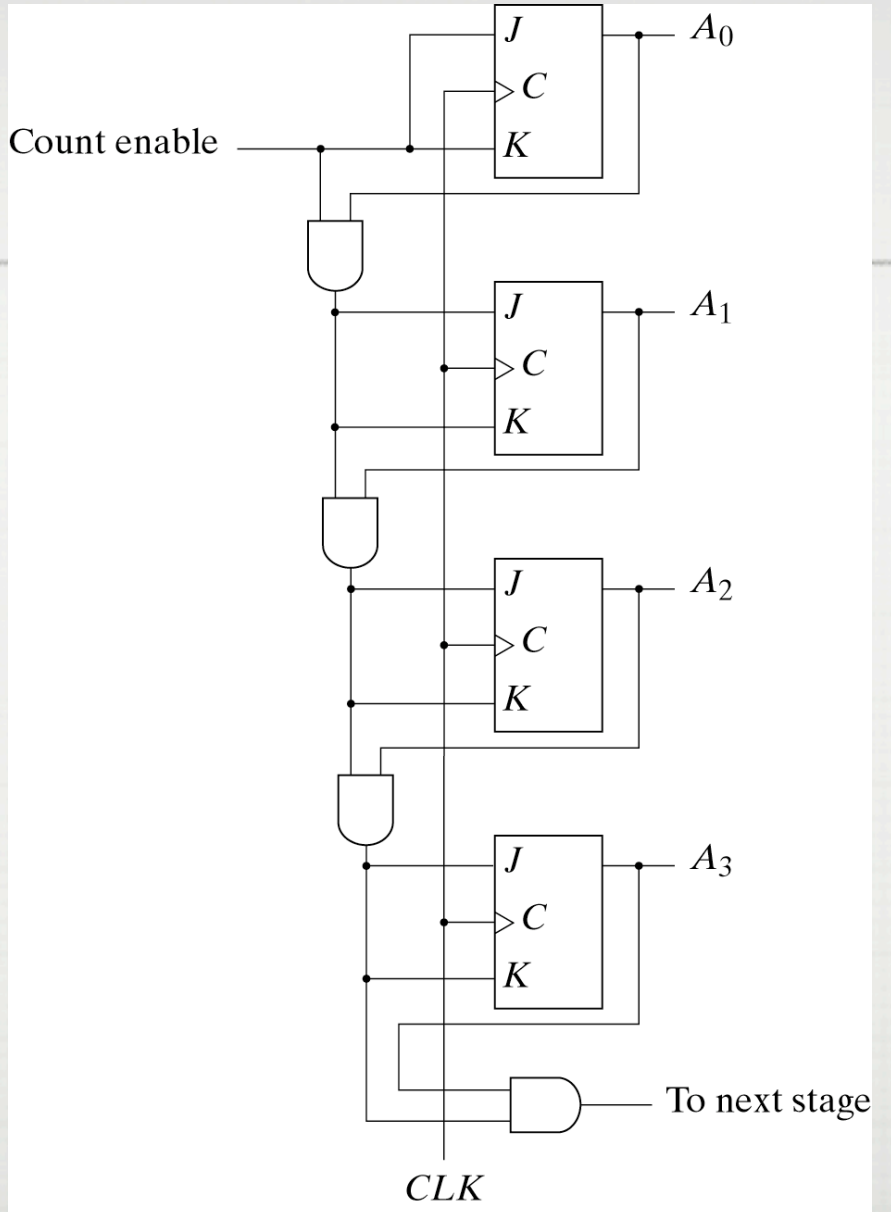


Fig. 6-12 4-Bit Synchronous Binary Counter

PS	NS
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

BY INSPECTION

A_0 TOGGLES IF E=1

A_1 TOGGLES IF EA_0=1

A_2 TOGGLES IF EA_0A_1=1

A3 TOGGLES IF $EA_0A_1A_2$=1

IF E = COUNT ENABLE =0

ALL HOLD

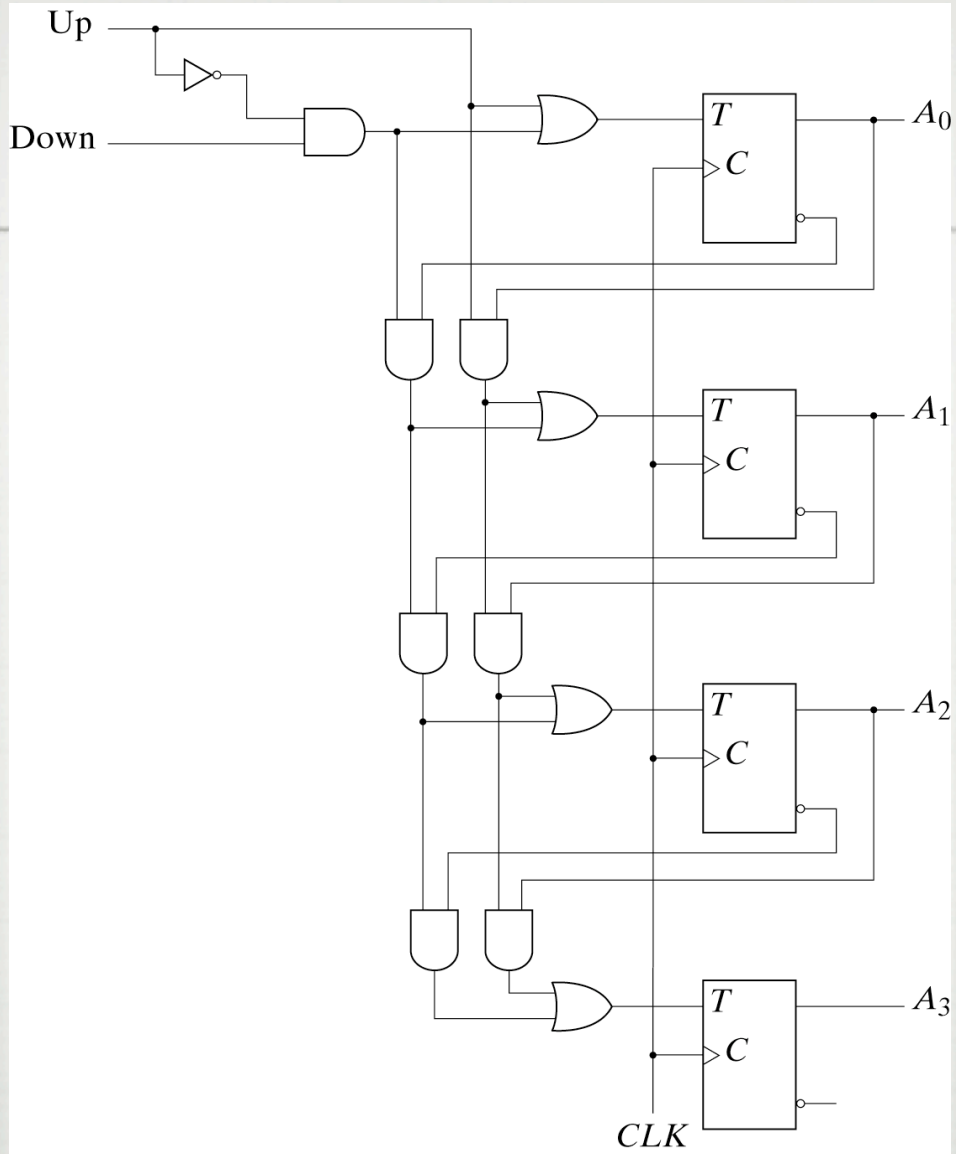


Fig. 6-13 4-Bit Up-Down Binary Counter

	UP	DOWN
PS	NS	NS
0000	0001	1111
0001	0010	0000
0010	0011	0001
0011	0100	0010
0100	0101	0011
0101	0110	0100
0110	0111	0101
0111	1000	0110
1000	1001	0111
1001	1010	1000
1010	1011	1001
1011	1100	1010
1100	1101	1011
1101	1110	1100
1110	1111	1101
1111	0000	1110

$T_0 = UP + DOWN$

$T_1 = UP \cdot A_0 + DOWN \cdot A_0'$

$T_2 = UP \cdot A_0 \cdot A_1 + DOWN \cdot A_0' \cdot A_1'$

$T_3 = UP \cdot A_0 \cdot A_1 \cdot A_2 + DOWN \cdot A_0' \cdot A_1' \cdot A_2'$

Table 6-5
State Table for BCD Counter

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	TQ_8	TQ_4	TQ_2	TQ_1
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

$$T_{Q1} = 1$$
$$T_{Q2} = Q_8' Q_1$$
$$T_{Q4} = Q_2 Q_1$$
$$T_{Q8} = Q_8 Q_1 + Q_4 Q_2 Q_1$$
$$y = Q_8 Q_1$$

USING CH. 5 DESIGN METHOD

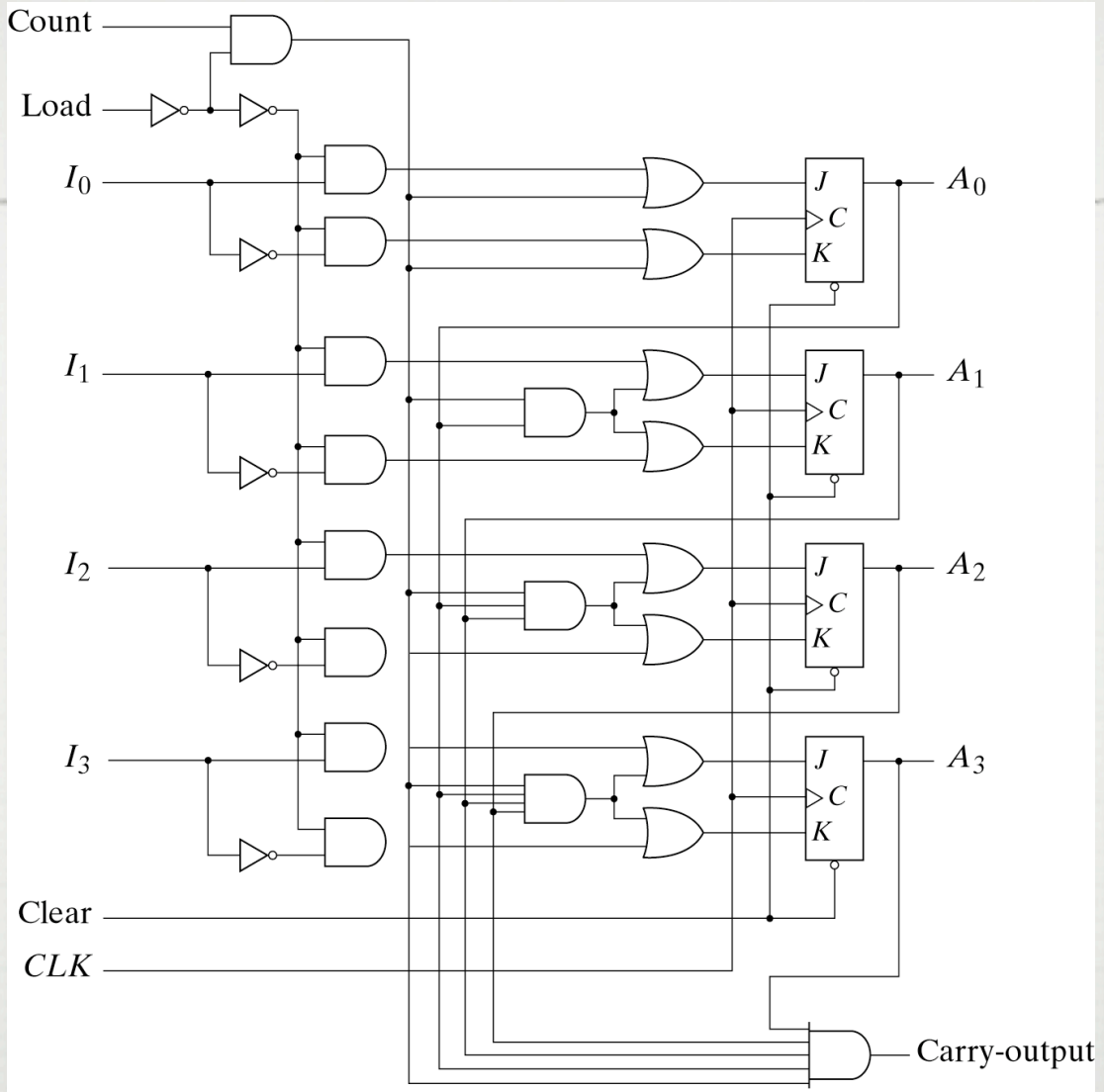


Fig. 6-14 4-Bit Binary Counter with Parallel Load

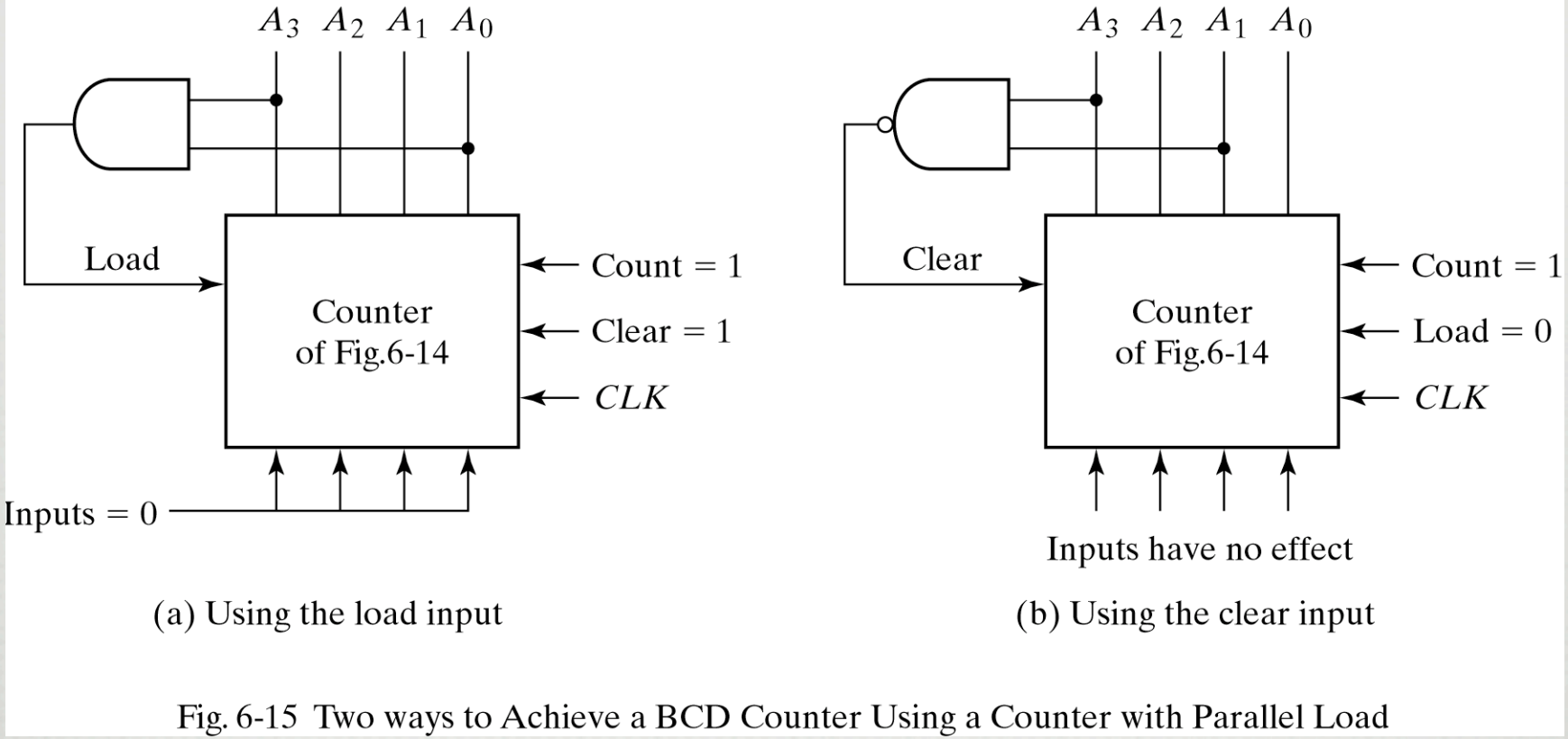
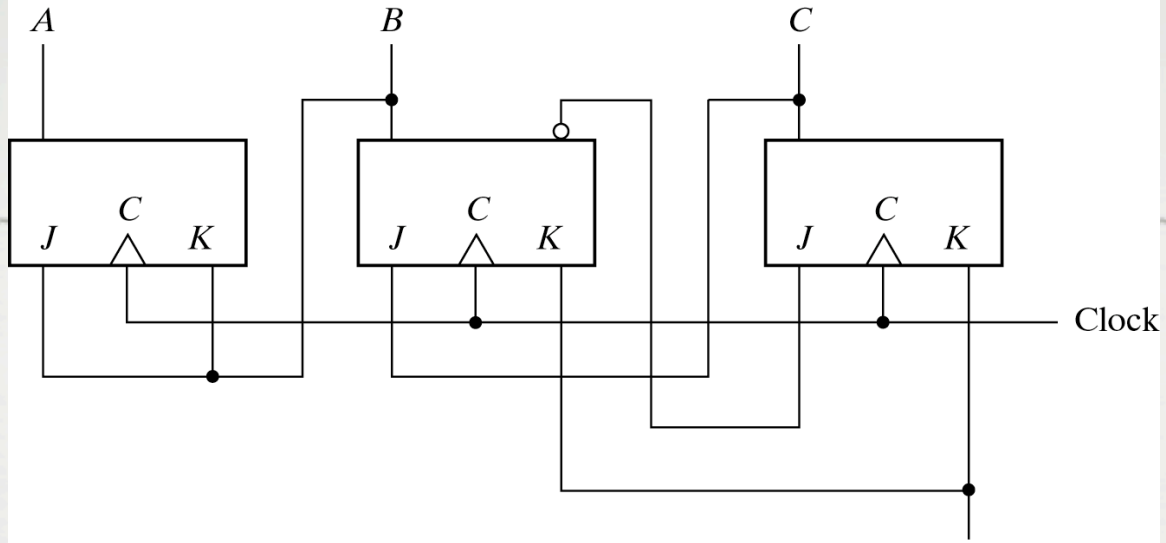


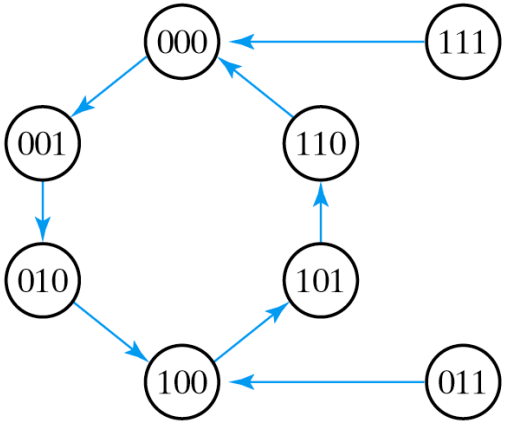
Fig. 6-15 Two ways to Achieve a BCD Counter Using a Counter with Parallel Load

Table 6-7
State Table for Counter

Present State			Next State			Flip-Flop Inputs					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

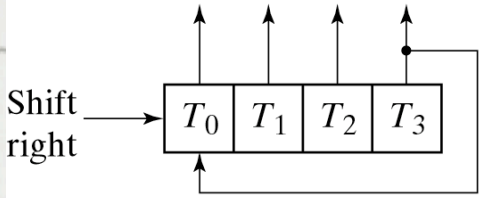


(a) Logic diagram

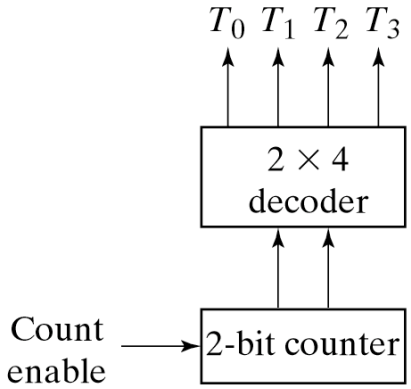


(b) State diagram

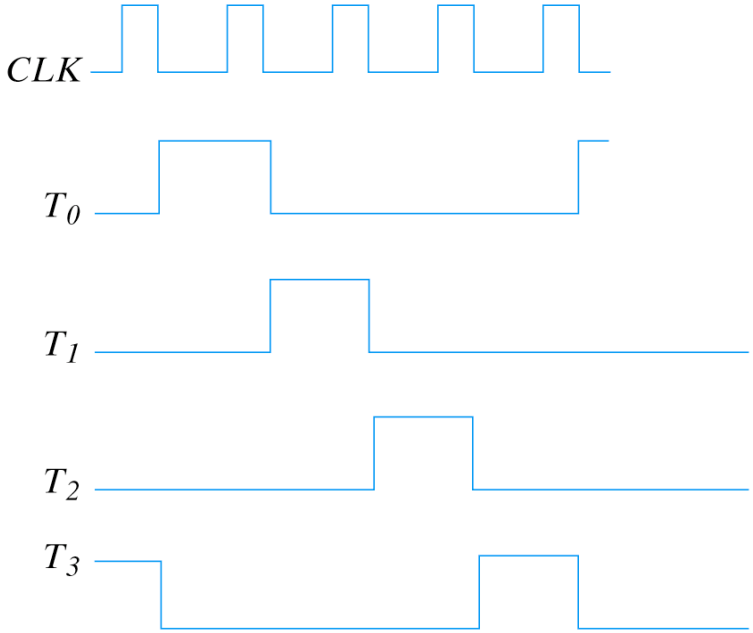
Fig. 6-16 Counter with Unused States



(a) Ring-counter (initial value = 1000)

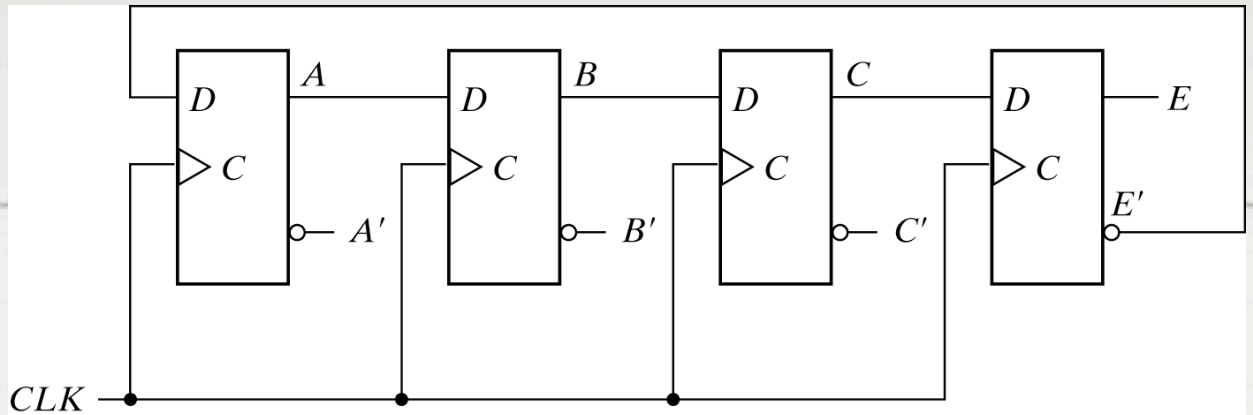


(b) Counter and decoder



(c) Sequence of four timing signals

Fig. 6-17 Generation of Timing Signals



(a) Four-stage switch-tail ring counter

Sequence number	Flip-flop outputs				AND gate required for output
	A	B	C	E	
1	0	0	0	0	$A'E'$
2	1	0	0	0	AB'
3	1	1	0	0	BC'
4	1	1	1	0	CE'
5	1	1	1	1	AE
6	0	1	1	1	$A'B$
7	0	0	1	1	$B'C$
8	0	0	0	1	$C'E$

(b) Count sequence and required decoding

Fig. 6-18 Construction of a Johnson Counter

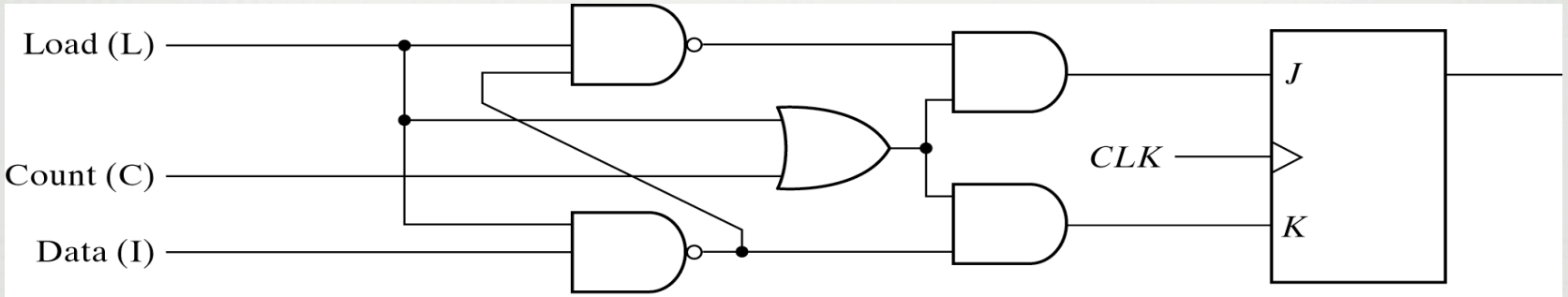


Fig. P6-21