Example 14.6

Consider a CMOS inverter fabricated in a 0.25-μm process for which $C_{ox} = 6$ fF/μm^2, $\mu_n C_{ox} = 115$ μA/V^2, $\mu_p C_{ox} = 30$ μA/V^2, $V_{tn} = -V_{tp} = 0.5$ V, and $V_{DD} = 2.5$ V. The W/L ratio of Q_N is 0.375 μm/0.25 μm, and that for Q_P is 1.125 μm/0.25 μm. The gate–source and gate–drain overlap capacitances are specified to be 0.3 fF/μm of gate width. Further, the effective (large-signal) values of drain–body capacitances are $C_{dbn} =$ 1 fF and $C_{dbp} = 1$ fF. The wiring capacitance $C_w = 0.2$ fF. Find t_{PHL}, t_{PLH}, and t_P when the inverter is driving an identical inverter.

Solution

First, we determine the value of the equivalent capacitance C using Eqs. (14.72) and (14.73),

$$C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w$$

where

$$C_{gd1} = 0.3 \times W_n = 0.3 \times 0.375 = 0.1125 \text{ fF}$$

$$C_{gd2} = 0.3 \times W_p = 0.3 \times 1.125 = 0.3375 \text{ fF}$$

$$C_{db1} = 1 \text{ fF}$$
$$C_{db2} = 1 \text{ fF}$$
$$C_{g3} = 0.375 \times 0.25 \times 6 + 2 \times 0.3 \times 0.375 = 0.7875 \text{ fF}$$
$$C_{g4} = 1.125 \times 0.25 \times 6 + 2 \times 0.3 \times 1.125 = 2.3625 \text{ fF}$$
$$C_w = 0.2 \text{ fF}$$

Thus,

$$C = 2 \times 0.1125 + 2 \times 0.3375 + 1 + 1 + 0.7875 + 2.3625 + 0.2 = 6.25 \text{ fF}$$

Next we use Eqs. (14.64) and (14.65) to determine t_{PHL},

$$\alpha_n = \frac{2}{\frac{7}{4} - \frac{3 \times 0.5}{2.5} + \left(\frac{0.5}{2.5}\right)^2} = 1.7$$

$$t_{PHL} = \frac{1.7 \times 6.25 \times 10^{-15}}{115 \times 10^{-6} \times (0.375/0.25) \times 2.5} = 24.6 \text{ ps}$$

Similarly, we use Eqs. (14.66) and (14.67) to determine t_{PLH},

$$\alpha_p = 1.7$$

$$t_{PLH} = \frac{1.7 \times 6.25 \times 10^{-15}}{30 \times 10^{-6} \times (1.125/0.25) \times 2.5} = 31.5 \text{ ps}$$

Finally, we determine t_P as

$$t_P = \frac{1}{2}(24.6 + 31.5) = 28 \text{ ps}$$