

# Lecture Notes for INEL 6055: Chapter 7

Manuel Toledo Quiñones  
Assistant Professor  
Electrical and Computer Engineering Department  
University of Puerto Rico  
Mayaguez, Puerto Rico

16th April 2002

## 1 Deep Sub-micron MOSFET

### 1.1 Down-scaling: Benefits and Rules

- MOSFET high/low transition time is determined by load capacitance and output current capability.
- Load capacitance is the input parasitic capacitance of next digital cell, and is proportional to the device area and thus to channel length.
- Current capability: in the ohmic region, eq. 5.17 gives

$$i_D = \frac{\mu_0 W C_{ox}}{L_{eff}} (V_{GS} - V_T) V_{DS}$$

Current capability is inversely proportional to channel length.

- If channel length is reduced by a factor  $S$ , device speed is increased by  $S^2$ .
- Circuit density goes up as well.
- Channel reduction also increases the penetration of the drain field into the substrate, increasing the chance of electrons jumping directly from source to substrate (punch-through effect).
- To prevent this from happening, substrate doping is increased. The depletion region width is

$$w_n \approx \sqrt{\frac{2\epsilon_s q (V_{bi} + V_R)}{q N_D}}$$

- To reduce the depletion layer width by a factor of  $S$ , doping must be increased by a factor  $S^2$ .
- Increasing substrate doping by a factor of  $S^2$  increases body factor by a factor of  $S$ ,

$$\gamma = \frac{\sqrt{2\epsilon_s q N_D}}{C_{ox}}$$

which in turn increases the threshold voltage.

- To prevent the increase in  $V_T$ , the oxide thickness is reduced by a factor of  $S$ . This would increase the load capacitance, so the width of the device is also reduced by a factor of  $S$  to compensate.
- See table 7.1.

## 1.2 Deep-sub-micron MOSFET

- Channel-length reduction introduces increases in the channel electric field.
- This could decrease the breakdown voltage to unacceptable levels.
- To reduce the maximum field in the depletion region, lightly-doped regions are introduced around the drain and source. The resulting device is called *lightly doped drain* (LDD) MOSFET.
- See slide 1.
- The lightly doped drain-source extensions are
  - doped with arsenic or antimony, which have lower diffusion constants than phosphorous.
  - shallow region are obtained.
  - poly self-aligned mask is used.
  - space oxide layer is created as a mask for phosphorous implantation.
  - Titanium is deposited to create low-resistance silicide layer on top of gate, drain and source.

## 1.3 Current Issues and Trends

- Current technology can produce feature dimensions under  $2\mu m$ .
- Next natural benchmark is  $100nm$  features.
- See slide 3. Results shown are similar to the ones published by IBM researchers in 1987.
- In the sub-threshold region, the drain current should behave like a BJT (see equation 5.44). Drain current should be determined by  $V_{GS}$ .

- Slide 3 shows the effect of a change in  $V_{DS}$  in drain current. Change in drain current indicates short-channel effect due to a too deep penetration of the drain-to-substrate depletion region under the gate.
- Slide 4 shows the energy band diagram. The absence of a significant barrier in the source areas allow electrons to get over and roll down to the drain.
- The OFF (leakage) current in top slide 3 figure is over  $1\mu A$ . This means that a million cells will require  $1A$  of current in the OFF state!
- improved situation is shown in slide 3 center and bottom. However, this would require a  $1nm$  high quality oxide layer. Such thickness would, however, allow electron tunneling. Thus the oxide will have to be replaced by another material with higher permittivity.
- Other possible solutions to this problem are (1) engineering the substrate doping profile (high doping below the surface, where the gate field is not so strong; lower doping at the surface to reduce  $V_T$ ); (2) SOI technology; (3) many others.
- Other issues for sub-100-nm mass production, such as lithography, exist.