DYNAMIC & DOMINO LOGIC

INEL 4207 - Digital Electronics

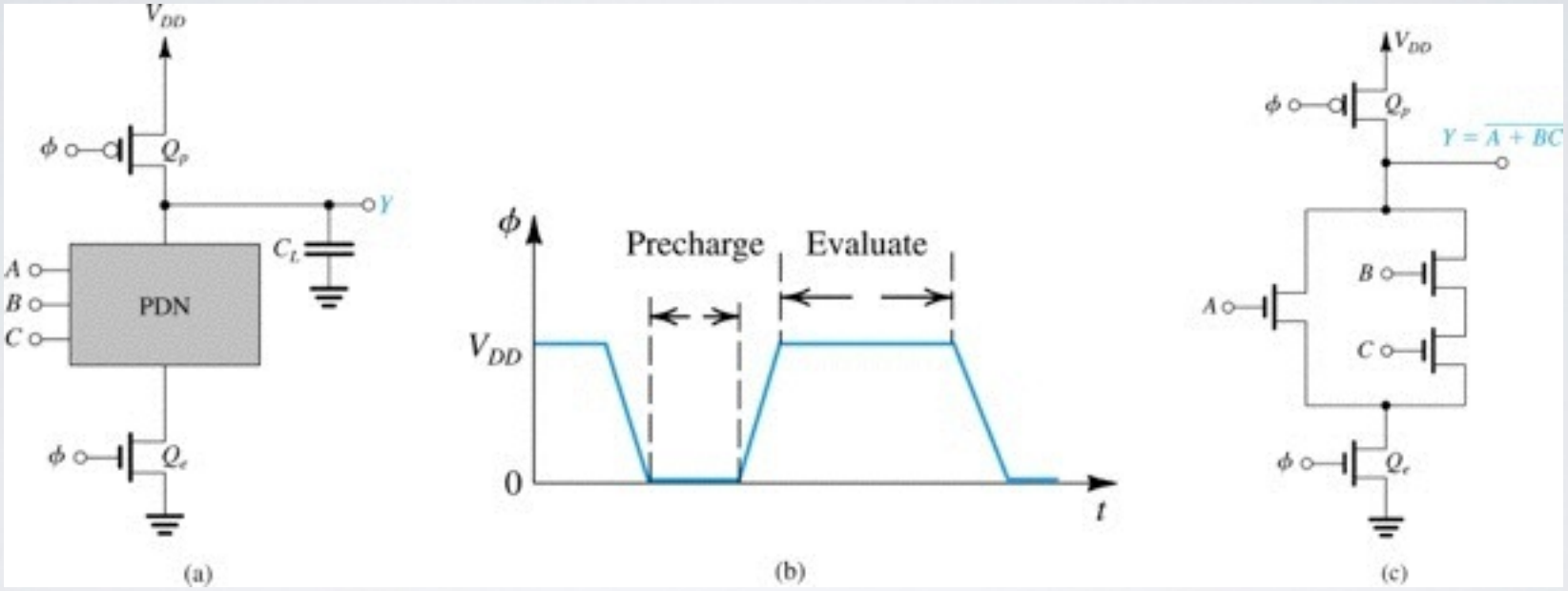


Figure 15.19 (a) Basic structure of dynamic-MOS logic circuits. (b) Waveform of the clock needed to operate the dynamic logic circuit. (c) An example circuit.

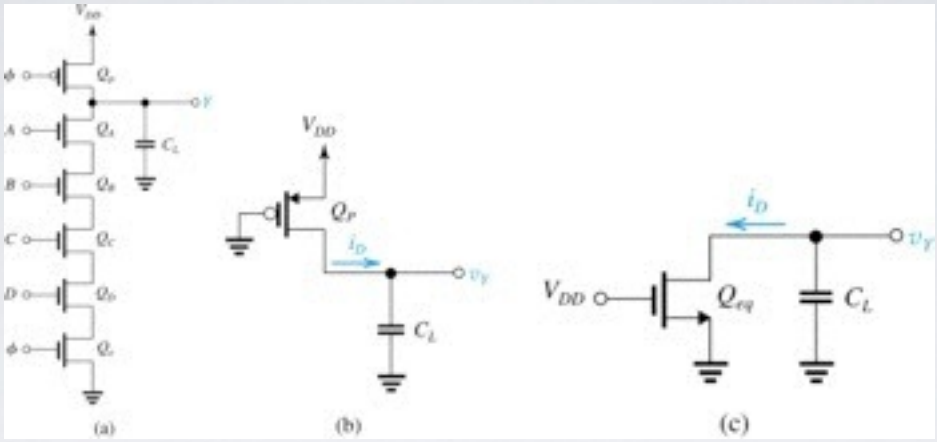


Figure 15.20 Circuits for Example.

Assume $V_{DD} = 1.8V$, $V_t = 0.5V$, $\mu_n C_{ox} = 4\mu_p C_{ox} = 0.3mA/V^2$, $(W/L)_n = 0.27\mu m/0.18\mu m$ (including Q_e), $(W/L)_p = 0.54\mu m/0.18\mu m$ (for Q_p), $C_L = 20fF$.

a) For the pre-charge operation, with Q_p's gate at $0V$ and if C_L is fully discharged at $t = 0$, find the time for v_Y to rise from 10% to 90% of V_{DD}.

b) For $A = B = C = D = 1$, find t_{PHL}

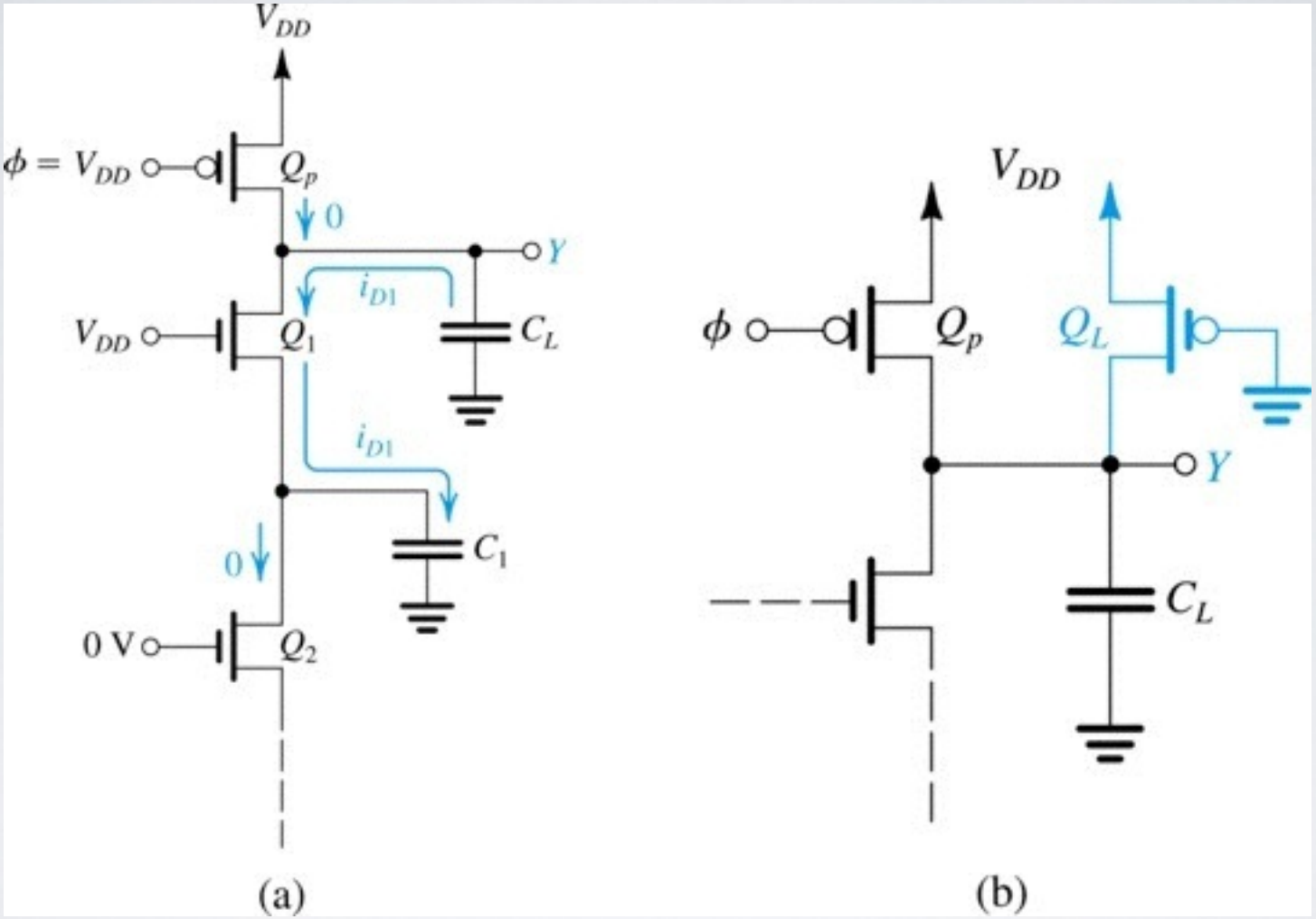
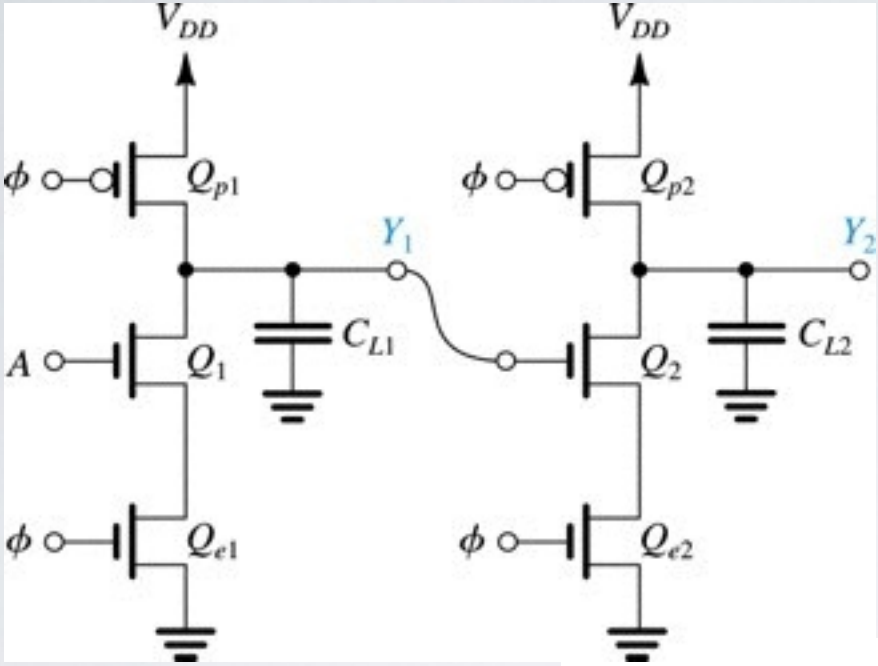


Figure 15.21 (a) Charge sharing. (b) Adding a permanently turned-on transistor Q_L solves the charge sharing problem at the expense of static power dissipation.

Cascading dynamic logic gates



By the time v_{Y1} drops to V_t, C_{L2} can loose a significant amount of charge causing v_{Y2} to can be significantly reduced.

Figure E 15.10

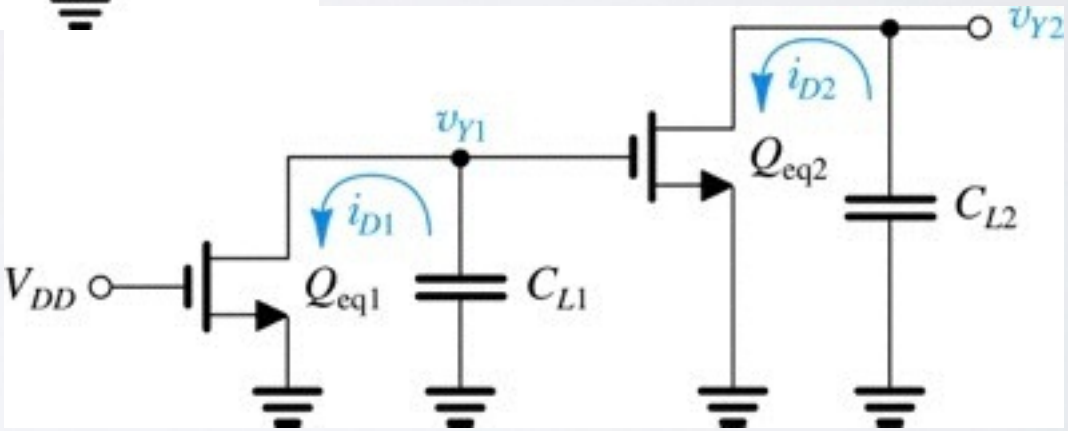


Figure 15.22 Two single-input dynamic logic gates connected in cascade. With the input A high, during the evaluation phase C_{L2} will partially discharge and the output at Y_2 will fall lower than V_{DD}, which can cause logic malfunction.

Consider the circuit as the evaluation phase begins: at $t = 0$, $v_{Y1} = v_{Y2} = V_{DD}$ and $v_\phi = v_A = V_{DD}$. Q_{p1} and Q_{p2} are cutoff and can be removed from the equivalent circuit. Replace series combinations of $Q_1 - Q_{e1}$ and $Q_2 - Q_{e2}$ by equivalent devices.

Consider the interval Δt during which v_{Y1} falls from V_{DD} to V_t, at which time Q_{eq2} turns off and C_{L2} stops discharging. Assume $(W/L)_n = 4\mu m/2\mu m$ and $C_{L1} = C_{L2} = 40fF$. Assume $V_{DD} = 5V$, $V_{t0} = 1V$, $\mu_n C_{ox} = 2.5\mu_p C_{ox} = 50\mu A/V^2$, $(W/L)_n = 4\mu m/2\mu m$.

Find

a) $(W/L)_{eq1}$ and $(W/L)_{eq2}$.

b) an average i_{D1}, $i_{D1,av}$, from $i_{D1}(v_{Y1} = V_{DD})$ and $i_{D1}(v_{Y1} = V_t)$.

c) Δt using $i_{D1,av}$

d) $i_{D2,av}$ obtained when v_{Y1} is halfway through its excursion (i.e. $v_{Y1} = 3V$). Hint: Q_{eq2} is in saturation.

e) Use Δt found in (c) and $i_{D2,av}$ to estimate the reduction in v_{Y2} and its final value.

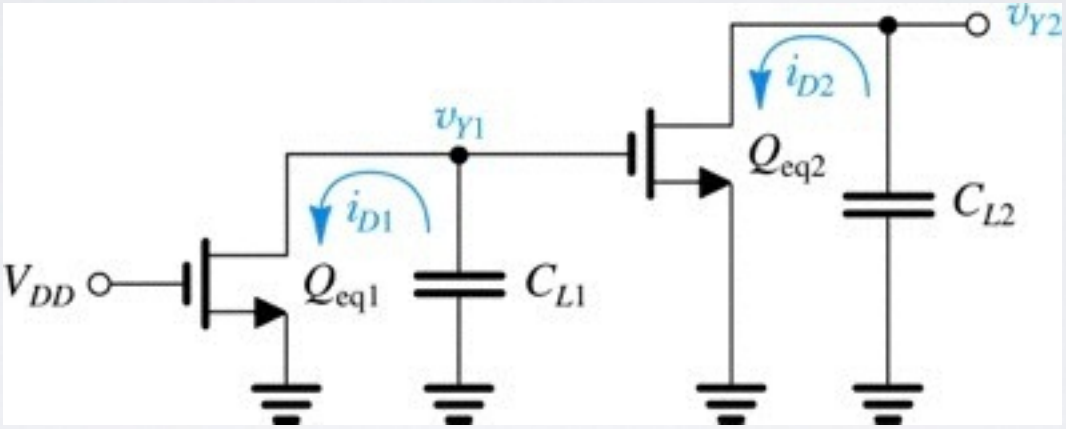


Figure 15.10

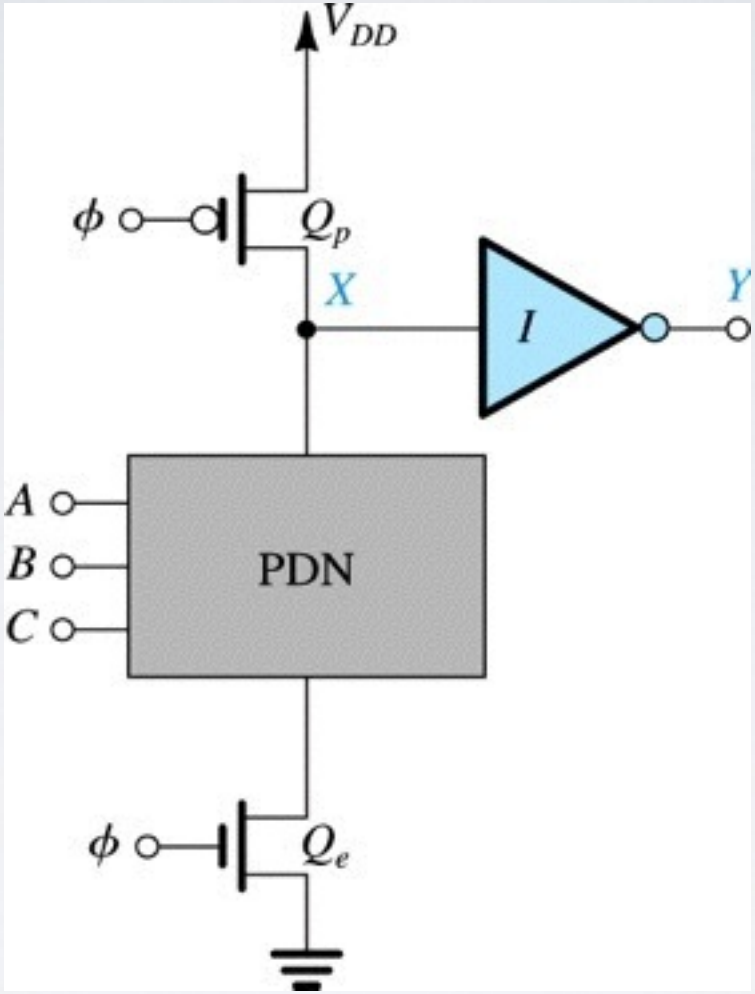


Figure 15.23 The Domino CMOS logic gate. The circuit consists of a dynamic-MOS logic gate with a static-CMOS inverter connected to the output. During evaluation, Y either will remain low (at 0 V) or will make one 0-to-1 transition (to V_{DD}).

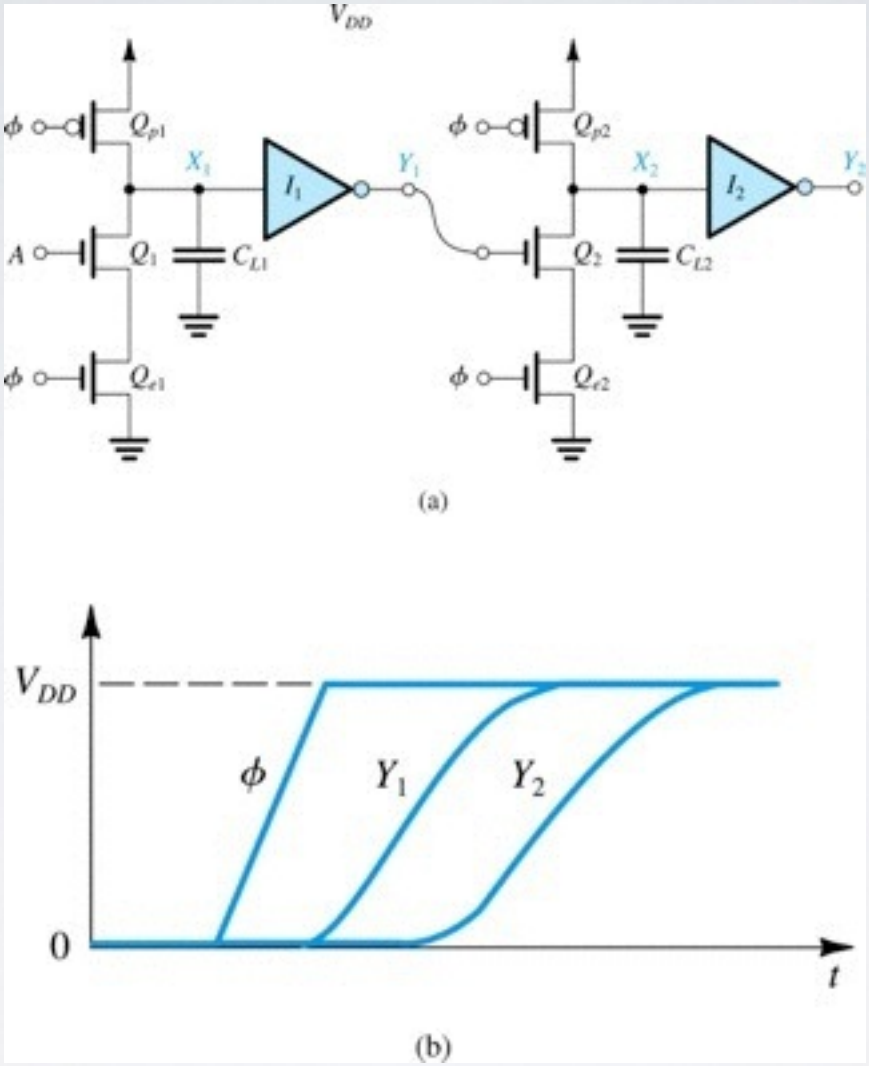


Figure 15.24 (a) Two single-input Domino CMOS logic gates connected in cascade. (b) Waveforms during the evaluation phase.