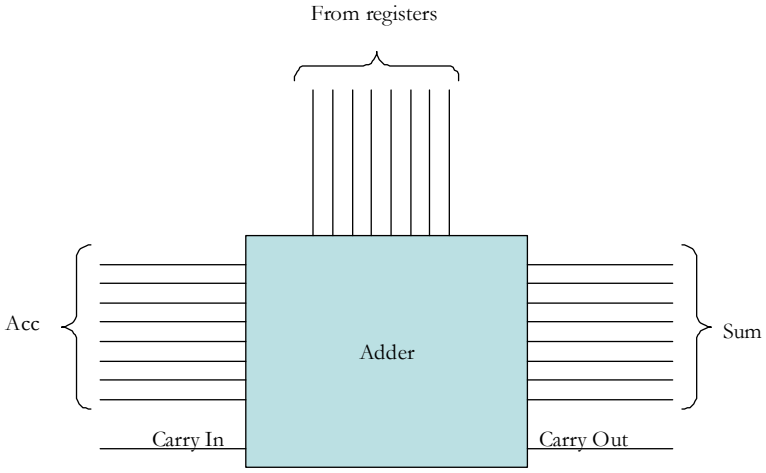
ICOM 4215 Project 2 Fall 2010
Processor ALU: Phase 1: Adder

Today: Monday, November 29, 2010
Due date of phase I: Monday, December 6, 2010
Group project: two or three students per group.
Points: 100 points (Penalties: Next day: -10 points, Two days late: -25 points, Three days late: -40
points, Four days late or more: not accepted)
Report and Code submission: Via email, please copy all members of your group in your email when sending the report.
Evaluation: Via oral exam, aka "Happy Hour".

Project: ALU design of the RISC AR.
The ALU implements arithmetic and logic operations, as well as data movement operations. Most of the arithmetic or logic operations will require two operands. This will allow you to implement the ALU with either one or two busses. In this first phase of the project, you will implement only the adder of the RISC AR.



The language to implement the Project will either be Verilog or VHDL (your Choice). The design should be clear enough to understand its components. We suggest you implement a testbench for input of the test signals.

Evaluation:
Project Report is 50% of your grade for project 2. Project Happy Hour is the other 50% of your grade.

Report
The report is a very simple document. It contains a schematic description of the Adder and a description of the process to simulate the adder. There should be a short description of the design considerations you used to make your design. In addition the appendix will contain

the code for the adder and the testbench that you designed to test your design. Length: No more than 6 pages (without appendix, 5 pages body and 1 page title).

Report Evaluation

Please include in the report the following elements:

Item	Points
1. Title page containing university, department, title, names, date	5
2. Summary or abstract: A brief description of the project, including what was designed, the approach taken to work as a team, and outcomes.	10
3. Introduction: background information. Brief information on adders.	10
4. Design: Describe the adder. Include schematic. What where the criteria used for the design? How does the testbench work?	25
5. Method: How you and your partner divided the tasks among group members?	10
6. Results and Discussion: Show time diagrams. What did you learn?	10
7. Conclusion: Summarize results. How would you improve the adder? What would you add or delete?	5
8. References: references used to back up the work (use them within the text)	5
9. Appendices: VHDL or Verilog code. Timing diagrams. Additional information required not suitable for the body of the report.	5
10. Professional appearance and organization	5
11. Grammar and composition	5
12. Language and vocabulary	5

Happy Hour Evaluation:

Aspect of the project where the student spent most of the time: _____

1. Her/his part is a significant effort contribution to the whole project. (40%)
2. Understands the project in general. Knowledge and experience on the topic related to his/her part. Management of questions. (40%)
3. Her/his part has been completed. (20%)