ICOM 4215 Project 2 Fall 2010 Processor ALU: Phase 2: Complete the ALU

Today: December 15, 2010

Due date phase I: December 29, 2010

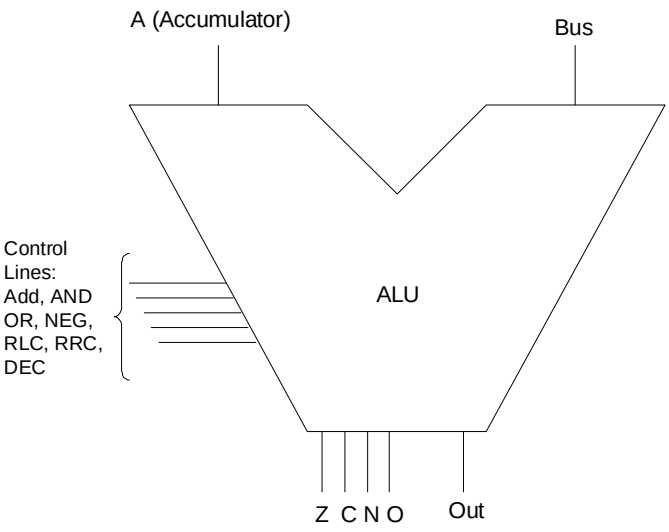
Group project: two or three students per group.

Submission:

- Via oral exam, aka “Happy Hour” with simulator.
- Report, via email

Project

ALU design of the RISC AR. The ALU implements arithmetic and logic operations, as well as data movement operations. Most of the arithmetic or logic operations will require two operands. This will allow you to implement the ALU with either one or two busses. In this second phase of the project, you will implement the rest of the ALU (include the adder). The ALU will include the logic necessary to implement the shift, and, or, add, neg, rotate left and right, and dec.



The language to implement the Project will either be Verilog or VHDL (your Choice). The design should be clear enough to understand its components. We suggest you implement a testbench for input of the test signals.