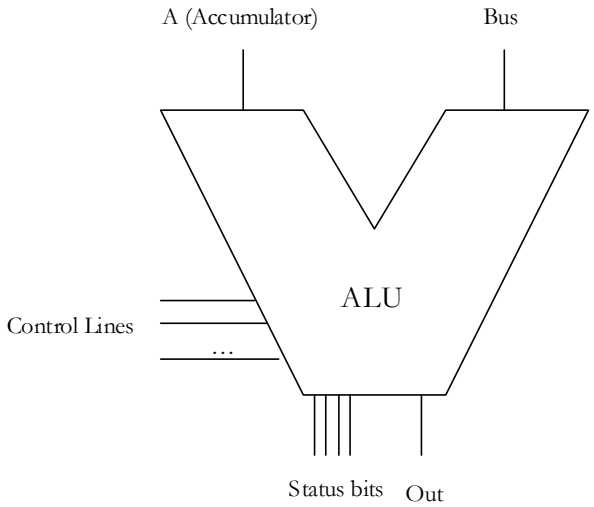
ICOM 4215 Project 2 Fall 2011
ALU

Today: October 24, 2011
Due date: November 7, 2011
Points: 100 points (Penalties: Next day: -10 points, Two days late: -25 points, Three days late: -40 points, Four days late or more: not accepted)
Group project – Three students per group
Submission:

- **Via oral exam, aka "Happy Hour"**
- **Report, via email**

Project:
Design an ALU for the RISC AR3 and test your design. The ALU implements arithmetic and logic operations Most of the arithmetic or logic operations will require two operands. Implement the functional units that support the ALU (multiplier and adder) and then the rest of the ALU. The ALU will include the logic necessary to implement the and, or, xor, addc, sub, mul, neg, not, rlc, rrc, and inc2.



The language to implement the Project will either be Verilog or VHDL (your Choice). The design should be clear enough to understand its components. We suggest you implement a testbench for input of the test signals.