ICOM 4215 Project 3 Fall 2012 Processor Controller

Today: Monday, November 21, 2012

Due date: Monday, December 6, 2012

Points: 100 points (Penalties: Next day: -10 points, Two days late: -25 points, Three days late: -40 points, Four days late or more: not accepted)

Group project – Three students per group

Submission:

- Via oral exam, aka "Happy Hour".
- Report, via email, subject on the email: Project 3 ICOM 4215, students will lose 5 points if the subject is changed. Send the email to naydag.santiago@upr.edu. Email due time, 11:59pm.

Project

Design the controller for the RISC AR5 previously designed in Projects 1 and 2.

Project requirements

Your team will design all the components of the processor and determine the control lines. Then the only part to turn in is the simulation either in Verilog or VHDL of the controller. As deliverable your group needs to specify all the components of the processor and the controller design and behavior. We will work with a 1 bus architecture. In addition, each group will have a different processor design, therefore, the controller's characteristics are different.

To make it clear: in order to generate the controller, you must know all the parts of your processor, but only the controller will be simulated in a hardware description language.

The report will contain: detailed schematics of the processor design. Detailed explanation of the controller, timing diagrams showing the behavior of the controller, appendix containing the code developed in VHDL or VERILOG.

The oral exam will be individually graded. Each student must demonstrate the proficiency and capability of designing a processor and a controller.

Report

Report will include four parts: (1) a description of the controller, (2) a schematic description, (3) Register Transfer notation, and (4) Timing Diagrams. Please include code as an attachment.