ICOM 4215: Computer Architecture and Organization

Introduction to Computer Architecture

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Slides modified from Dr. T. Noack course slides
Original source: Authors of Heuring and Jordan book
And Stallings book

Architecture & Organization 1

- Architecture is those attributes visible to the programmer
  - Instruction set, number of bits used for data representation, I/O mechanisms, addressing techniques.
  - e.g. Is there a multiply instruction?
- Organization is how features are implemented
  - Control signals, interfaces, memory technology.
  - e.g. Is there a hardware multiply unit or is it done by repeated addition?

This slide is from Stallings Architecture

Architecture & Organization 2

- All Intel x86 family share the same basic architecture
- The ARM11 family share the same basic architecture

- This gives code compatibility
  - At least backwards
- Organization differs between different versions

Structure & Function

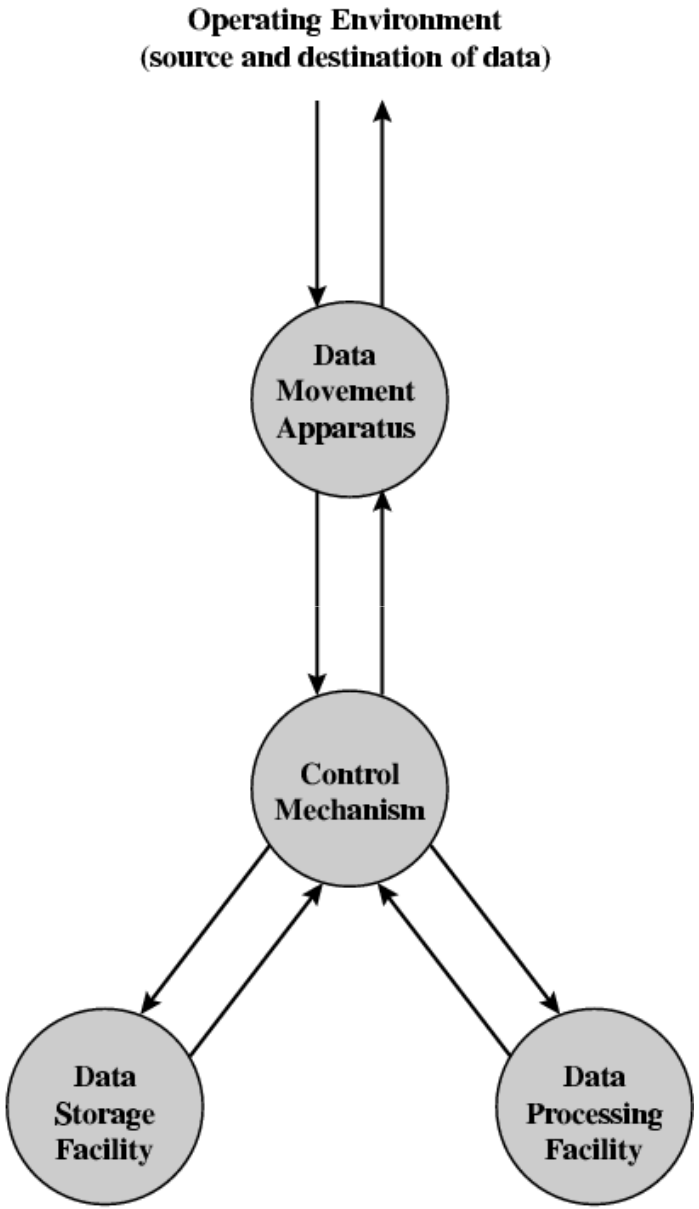
- Structure is the way in which components relate to each other
- Function is the operation of individual components as part of the structure

Function

- All computer functions are:
  - Data processing
  - Data storage
  - Data movement
  - Control

This slide is from Stallings Architecture

Functional View



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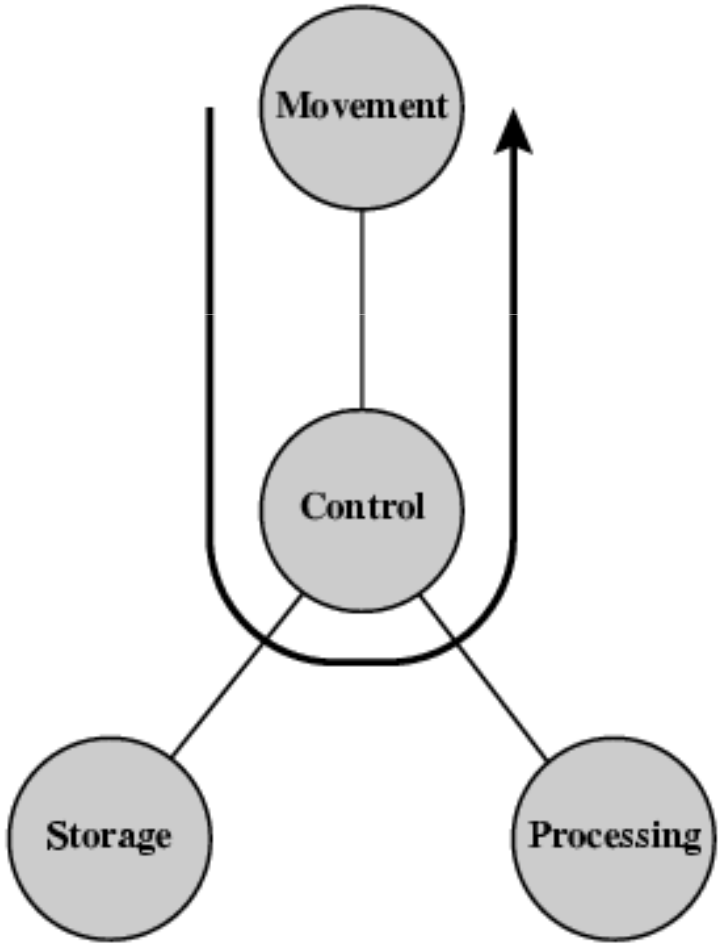
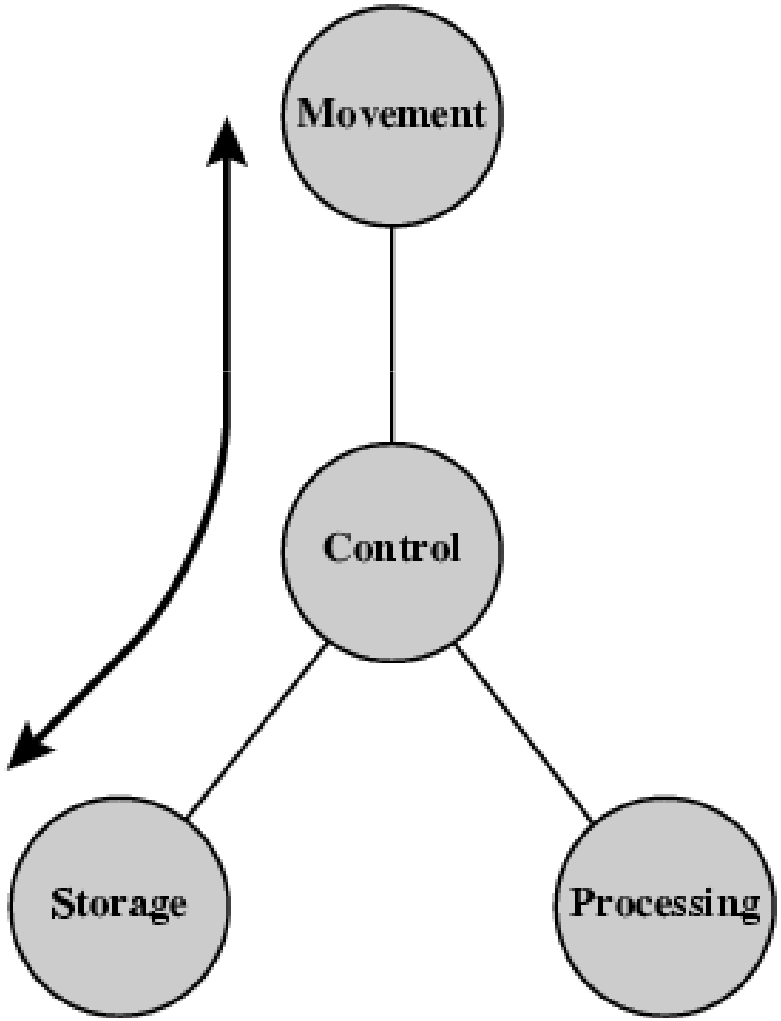
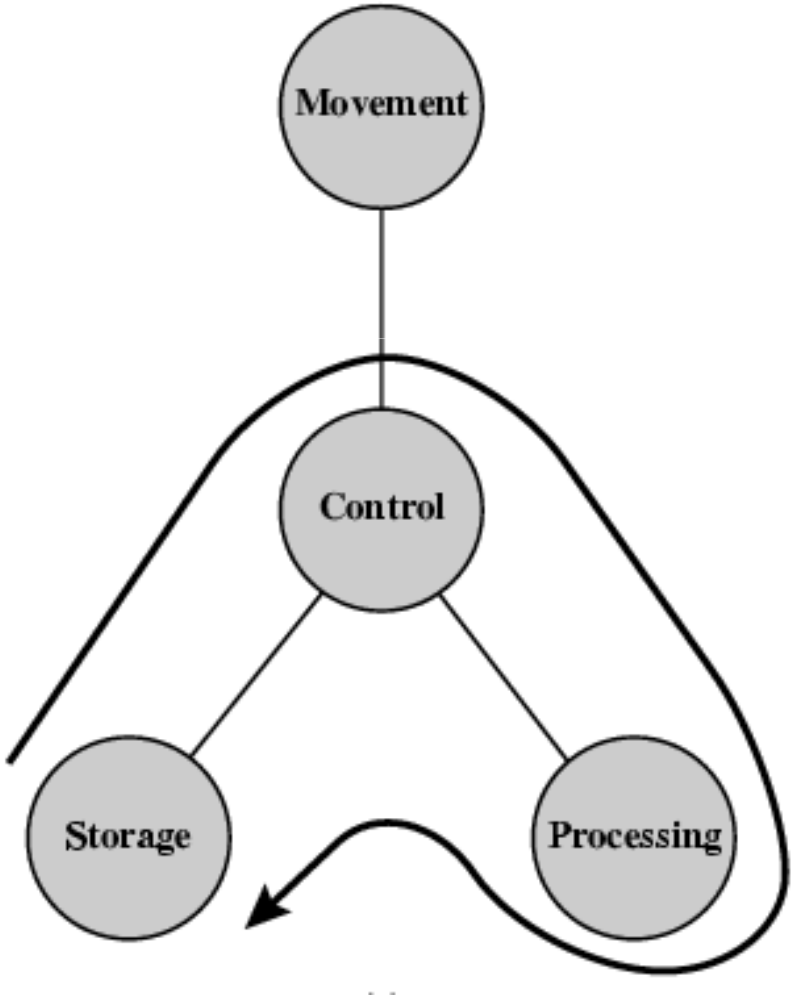
Operations (a) Data movement



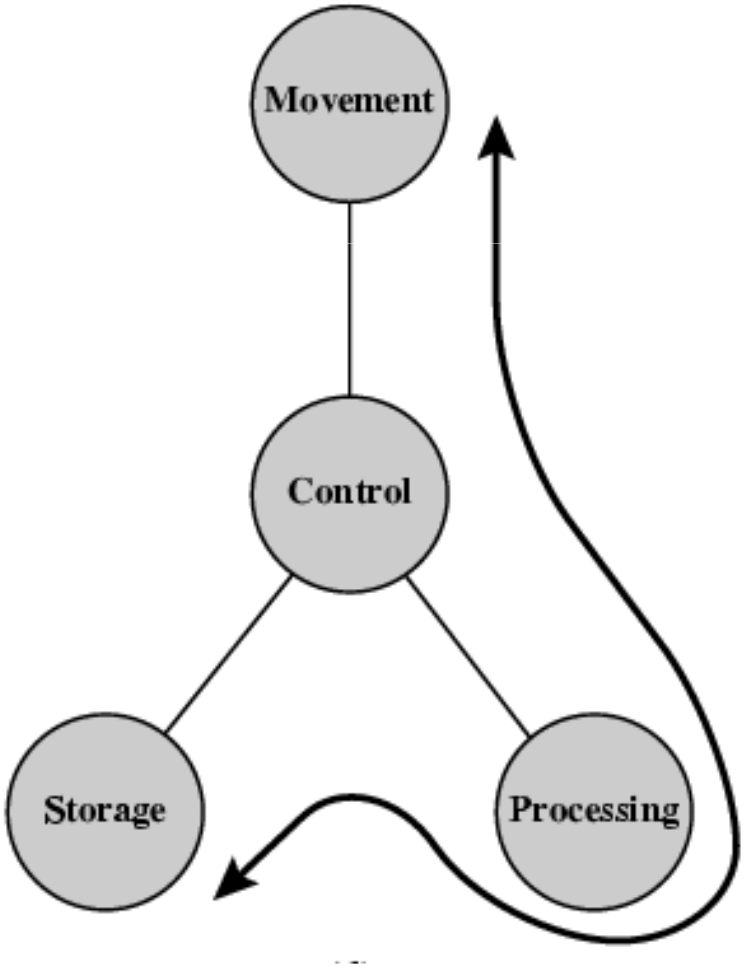
Operations (b) Storage



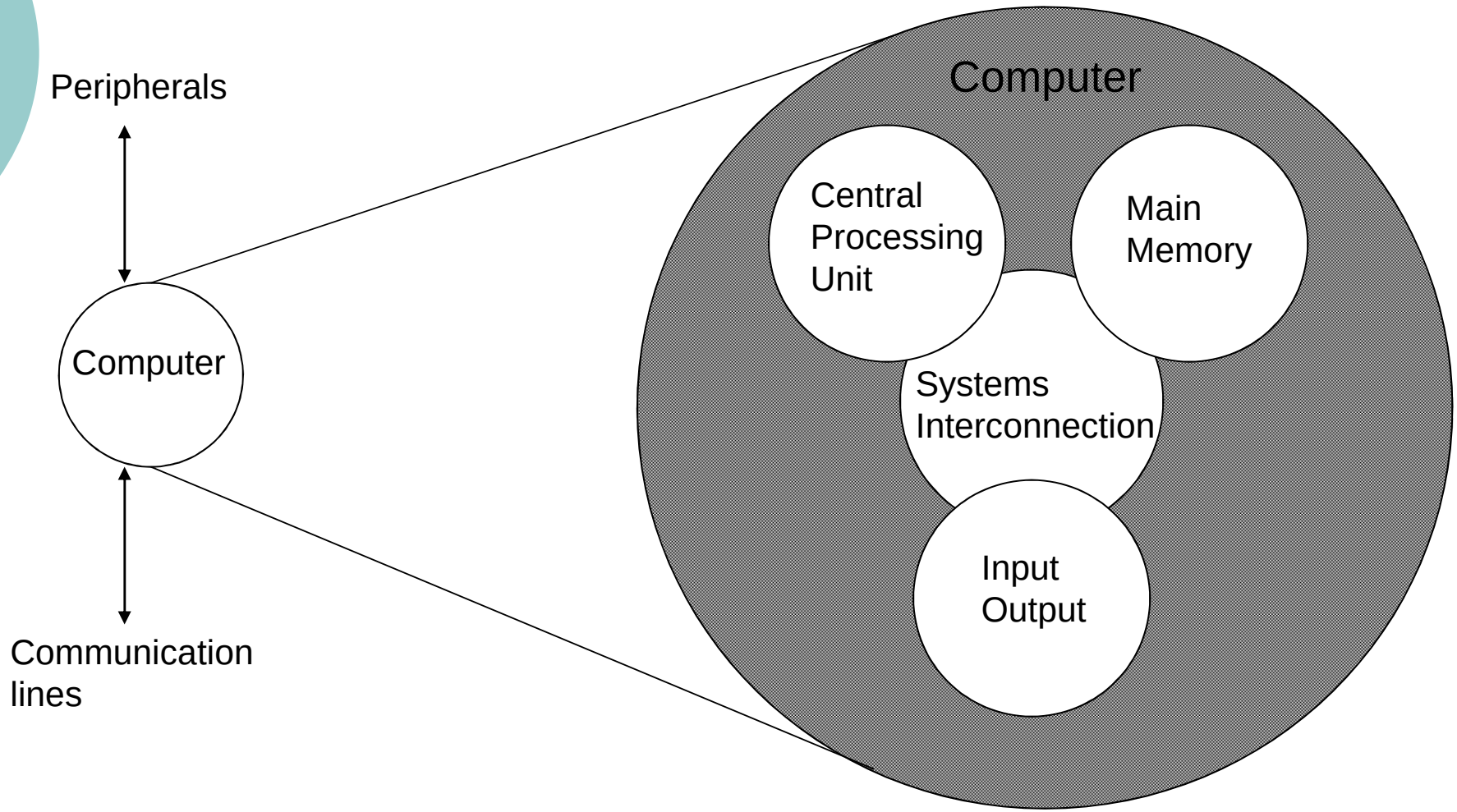
Operation (c) Processing from/to storage



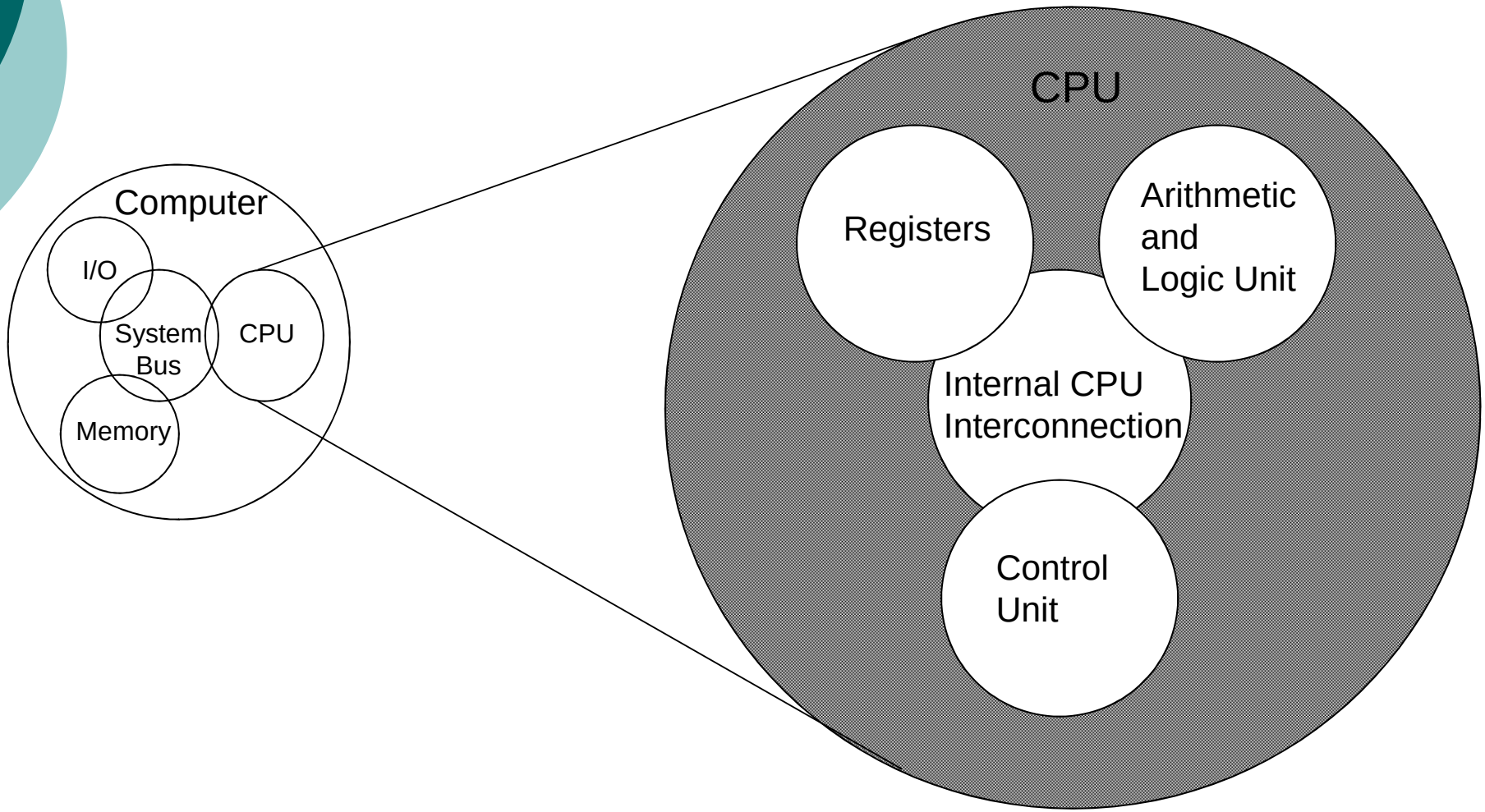
Operation (d)
Processing from storage to I/O



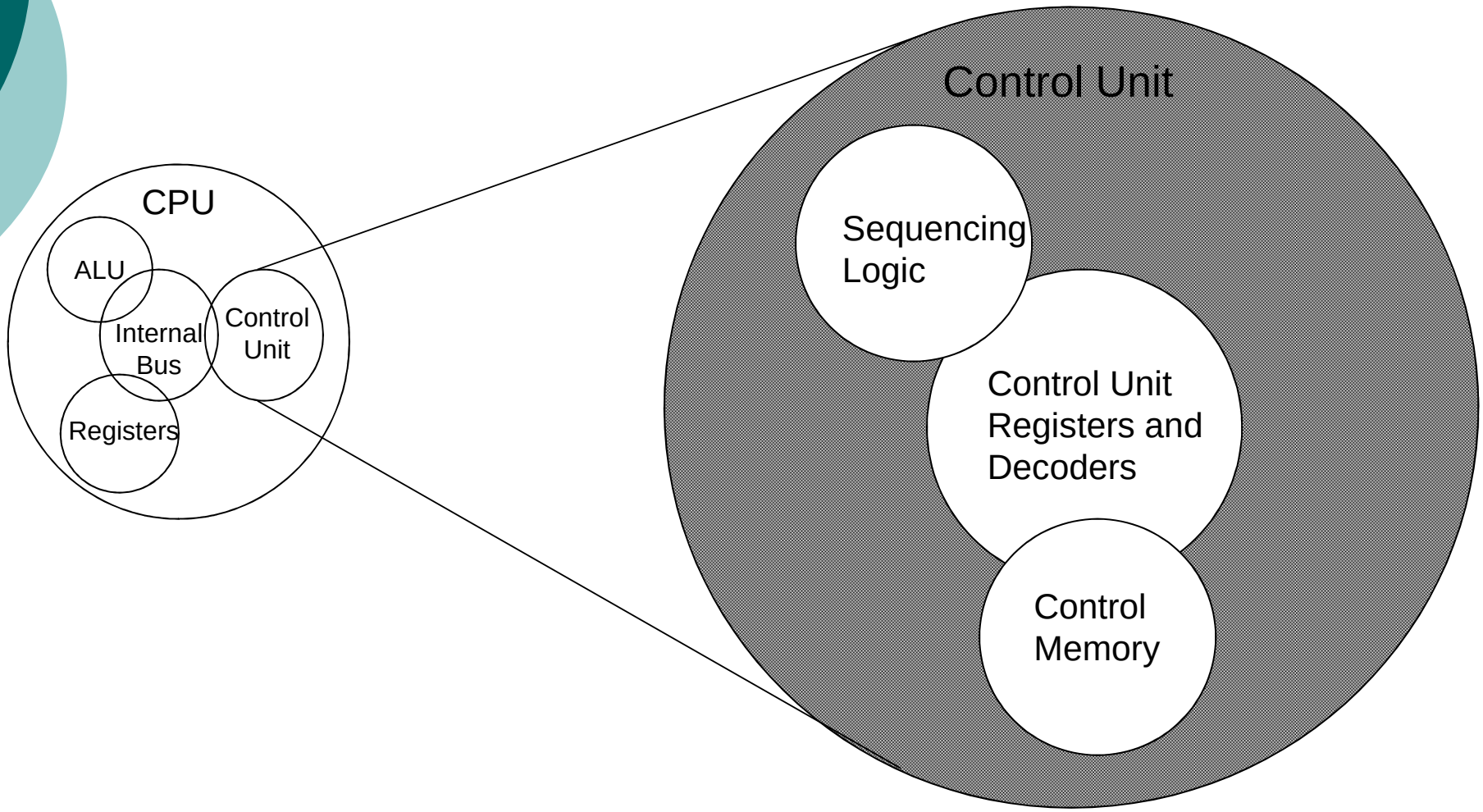
Structure - Top Level



Structure - The CPU



Structure - The Control Unit



Computer Architecture - Basics

Computer organization
- The region of system design from HLL and basic functionality to ISA (Instruction set architecture)

Computer architecture
- System design from ISA to VLSI specification

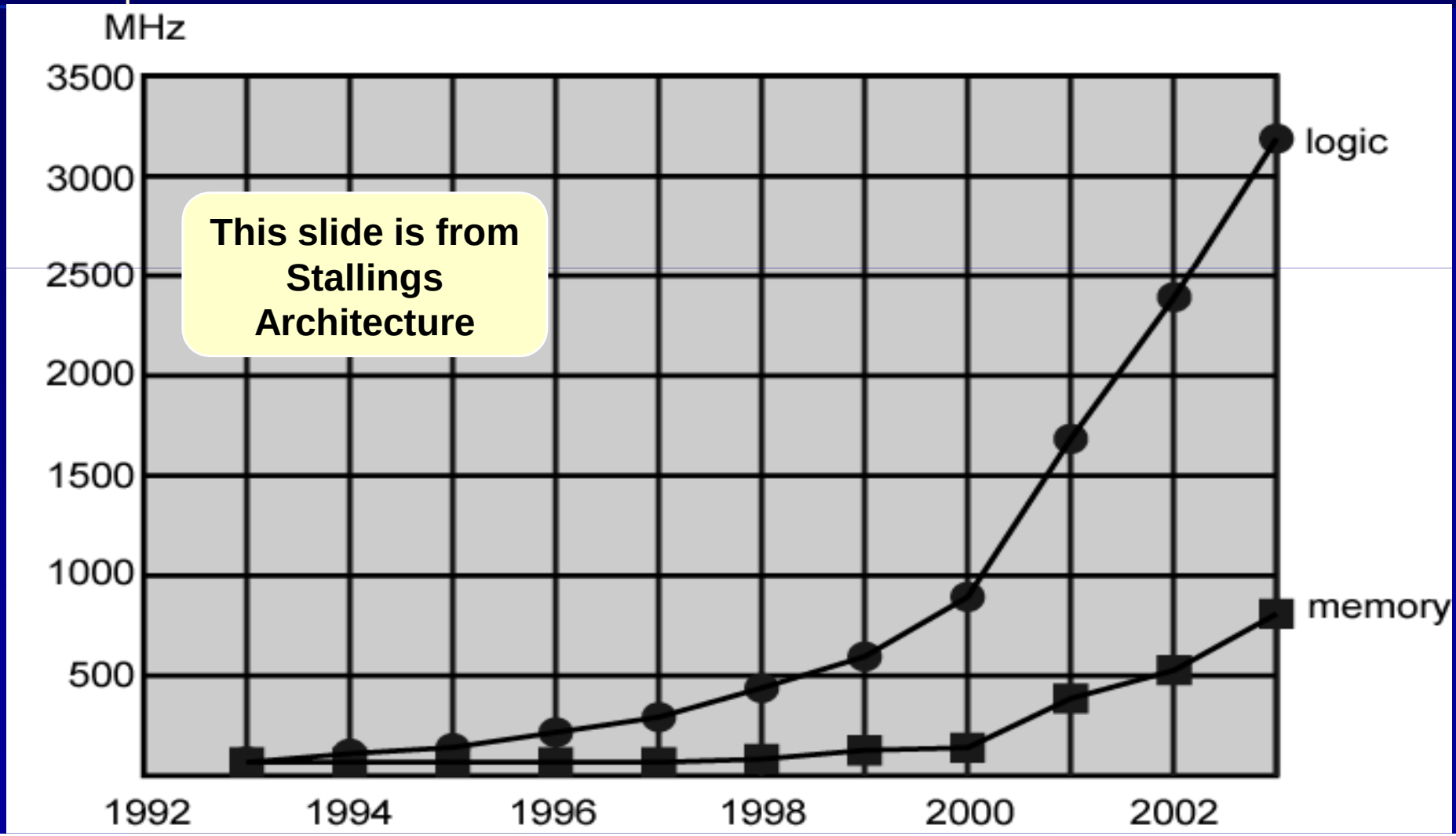
ISA (Instruction Set Architecture)
- Registers and memory organization
- Instruction formats
- Addressing modes
- Instruction set
- Exception and interrupt handling

This slide is from Heuring and Jordan

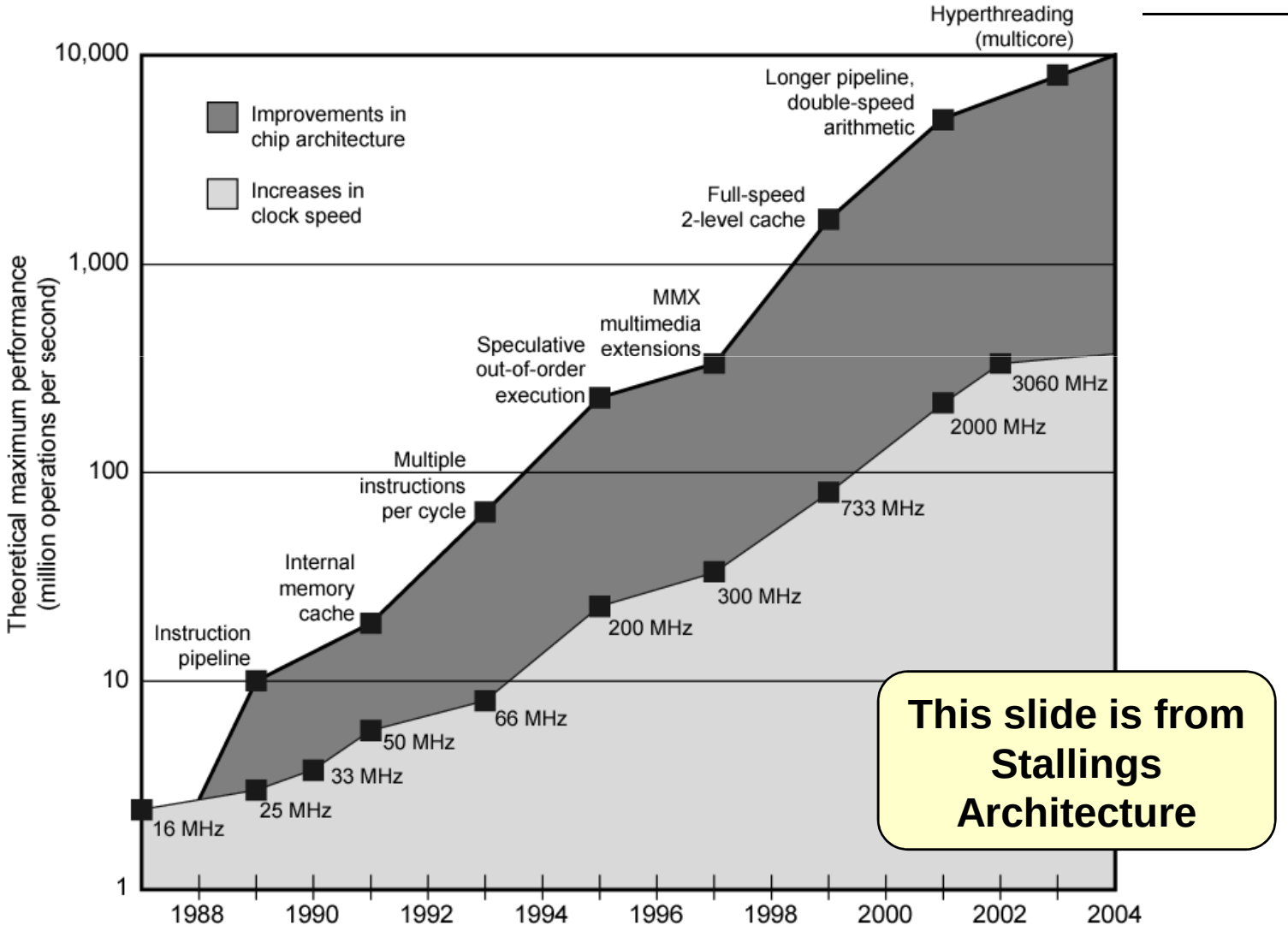
Logic and system performance, then and now

- Comments
  - Logic speed has improved much more than memory speed – one solution – cache memory
  - This slide doesn’t show density improvement
  - In the intel performance slide
    - Light gray area shows process improvement
    - Dark gray is what organization and architecture accomplished
- Both figures are copied from Stallings architecture book

Logic and Memory Performance Gap



Intel Microprocessor Performance



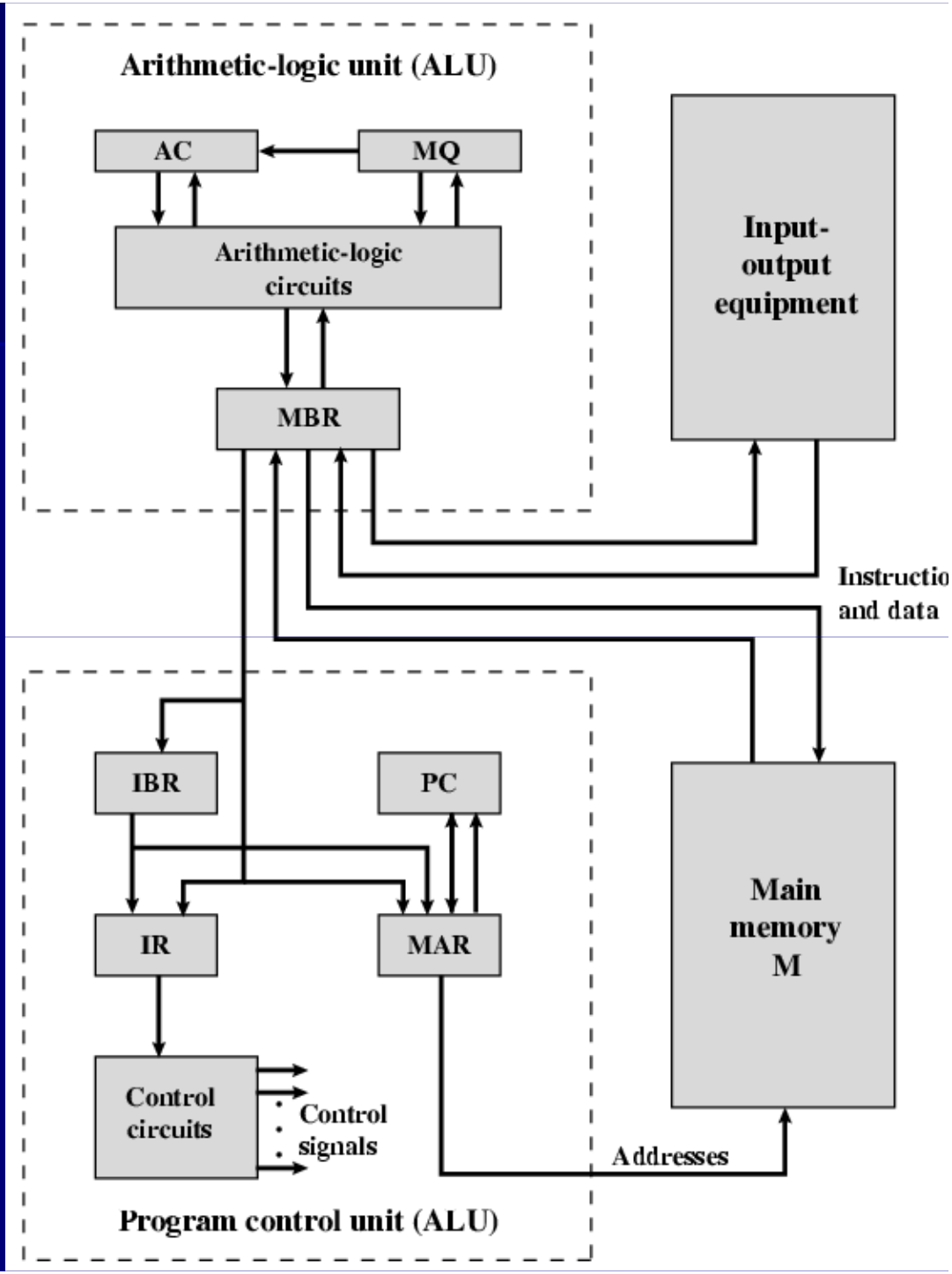
This slide is from Stallings Architecture

Processor structure – then and now

- The first slide is the 1946 IAS (institute for advanced studies – Princeton) machine
  - Actually, Von Neumann wrote a paper based on the ENIAC architecture and got the credit
  - This is almost the unavoidable basic structure of a stored-program machine
  - Many copies of the IAS machine were made – some were in service until 1967
- The second slide is a modern architecture showing:
  - Multiple cores
  - Caches
  - Interconnect
- Note that the original IAS ideas are still there

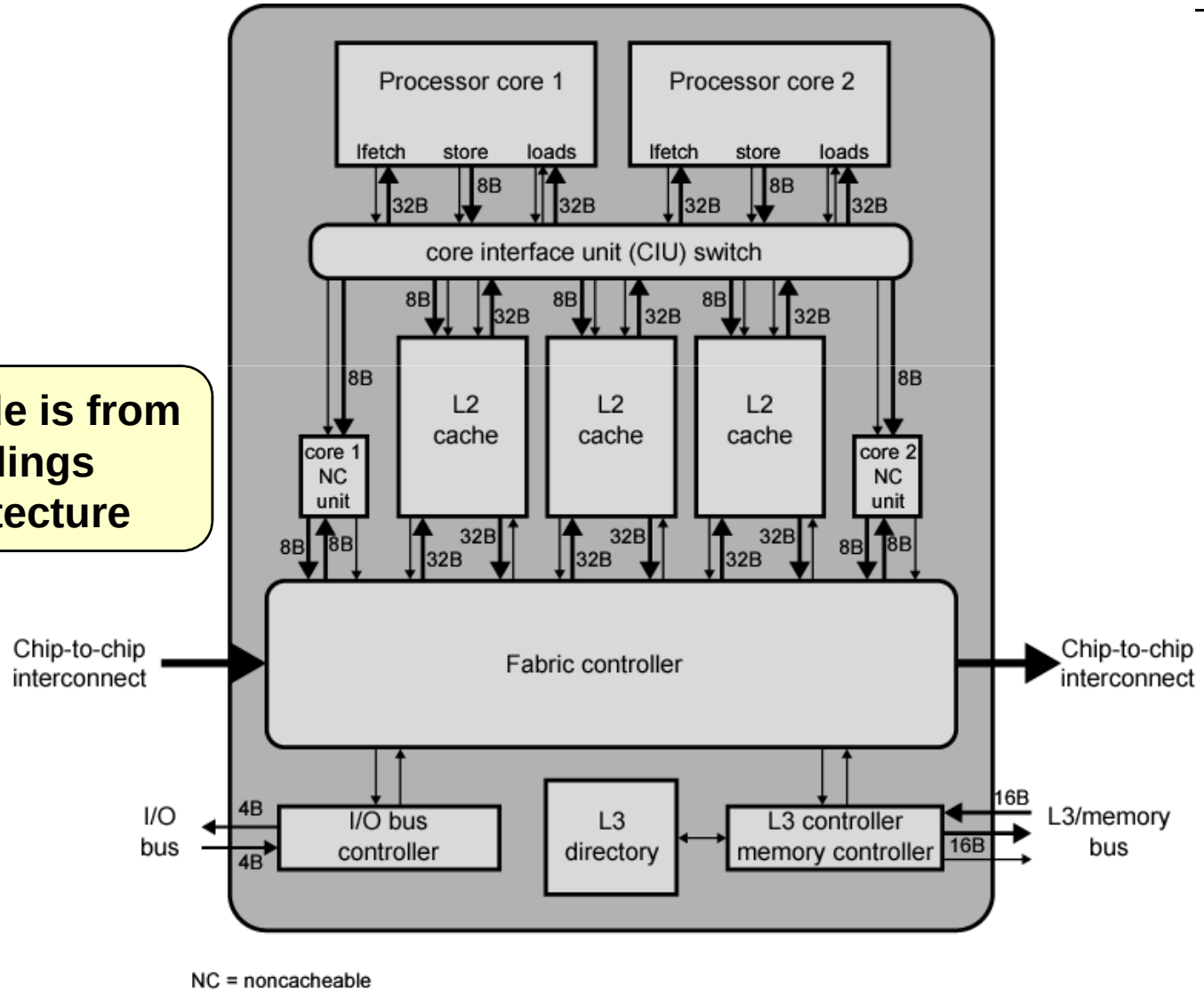
Structure of IAS (1946) – detail

This slide is from Stallings Architecture



POWER4 Chip Organization

This slide is from Stallings Architecture



Course Goals: Understanding Structure and Function of Digital Computer at 3 Levels

- Multiple levels of computer operation
  - Application level
  - High Level Language(s), HLL, level(s)
  - **This course**
    - Assembly/machine language level: instruction set
    - System architecture level: subsystems & connections
    - Digital logic level: gates, memory elements, buses
  - Electronic design level
  - Semiconductor physics level
- Interactions and relations between levels
  - View of machine at each level
  - Tasks and tools at each level
- Historical perspective
- Trends and research activities

This slide is from Heuring and Jordan

Prerequisites

- Experience with a high level language
  - Java
  - C, etc.
- Assembly language programming
- Digital logic circuits
  - Appendix A summarizes logic design in sufficient detail so the text can be used in courses without digital logic circuits as a prerequisite.

This slide is from Heuring and Jordan

Text Overview

1: The General Purpose Machine
2: Machines, Machine Languages, and Digital Logic
3: Some Real Machines
4: Processor Design at the Gate Level
5: Processor Design - Advanced Topics
6: Computer Arithmetic and the Arithmetic Unit
7: Memory System Design
8: Input and Output
9: Peripheral Devices
10: Communications, Networking and the Internet

This slide is from Heuring and Jordan

Course Overview – Basic aspects

1: The General Purpose Machine
   - ISA (Instruction Set Architecture)
   - The architect's view
   - The Logic designers view

2: Machines, Machine Languages, and Digital Logic
   - SRC (Simple RISC Computer) an example for the entire course
   - RTN (Register Transfer Notation) – a simple language that describes from ISA to logic

3: Some Real Machines

Speedup methods – pipelining and parallelism

- 4: Processor Design at the Gate Level
  - This introduces
    - Stages of an instruction – Fetch, Decode, Operand Fetch, Execution, Writeback
  - The LogicWorks version of the SRC will be the primary example
- 5: Processor Design - Advanced Topics
  - The crux chapter – this introduces
    - Pipelining
    - Instruction-level parallelism
  - Microcoded control units
    - A processor within a processor

Components – arithmetic and memory

- 6: Computer Arithmetic and the Arithmetic Unit
  - Arithmetic operations and types
    - Integer
    - Floating point
    - Specialized – logic operations and bit fiddling
  - Design or arithmetic units
- 7: Memory System Design
  - Memory cells – static/dynamic, RAM/ROM variants
  - Memory organization – SDRAM and DDR RAM examples
  - Cache memory organization

Components again – I/O and peripherals

8: Input and Output

- Primarily how the processor handles interrupts, exceptions and DMA

9: Peripheral Devices

- Just background information

10: Communications, Networking and the Internet

- Not covered in this course – others cover it well