ICOM 4215 Project 2 Spring 2012 Processor ALU

Today: March 28, 2012

Due date: April 13, 2012

Points: 100 points (Penalties: Next day: -10 points, Two days late: -25 points, Three days late: -40 points, Four days late or more: not accepted)

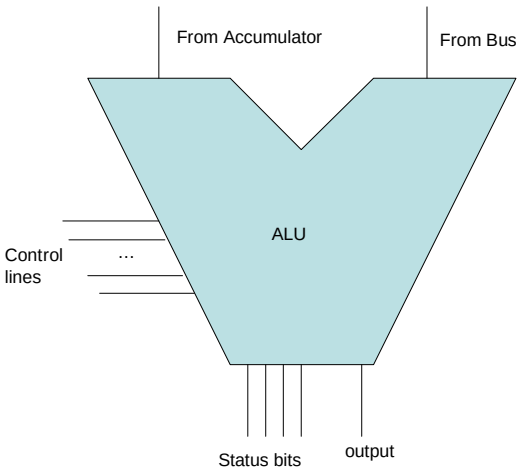
Group project – Three students per group

Submission:

- Via oral exam, aka "Happy Hour".
- Report, via email, subject on the email: Project 2 ICOM 4215, students will lose 5 points if the subject is changed. Send the email to nayda@ece.uprm.edu. Email due time, 11:59pm.

Project

Design an ALU for the RISC AR4 and test your design. The ALU implements arithmetic and logic operations Most of the arithmetic or logic operations will require two operands. Implement the functional units that support the ALU (multiplier and adder) and then the rest of the ALU. The ALU will include the logic necessary to implement the `and, or, xor, addc, sub, mac, neg, not, rlc, rrc,` and `inc2.`



The language to implement the Project will either be Verilog or VHDL (your Choice). I expect a structural design. The design should be clear enough to understand its components. We suggest you implement a testbench for input of the test signals.