ICOM 4215 Project 2 Spring 2013 Processor ALU and Controller

Today: April 22, 2013

Due date: May 10, 2013

Points: 100 points (Penalties: Next day: -10 points, Two days late: -25 points, Three days late: -40 points, Four days late or more: not accepted)

Group project – Three students per group

Submission:

- Via oral exam, aka "Happy Hour".
- Report, via email, subject on the email: Project 2 ICOM 4215, students will lose 5 points if the subject is changed. Send the email to naydag.santiago@upr.edu. Email due time, 11:59pm.

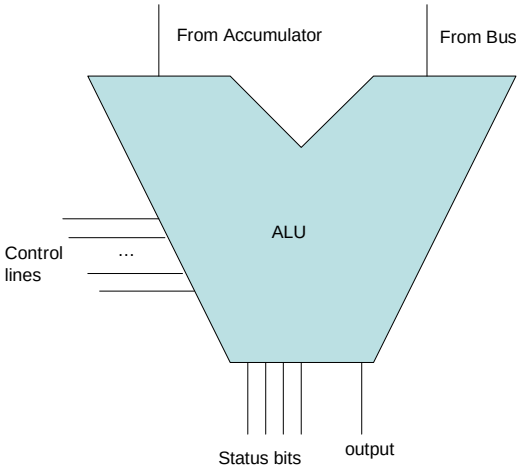
Project

Design an ALU and the Controller for the RISC AR5 previously described in project 1. Simulate.

Project Requirements

ALU

The ALU implements arithmetic and logic operations Most of the arithmetic or logic operations will require two operands. Implement the functional units that support the ALU (multiplier and adder) and then the rest of the ALU. The ALU will include the logic necessary to implement the and, or, addc, sub, mul, neg, not, rlc, rrc, and inc2.



Controller

Your team will design all the components of the complete processor and determine the control lines. As deliverable your group needs to specify all the components of the processor and the controller design and behavior. We will work with a 1-bus architecture. In addition, each group will have a different processor design; therefore, the controller's characteristics are different.

To make it clear: in order to generate the controller, you must know all the parts of your processor, but only the controller and the ALU will be simulated in a hardware description language.

The language to implement the Project will either be **Verilog or VHDL** (your Choice). I expect a structural design. The design should be clear enough to understand its components. We suggest you implement a testbench for input of the test signals.

Report

The report will contain: detailed schematics of the processor design. Detailed explanation of the controller and ALU, timing diagrams showing the behavior of the controller and ALU, appendix containing the code developed in VHDL or VERILOG.

Oral Exam

The oral exam will be individually graded. Each student must demonstrate the proficiency and capability of designing a processor and a controller.