

# **Memory types and interfacing**

**Cell types (DRAM, SRAM, EEPROM, EPROM,  
PROM, and ROM)**

**Organization types**

**Interfacing to a bus**

# Memory - from the cell up

## Cell types - in decreasing order of forgetfulness

**DRAM - Dynamic RAM - remembers for 4ms or so**

**SRAM - Static RAM - remembers while the power is on**

**EEPROM - Static RAM that remembers even with power off**

**EPROM - Electrically programmable ROM**

**UVROM - Electrically programmable - UV erasable ROM**

**PROM - Programmable, just once**

**ROM - Factory programmed ROM**

## Organization types

**All are more-or-less square arrays of cells with addressing and read/write logic**

**Field programmables usually require an extra, higher programming voltage**

# Cells

## Basic Cell

- Selected by X and Y
- Outputs data when selected
- DRAM loses info when read
- SRAM, etc., retain info

## Cell array

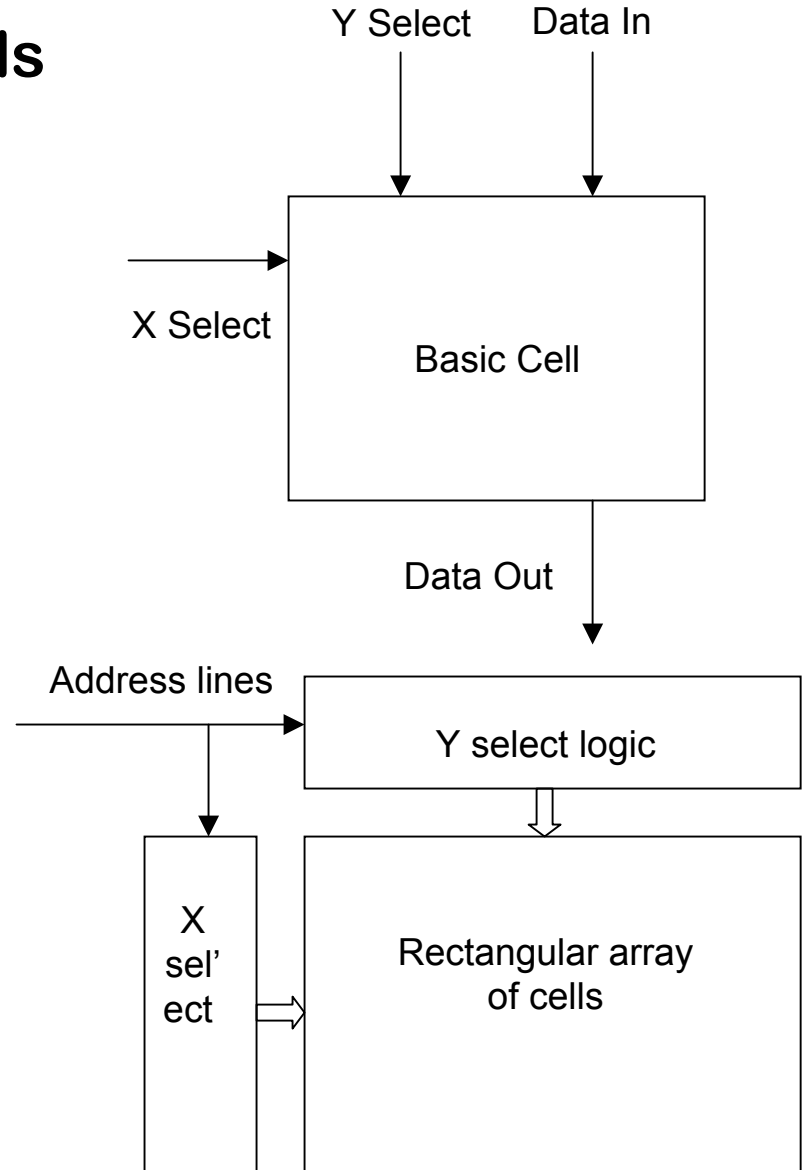
- More-or-less square array of cells

## Select logic

- Maps N address lines into 2-nth select lines

## Data logic

- Not shown
- Sends data to/from selected cell



# Memory organization and readout

## All nondynamic types

### Example, 2K x 8 memory

11 address lines

8 data lines

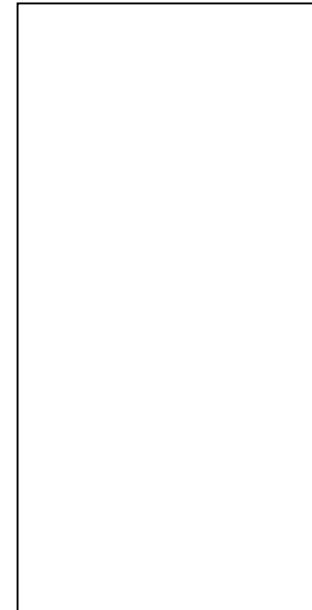
Read/Write

Chip select

Power

16K - 2 to 14th cells

128 x 128 array



# Memory organization and readout

## All dynamic types

### Example, 1M x 4 memory

1M ( $2^{20}$ ) address space

20 address lines (time-shared between row and column)

4 data lines

Read/Write

Row address strobe  
(RAS)

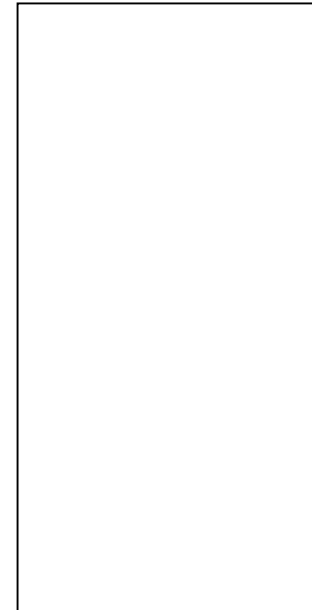
column address strobe  
(CAS)

Chip select

Power

4M - ( $2^{22}$ ) cells

256 x 256 x 4 array



# Memory cycle – dynamic RAM

## Steps in a read cycle

Lower bits of address (row address) asserted, then edge-triggered in by RAS

Entire row is transferred (destructively) to row buffer

Upper bits of address (row address) asserted, then edge-triggered in by CAS

Selected 4 bits are gated to output pins

Entire row buffer is transferred back to memory cells of row

## Steps in a refresh cycle

Lower bits of address (row address) asserted, then edge-triggered in by RAS

Entire row is transferred (destructively) to row buffer

Entire row buffer is transferred back to memory cells of row

# More memory cycles – dynamic RAM

## Steps in a write cycle (late write)

Lower bits of address (row address) asserted, then edge-triggered in by RAS

Entire row is transferred (destructively) to row buffer

Upper bits of address (row address) asserted, then edge-triggered in by CAS

Selected 4 bits of data are gated to selected bits of row buffer

Entire row buffer is transferred back to memory cells of row

## Read-modify-write

Data is read, new data is written

## Early write

Data is transferred along with strobcs rather than waiting for row transfer, then gated into row buffer

# Memory addressing details

## Wide-bus issues

### Example – MIPS

Memory is basically word-organized

This means bottom two bytes of address bus are always 0 for a full-word operation

Specialized write cycles

- Single-byte (byte 0, 1, 2, or 3)

- Left end (1,2, or 3 bytes)

- Right end (1,2, or 3 bytes)

For these transfers data normally emerges from CPU on the correct lines for the byte

## Wide-bus, narrow memory or device

Example – byte- or halfword-oriented interface on word-wide bus

Data must emerge on low-order bytes of bus – not like odd-byte read of memory

This logic is normally part of the I/O bus structure – odd addresses in byte-wide bus cause data to be copied to/from low-order bytes

# Memory addressing details

## Alternatives to the logic

I/O register numbers are multiples of 2 or 4

This means register selects are connected to bits 2 to x of address bus

Common for memory-mapped interfaces

## Slow transfers

CPU can do NOP's while transfer occurs

Device or bus logic can request wait states

Often done by operating system – HLL outb, inw, etc. system calls take care of this

# Memory types in newer PC's

## DRAM

### Asynchronous

Clock cycle is of fixed minimum duration – slow transfer wastes an entire clock cycle

This category includes EDO (extended data output) – pre-1999

### Synchronous (usually called SDRAM)

Shares clock with CPU – CPU doesn't have to wait for next memory time slot

DDR-SDRAM – two transfers per clock cycle

Protocol-based – uses specialized bus (narrow, high-speed) for higher speeds (200 MHz)

### Parity and ECC (error-correcting code)

Parity is obsolescent

ECC is often used on servers

### Packaging

Most now use DIMM's (168-pin is 64 bits wide, 72-pin is 32)

This data is from *PC Hardware in a Nutshell*, Thompson & Thompson, O'Reilly, 2000