

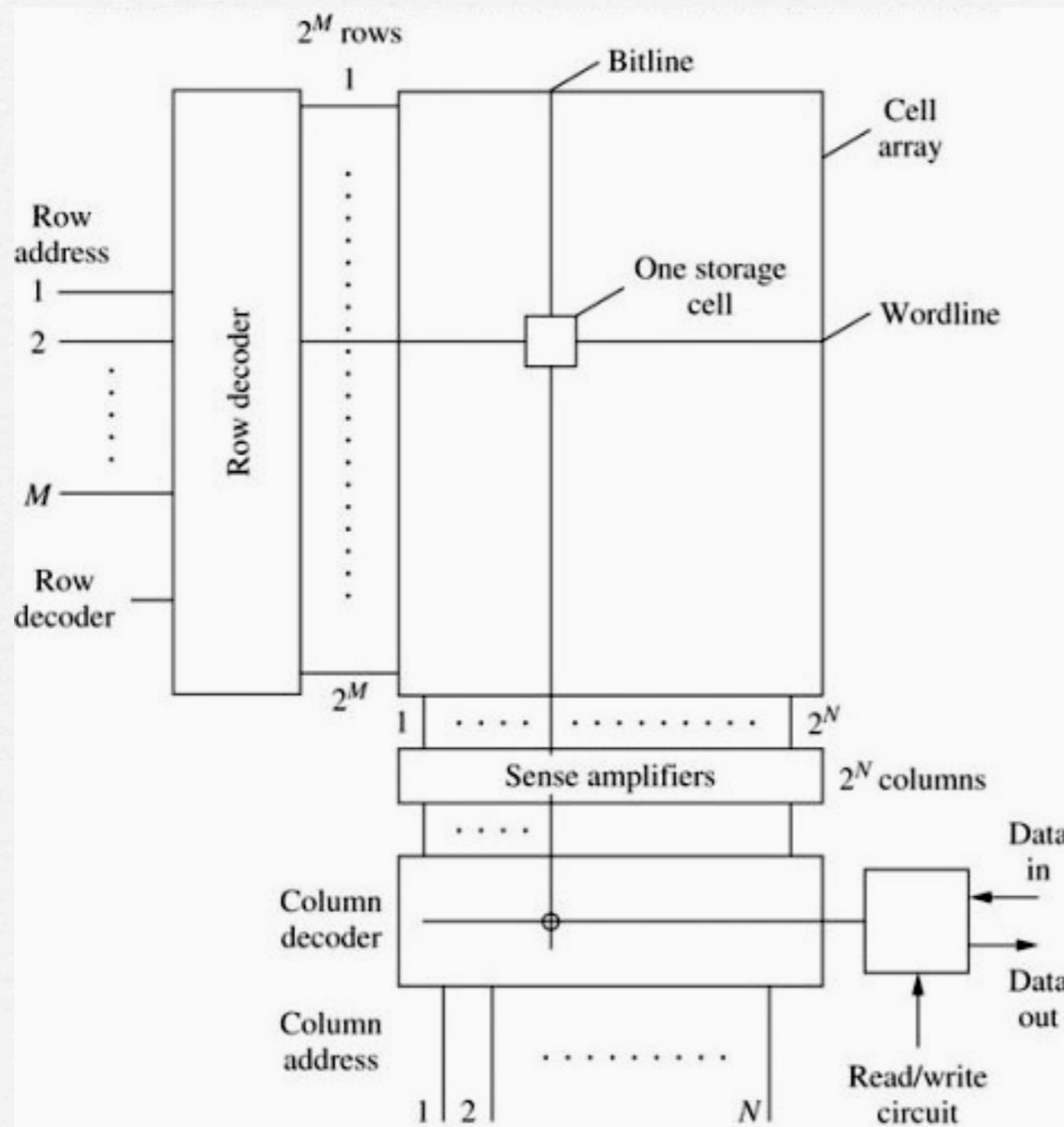
ROM Memory and Decoders

INEL4207 - April 27, 2011

Read-Only Memory (ROM)

- Non-volatile
- ROM is often needed in digital systems such as:
 - Holding the instruction set for a microprocessor
 - Firmware

A 256-MByte Memory Chip



- Memory block contains 2^{M+N} storage locations
- When a bit is selected,
 - sense amplifiers: used to read/write to the RAM location

NMOS NOR Address

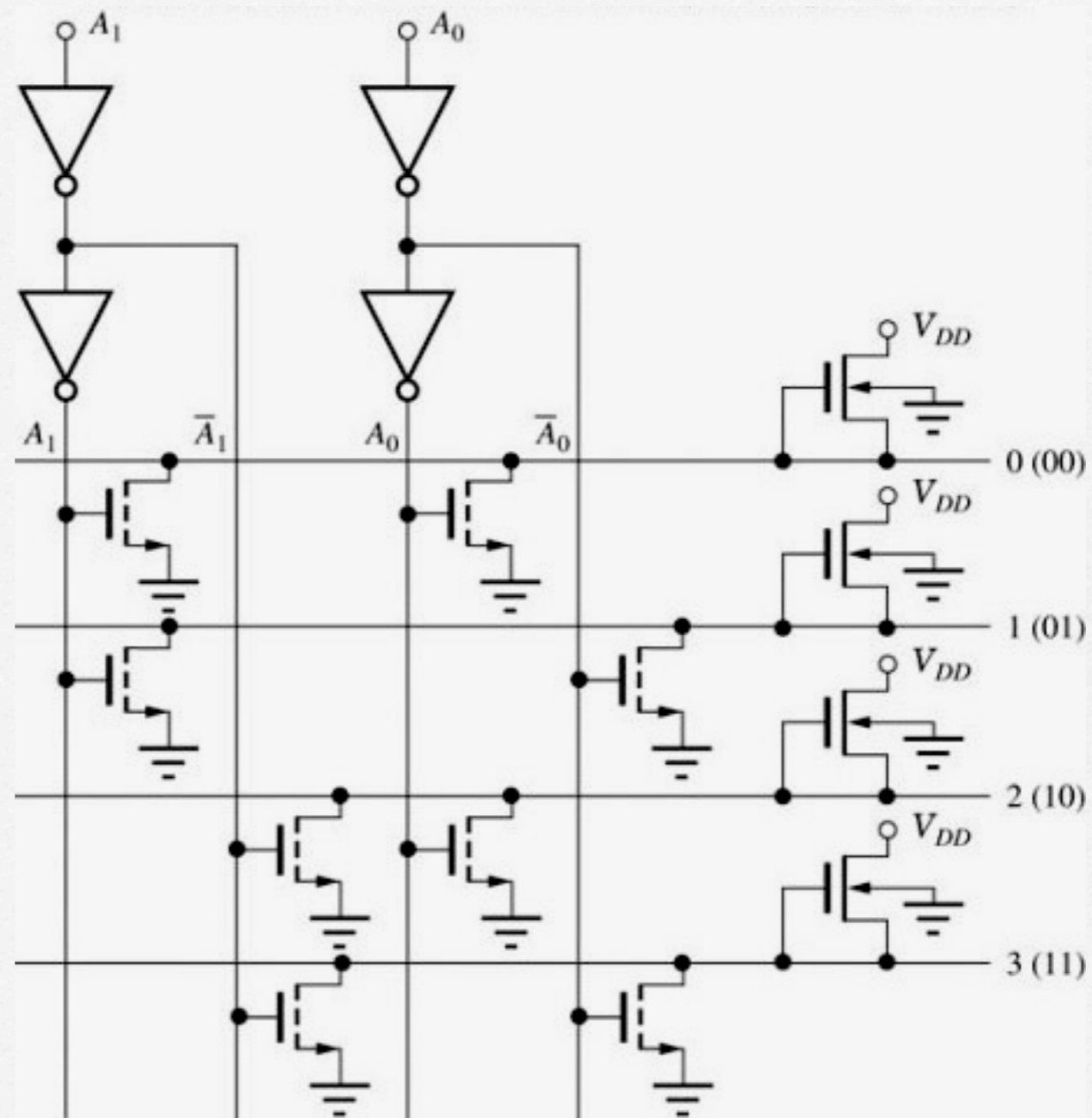
- Output 0 is high if both A_0 and A_1 are low

$$\text{ROW 0} = (A_1 + A_0)'$$

$$\text{ROW 1} = (A_1 + A_0')'$$

$$\text{ROW 2} = (A_1' + A_0)'$$

$$\text{ROW 3} = (A_1' + A_0')'$$



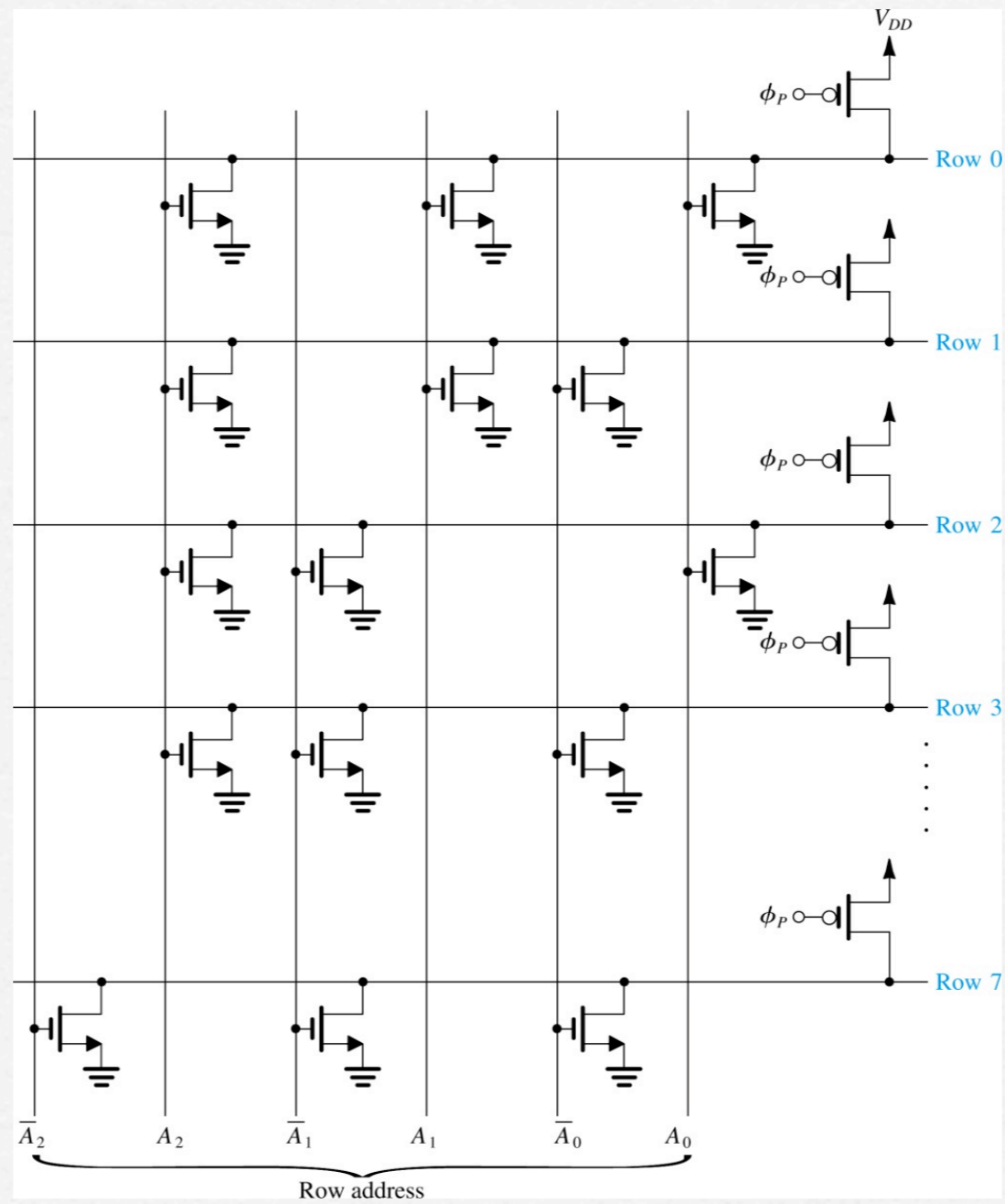


Figure 16.25 A NOR address decoder in array form. One out of eight lines (row lines) is selected using a 3-bit address.

NMOS NAND Address Decoders

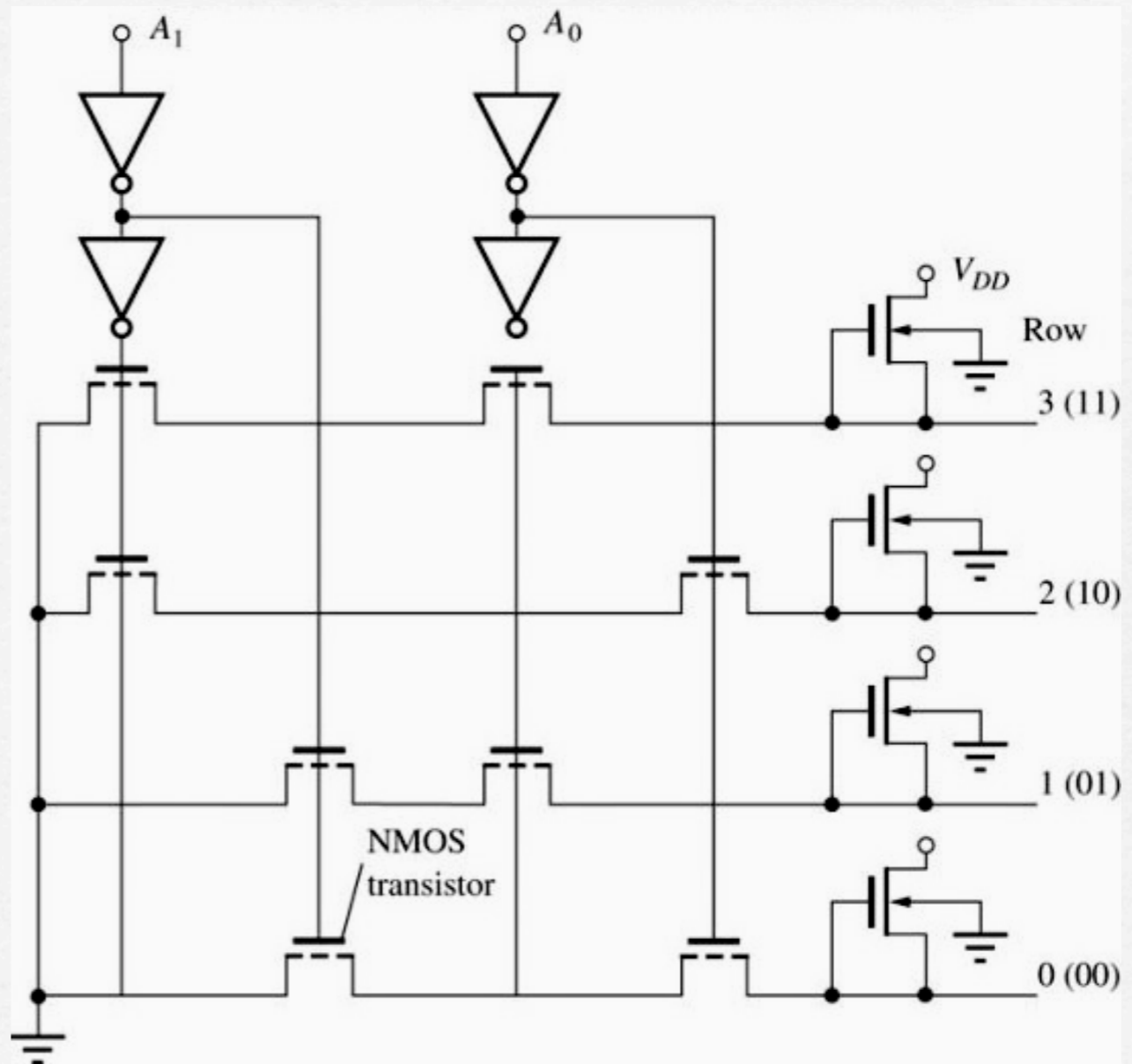
- Output 3 is low if both A_0 and A_1 are high

$$\text{ROW 0} = (A_1' A_0')$$

$$\text{ROW 1} = (A_1' A_0)$$

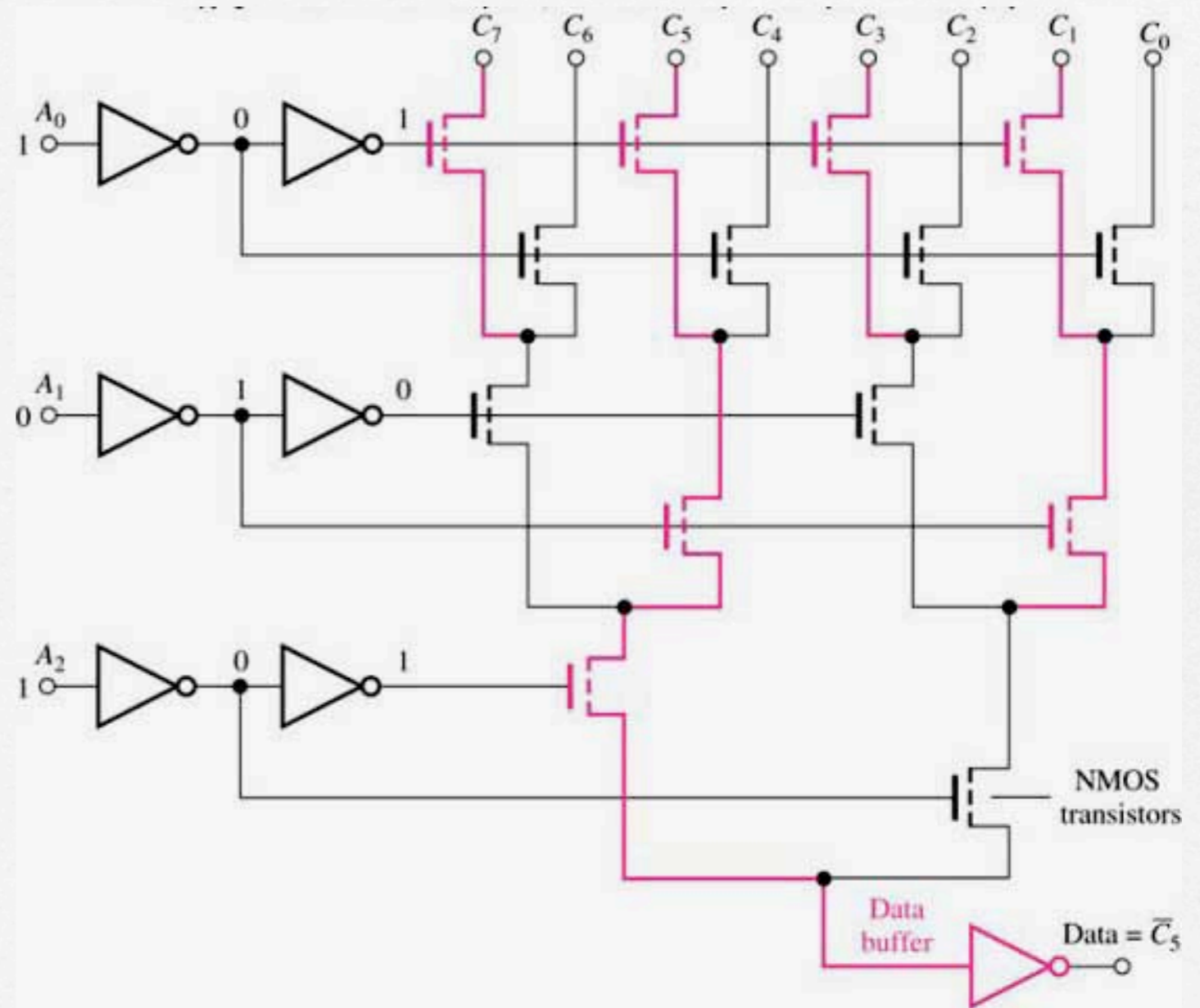
$$\text{ROW 2} = (A_1 A_0')$$

$$\text{ROW 3} = (A_1 A_0)$$



Pass-transistor Column Decoder

- 3-bit column data selector using pass-transistor logic



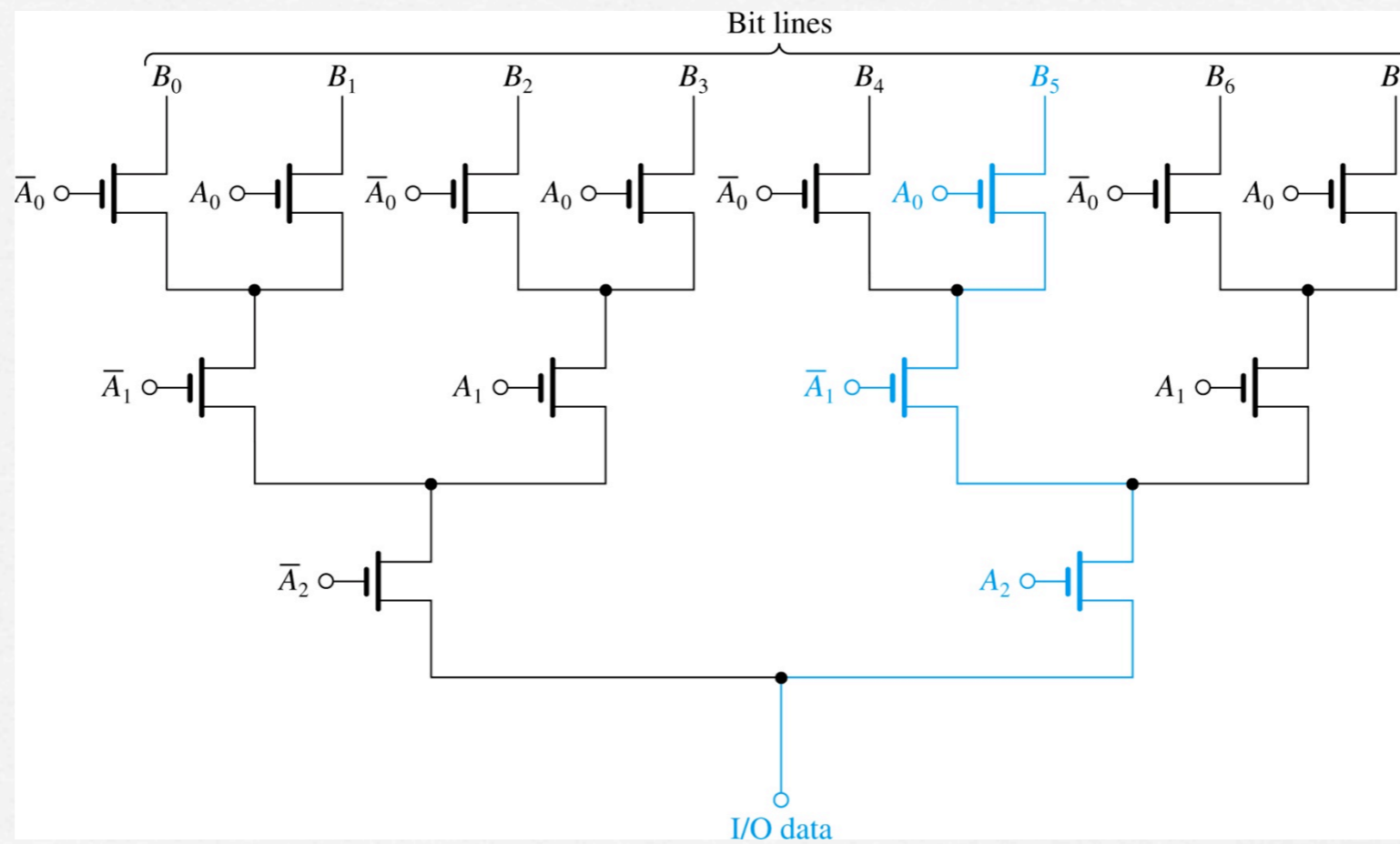


Figure 16.27 A tree column decoder. Note that the colored path shows the transistors that are conducting when $A_0 = 1$, $A_1 = 0$, and $A_2 = 1$, the address that results in connecting B_5 to the data line.

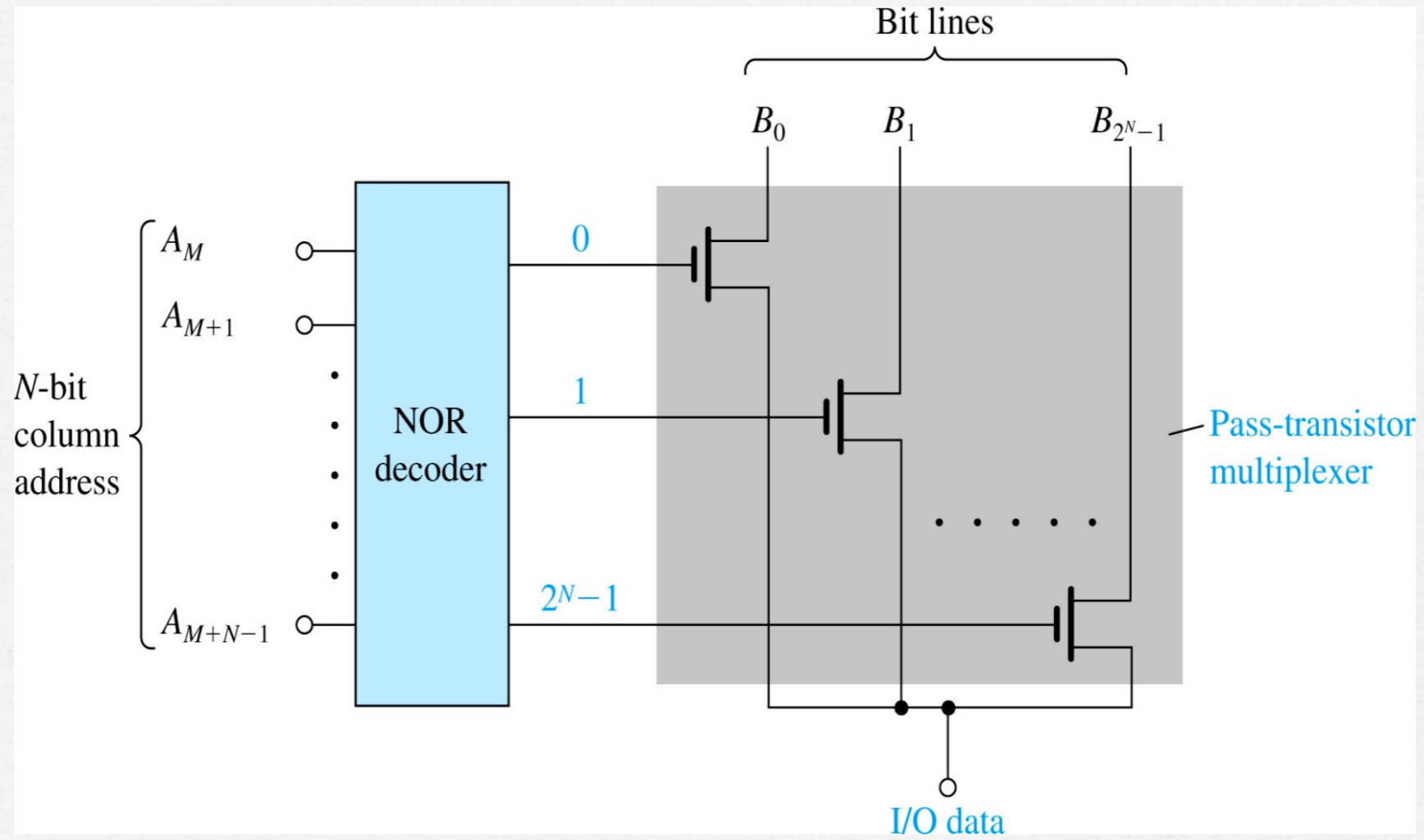
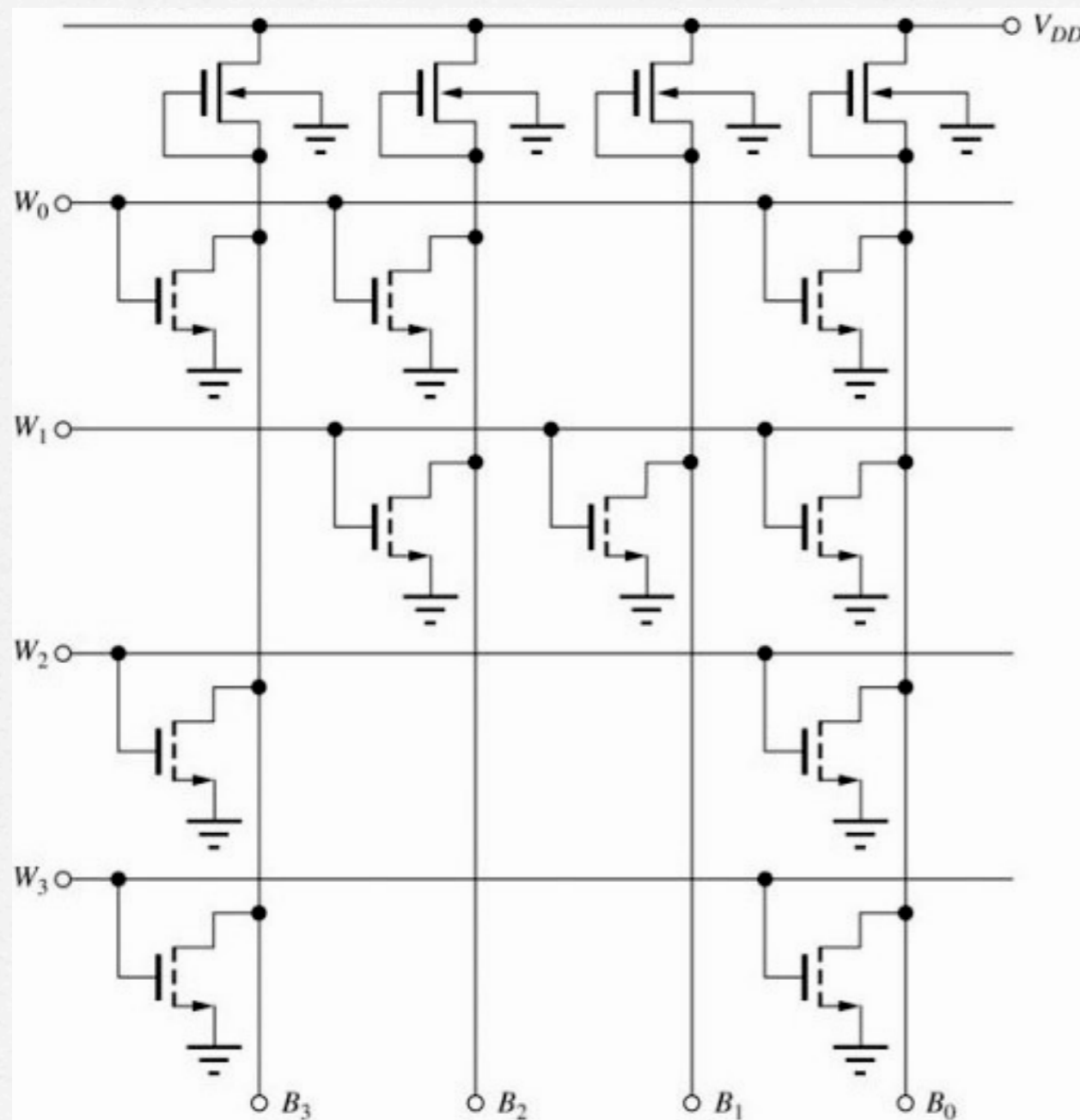


Figure 16.26 A column decoder realized by a combination of a NOR decoder and a pass-transistor multiplexer.

Read-Only Memory (ROM)



- The basic structure of the NMOS static ROM is shown in the figure
- The existence of a NMOS means a "0" is stored at that address otherwise a "1" is stored
- The major downfall to this particular circuit is that it dissipates a lot of power

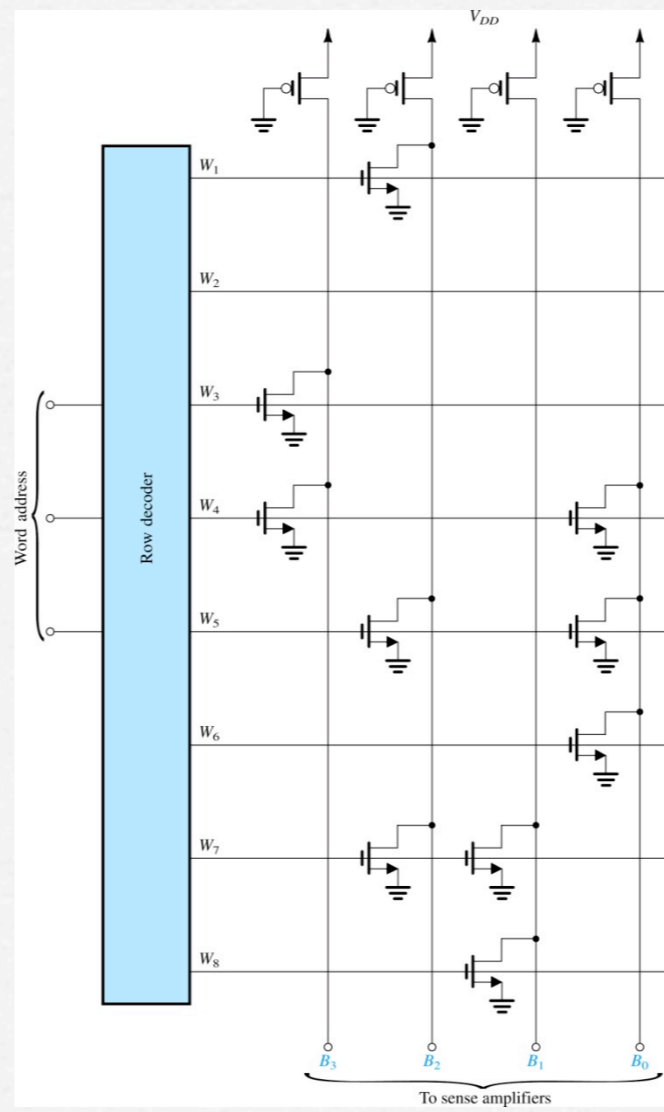
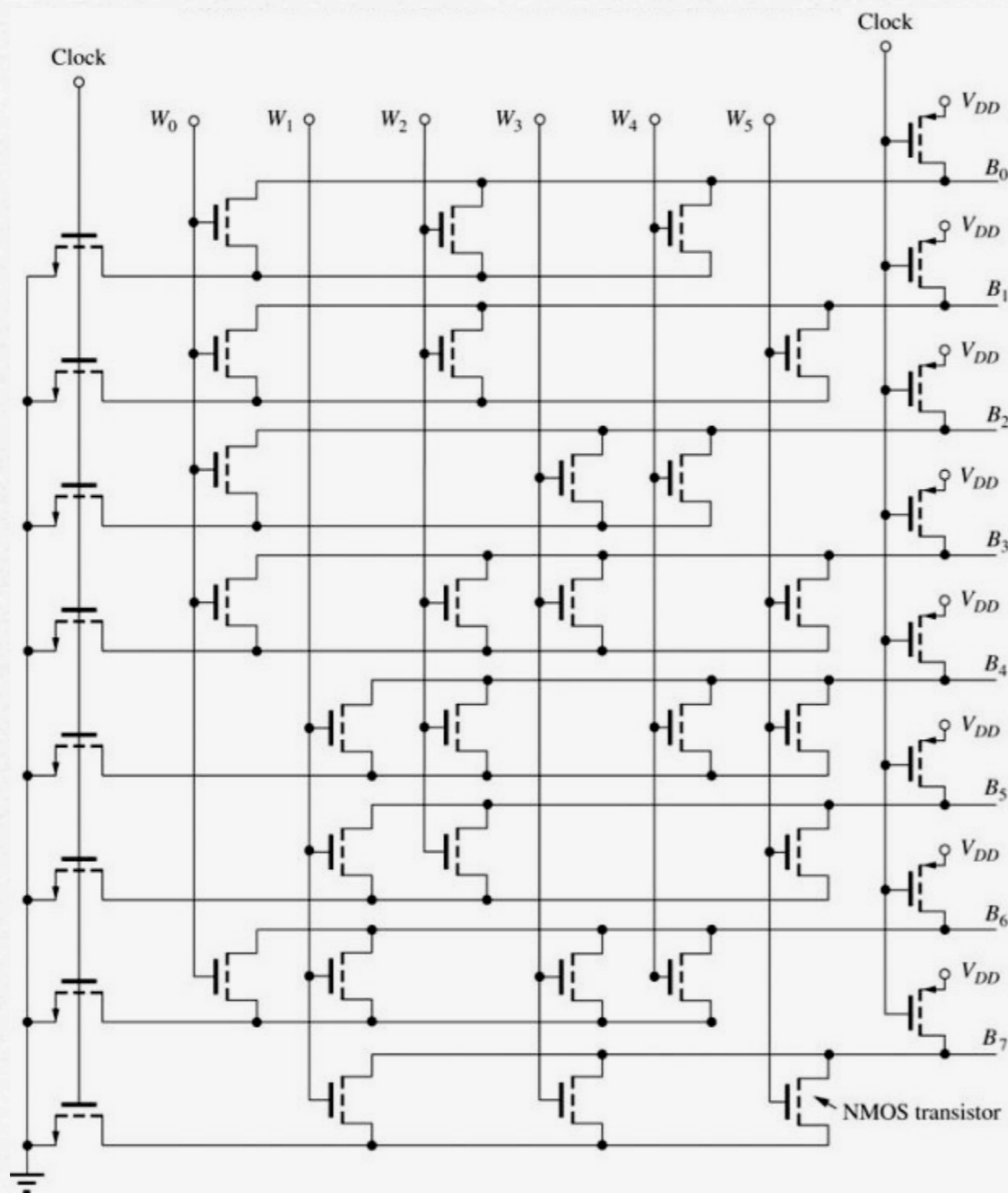
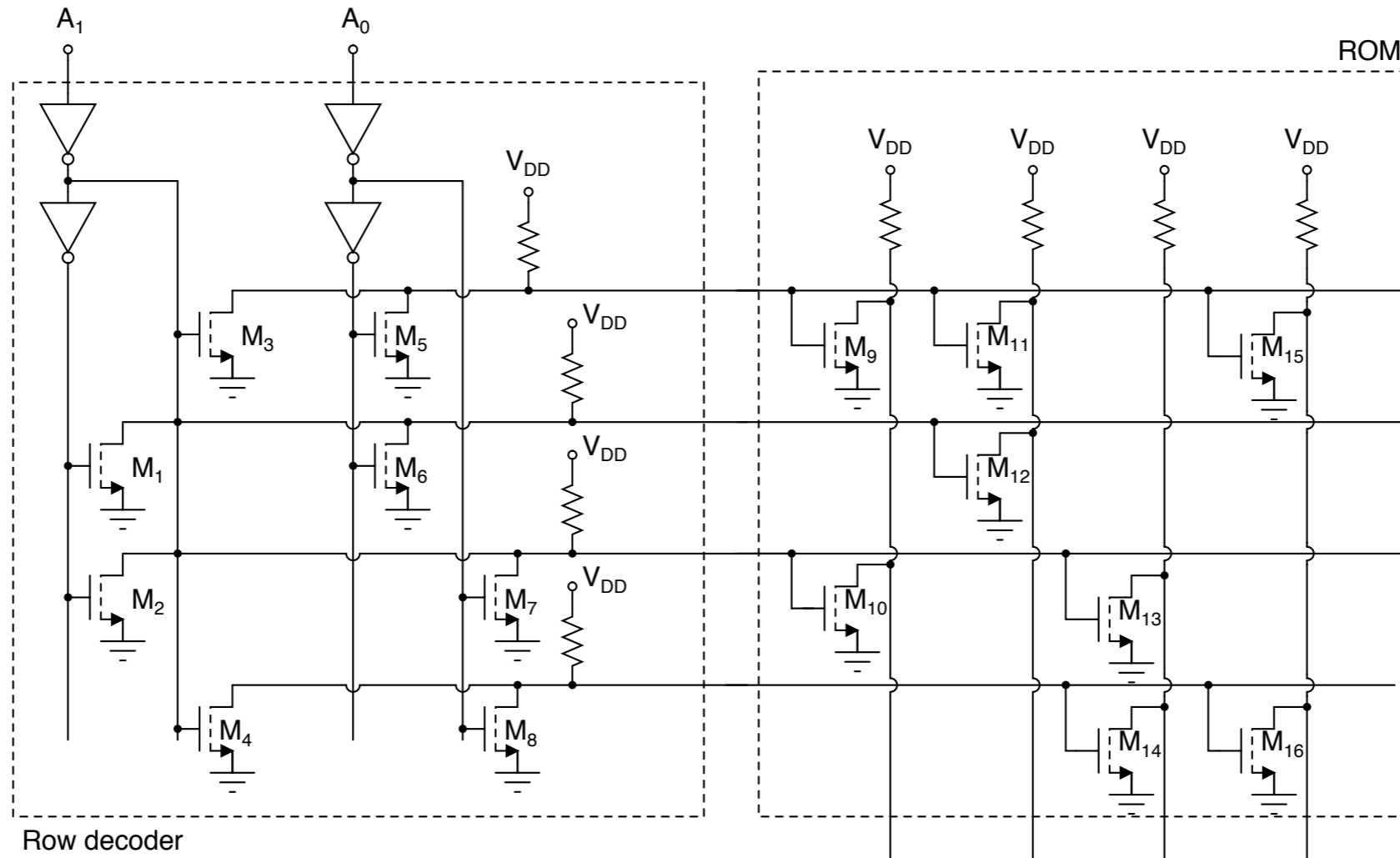


Figure 16.30 A simple MOS ROM organized as 8 words \times 4 bits.

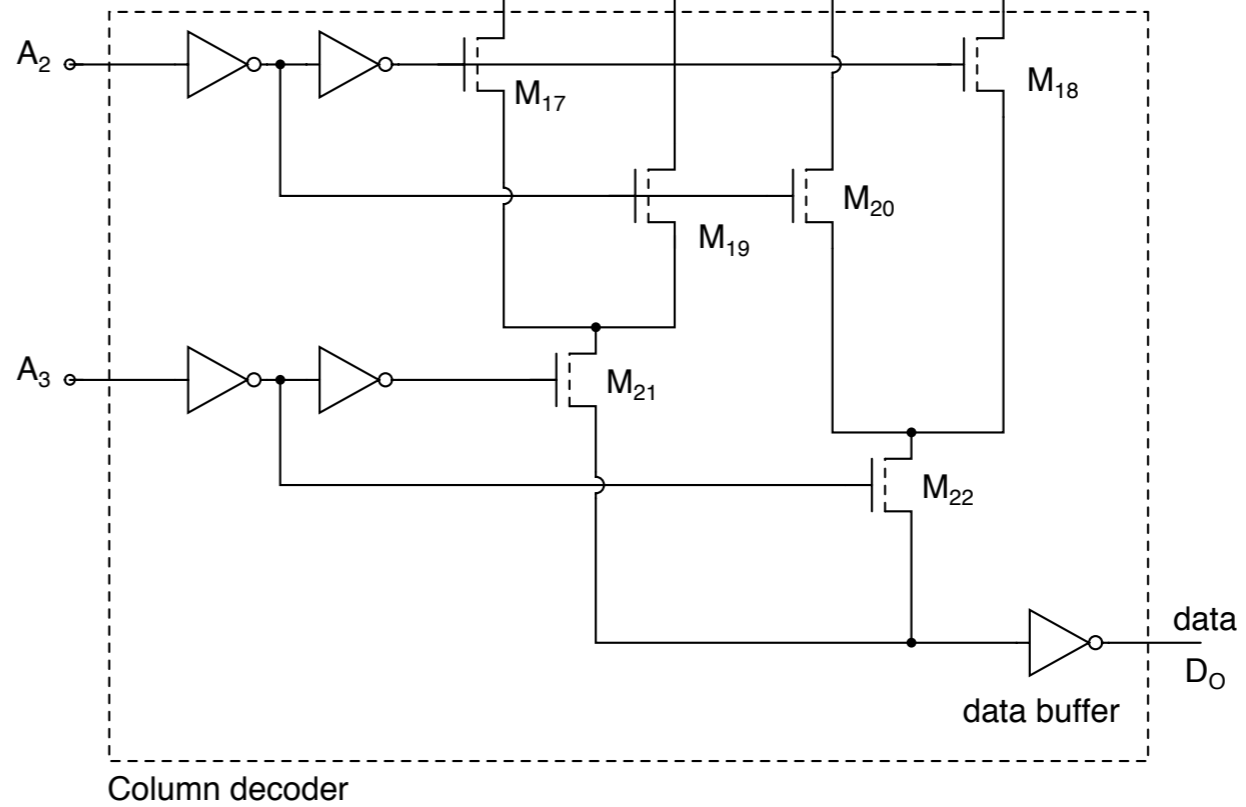
Read-Only Memory (ROM)

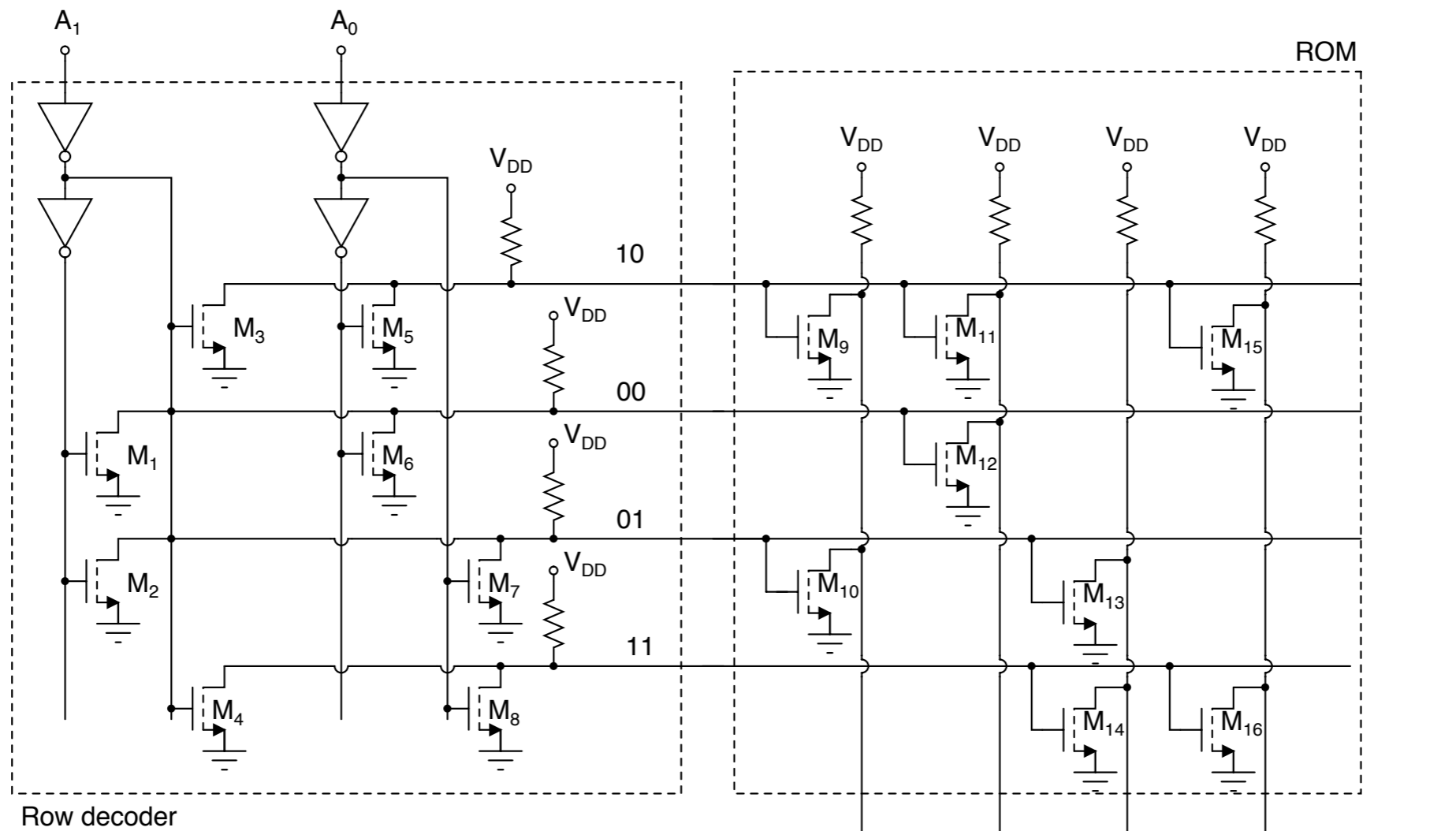


- The domino CMOS ROM is one technique used to lower the amount of power dissipation

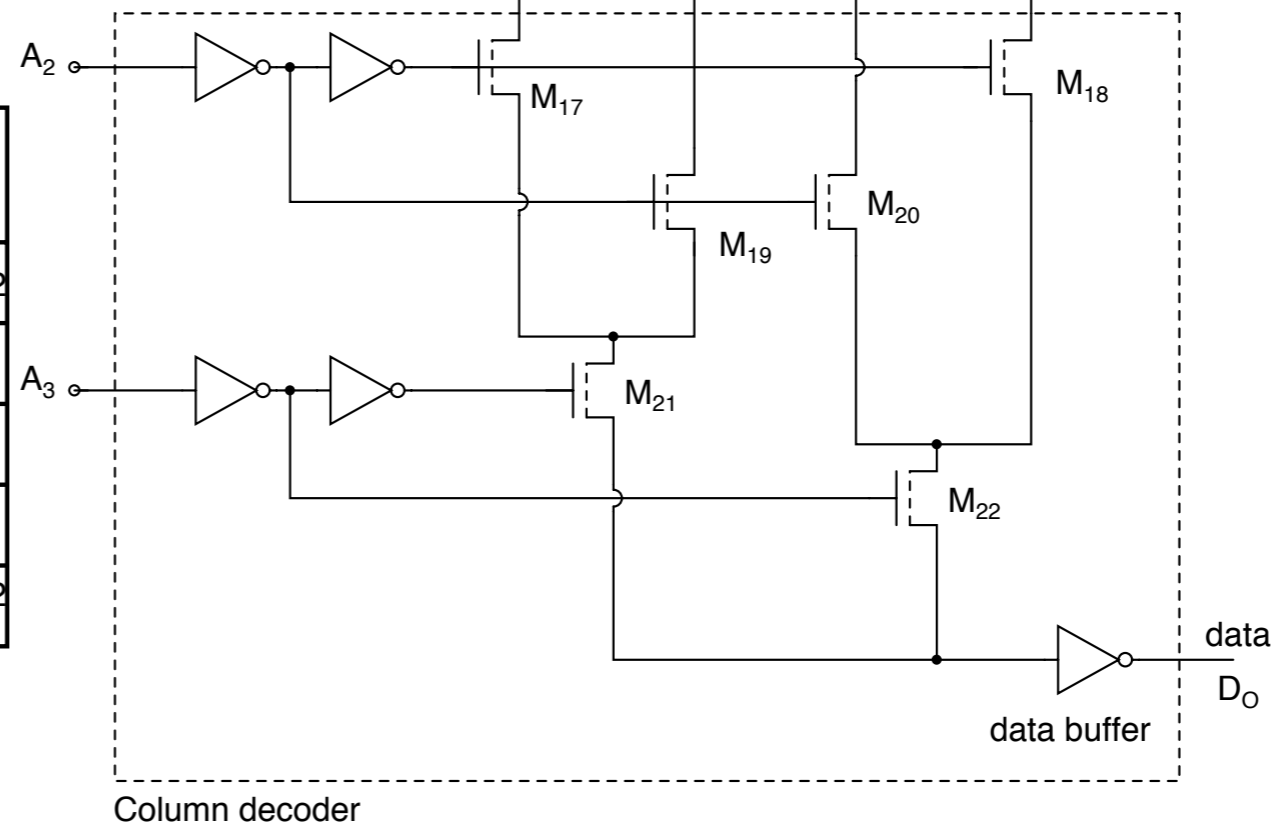


address $A_3A_2A_1A_0$	D_O	transistors "ON" (subscripts only)
0101		
1000		
0010		
1010		
0001		





address $A_3A_2A_1A_0$	D_0	transistors "ON" (subscripts only)
0101	0	3,4,5,6,10,13,17,18,22
1000	1	3,4,7,8,12,19,20,21
0010	0	1,2,7,8,9,11,15,19,20, 22
1010	1	1,2,7,8,9,11,15,19,20, 21
0001	1	3,4,5,6,10,13,19,20,22



Column decoder